Additional Resources: Product Page—PCB Feetprint Technical Decumentation

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PATENTED: THIS PRODUCT IS COVERED BY U.S. PATENT 5,736,910



**DOCUMENT / PART NO.: SI-52003-F** 

TITLE: 10/100BT, PoE; TAB UP, SHIELDED

ISSUE		DE	SCRI	PTIOI	N OF	CHAN	IGE			REVIE	WED	BY	A	PPRO	VED	BY	EC	N#
Α0	USE NE	USE NEW FORMAT AND PRODUCTION RELEASE				David Chan			D	Danny Kwan			06257					
<b>A</b> 1	Update the circuit drawing							Bain Liu			Steve Weller			06383				
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PAGE	1	2	3	4														
REV.	A1	A1	A1	A1														
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REV.															24-	0435-	-F RE	V A(



Additional Resources:

Product Page

## ELECTRICAL CHARACTERISTICS @ 25°C

1.0 TURNS RATIO:

(P1-P3): (J1-J2) 1CT: 1CT ±2% (P4-P5):(J3-J6) 1CT: 1CT ±2%

2.0 DC RESISTANCE:

(P1-P3): (P4-P5) 1.4 OHMS (J1-J2): (J3-J6) 1.2 OHMS

3.0 INDUCTANCE:

(P1-P3) 350uH MIN. @ 0.1V, 100KHz, 8mA DC BIAS (P4-P5) 350uH MIN. @ 0.1V, 100KHz, 8mA DC BIAS

4.0 LEAKAGE INDUCTANCE:

(P4-P5) WITH J6 AND J3 SHORT 0.3uH MAX. @ 1MHz (P1-P3) WITH J2 AND J1 SHORT 0.3uH MAX. @ 1MHz

5.0 INTERWINDING CAPACITANCE:

(P4,P5) TO (J3,J6) 60pF TYP @ 1MHz (P1.P2.P3) TO (J1,J2) 60pF TYP @ 1MHz

6.0 RETURN LOSS: (P1-P3)=100 OHMS REF. AND (P4-P5)=100 OHM REF.

1MHz TO 30MHz 30MHz TO 60MHz -18dB MIN. -(19-20LOG(f/30MHz)) 60MHz TO 80MHz 12dB MIN.

7.0 DIELECTRIC WITHSTAND:

(J3,J6) TO (P4,P5) 1500Vms (J1,J2) TO (P1,P3) 1500Vrms

8.0 INSERTION LOSS: RS=RL=100 OHMS 1MHz-65MHz

9.0 RISE TIME: RS=RL=100 OHMS OUTPUT VOLTAGE = 1V PEAK PULSE WIDTH = 112nS

3.0nS MAX 3.0nS MAX

TITLE

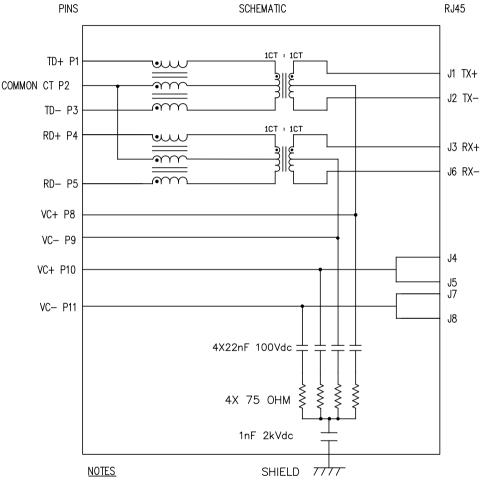
10.0 CROSS TALK:

11.0 CM TO CM ATTENUATION:

-35dB MIN.

30MHz TO 100MHz -30dB MIN. 100MHz TO 130MHz -20dB MIN.

350mA MAX @ 57 VDC CONTINUOUS 500mA MAX @ 57 VDC FOR 200 MILLSECONDS 12.0 BALANCED DC LINE CURRENT:



1.0 DESIGNED TO SUPPORT IEEE 802.3

ORIGINATED BY	DATE
Zeng Xiaochun	SI-52003-F
DRAWN BY	DATE
Duan Jun	SI-52003-F

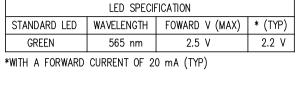
**MagJack®** 10/100BT, PoE **TAB UP. SHIELDED** PATENTED

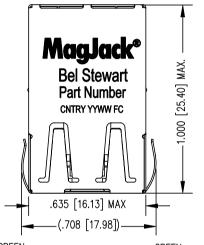
-1dB MAX

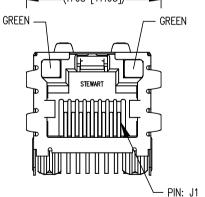
PART NO. / DRAWING NO.	STANDA	RD DIM.	[] METRIC DIM. AS REFERENCE			
SI-52003-F	TOL. IN INCH		UNIT : INCH [mm]	REV.: A1		
FILE NAME	.X		SCALE: N/A	SIZE: A4		
SI-52003-F.DWG	.xx		SCALE: N/A	SIZE: A4		
31-32003-F.DVVG	.xxx	±0.005	$\oplus$	PAGE: 2		



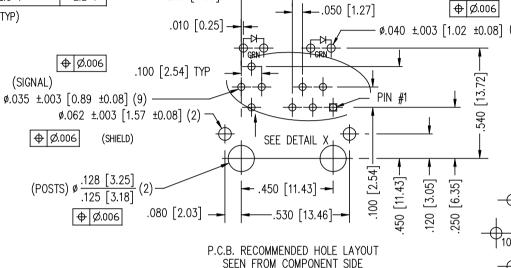
Additional Resources



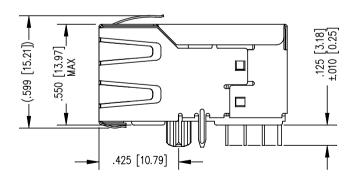




TITLE



ALL CENTERLINE DIMENSIONS ARE BASIC.



## NOTES:

1. CONNECTOR MATERIALS:

HOUSING: THERMOPLASTIC UL94 V-0 CONTACT/SHIELD: COPPER ALLOY SHIELD PLATING: NICKEL OR TIN

CONTACT PLATING: 50 MICRO-INCH SELECTIVE HARD GOLD PLATING

OR EQUIVALENT IN CONTACT AREA

DETAIL X

2. PIN NOT ELECTRICALLY CONNECTED MAYBE OMITTED. SEE ELECTRICAL DRAWING FOR OMITTED PINS.

- 3. TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS.
- 4. ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE ±.005 [0.13]
- REFLOW AND WAVE SOLDER COMPATIBLE -260°C FOR 10 SECONDS MAX.

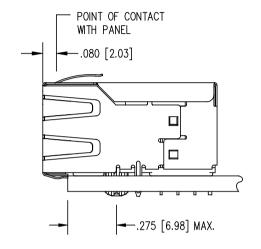
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PART NO. / DRAWING NO.	STANDA	RD DIM.	[] METRIC DIM. AS REFERENCE				
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51-52003-F.DWG	.XXX	±0.005		PAGE: 3			



Additional Resources:



- THE SUGGESTED PANEL OPENING IS INTENDED
   TO GIVE THE USER THE ABILITY TO HAVE
   REASONABLE JACK / PANEL CLEARANCES
   YET MAINTAIN RELIABLE GROUNDING
   CAPABILITY.

ORIGINATED BY	DATE
Zeng Xiaochun	SI-52003-F
DRAWN BY	DATE
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PART NO. / DRAWING NO.	STANDA	RD DIM.	[] METRIC DIM. AS REFERENCE				
SI-52003-F	TOL. IN	INCH	UNIT : INCH [mm]	REV.:			
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	l .xxx	±0.005		· ~~			



**A1**