

# Q24S30033

## Quarter-Brick DC-DC Converter

The **Q24S30033** surface mounted DC-DC converter offers unprecedented performance in the industry-standard quarter brick format. This is accomplished through the use of patent pending circuit and packaging techniques to achieve ultra-high efficiency, excellent thermal performance and a very low body profile.

In telecommunications applications the **Q Family** 30 A converters provide thermal performance that far exceeds all quarter bricks and is comparable even to existing half-bricks. Low body profile and the preclusion of heatsinks minimize airflow shadowing, thus enhancing cooling for downstream devices. The use of 100% surface-mount technologies for assembly, coupled with advanced electric and thermal circuitry and packaging, results in a product with extremely high quality and reliability.



### Key Features & Benefits

- RoHS lead free and lead-solder-exempt products are available
- Delivers up to 30 A
- Higher current capability at 70 °C than existing quarter brick and 30 A half-brick converters
- High efficiency: 88% @ 30 A, 89% @ 15 A
- Starts-up into pre-biased output
- No minimum load required
- No heatsink required
- Low profile: 0.26" [6.6 mm]
- Light weight: 1 oz [28 g] typical
- Industry-standard footprint: 1.45" x 2.30"
- Meets Basic Insulation Requirements of EN60950
- On-board LC input filter
- Fixed frequency operation
- Fully protected
- Remote output sense
- Output voltage trim range: +10%/-20%
- Trim resistor via industry-standard equations
- High reliability: MTBF 2.6 million hours, calculated per Telcordia TR-332, Method I Case 1
- Positive or negative logic ON/OFF option
- UL 60950 recognized in U.S. & Canada, and DEMKO certified per IEC/EN 60950
- Meets conducted emissions requirements of FCC Class B and EN55022 Class B with external filter
- All materials meet UL94, V-0 flammability rating



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## 1. ELECTRICAL SPECIFICATIONS

Conditions:  $T_A = 25^\circ\text{C}$ , Airflow = 300 LFM (1.5 m/s),  $V_{in} = 24\text{ VDC}$ , unless otherwise specified.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	TYP	MAX	UNITS
<b>Absolute Maximum Ratings</b>					
Input Voltage	Continuous	0		40	VDC
Operating Ambient Temperature		-40		85	$^\circ\text{C}$
Storage Temperature		-55		125	$^\circ\text{C}$
<b>Input Characteristics</b>					
Operating Input Voltage Range		18	24	36	VDC
Input Under Voltage Lockout	Non-latching				
Turn-on Threshold		16	17	17.5	VDC
Turn-off Threshold		15	16	16.5	VDC
<b>Output Characteristics</b>					
External Load Capacitance	Plus full load (resistive)			30,000	$\mu\text{F}$
Output Current Range		0		30	ADC
Current Limit Inception	Non-latching	33	36	40	ADC
Peak Short-Circuit Current	Non-latching. Short=10m $\Omega$ .		45	55	A
RMS Short-Circuit Current	Non-latching			8	Arms
<b>Isolation Characteristics</b>					
I/O Isolation		2000			VDC
Isolation Capacitance			230		$\rho\text{F}$
Isolation Resistance		10			M $\Omega$
<b>Feature Characteristics</b>					
Switching Frequency			435		kHz
Output Voltage Trim Range <sup>1</sup>	Use trim equations on Page 6	-20		+10	%
Remote Sense Compensation <sup>1</sup>	Percent of $V_{OUT(NOM)}$			+10	%
Output Over-Voltage Protection	Non-latching	117	122	127	%
Over-Temperature Shutdown (PCB)	Non-latching		118		$^\circ\text{C}$
Auto-Restart Period	Applies to all protection features		100		ms
Turn-On Time			2.5		ms
<b>ON/OFF Control (Positive Logic)</b>					
Converter Off		-20		0.8	VDC
Converter On		2.4		20	VDC
<b>ON/OFF Control (Negative Logic)</b>					
Converter Off		2.4		20	VDC
Converter On		-20		0.8	VDC
<b>Input Characteristics</b>					
Maximum Input Current	30 ADC, 1.8 VDC Out @ 18 VDC In			6.3	ADC
Input Stand-by Current	$V_{in} = 24\text{ V}$ , converter disabled		3.5		mAdc

Input No Load Current (0 load on the output)	Vin = 24 V, converter enabled	140			mAdc
Input Reflected-Ripple Current	See Figure 21 - 25MHz bandwidth	6			mAPK-PK
Input Voltage Ripple Rejection	120Hz	TBD			dB
<b>Output Characteristics</b>					
Output Voltage Set Point (no load)	-40°C to 85°C	3.267	3.300	3.333	VDC
Output Regulation					
Over Line		±2	±5	mV	
Over Load		±2	±5	mV	
Output Voltage Range	Over line, load and temperature	3.250			3.350 VDC
Output Ripple and Noise - 25MHz bandwidth	Full load + 10 µF tantalum + 1 µF ceramic	30	50	mVPK-PK	
<b>Dynamic Response</b>					
Load Change 25% of Iout Max, di/dt = 0.1 A/µS	Co = 1 µF ceramic (Fig.16)	50			mV
	di/dt = 5 A/µS Co = 450 µF tant. + 1 µF ceramic (Fig.17)	140			mV
Setting Time to 1%		100			µs
<b>Efficiency</b>					
100% Load		88			%
50% Load		89			%

<sup>1)</sup> Vout can be increased up to 10% via the sense leads or up to 10% via the trim function, however total output voltage trim from all sources should not exceed 10% of VOUT(nom), in order to insure specified operation of over-voltage protection circuitry. See further discussion at end of Output Voltage Adjust /TRIM section.

## 2. OPERATIONS

### 2.1 INPUT AND OUTPUT IMPEDANCE

These power converters have been designed to be stable with no external capacitors when used in low inductance input and output circuits.

However, in many applications, the inductance associated with the distribution from the power source to the input of the converter can affect the stability of the converter. The addition of a 33 µF electrolytic capacitor with an ESR < 1 Ω across the input helps ensure stability of the converter. In many applications, the user has to use decoupling capacitance at the load. The power converter will exhibit stable operation with external load capacitance up to 30,000 µF.

### 2.2 ON/OFF (Pin 2)

The ON/OFF pin is used to turn the power converter on or off remotely via a system signal. There are two remote control options available, positive logic and negative logic and both are referenced to Vin(-). Typical connections are shown in Fig. 1.

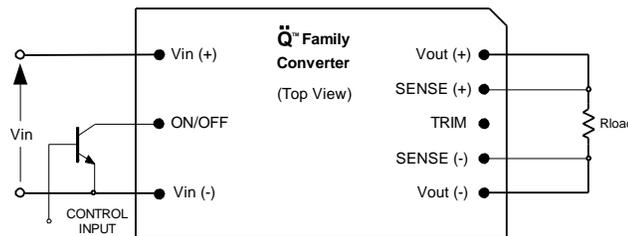


Figure 1. Circuit configuration for ON/OFF function.

The positive logic version turns on when the ON/OFF pin is at logic high and turns off when at logic low. The converter is on when the ON/OFF pin is left open.

The negative logic version turns on when the pin is at logic low and turns off when the pin is at logic high. The ON/OFF pin can be hard wired directly to Vin(-) to enable automatic power up of the converter without the need of an external control signal.

ON/OFF pin is internally pulled-up to 5 V through a resistor. A mechanical switch, open collector transistor, or FET can be used to drive the input of the ON/OFF pin. The device must be capable of sinking up to 0.2 mA at a low level voltage of  $\leq 0.8$  V. An external voltage source of  $\pm 20$  V max. may be connected directly to the ON/OFF input, in which case it should be capable of sourcing or sinking up to 1 mA depending on the signal polarity. See the Start-up Information section for system timing waveforms associated with use of the ON/OFF pin.

### 2.3 REMOTE SENSE (PINS 5 AND 7)

The remote sense feature of the converter compensates for voltage drops occurring between the output pins of the converter and the load. The SENSE(-) (Pin 5) and SENSE(+) (Pin 7) pins should be connected at the load or at the point where regulation is required (see Fig. 2).

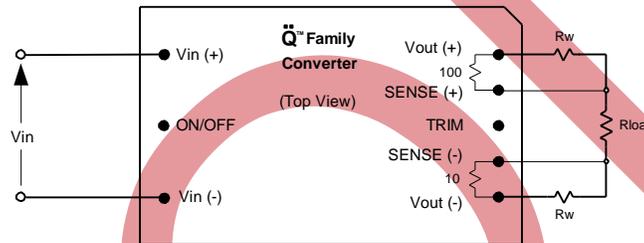


Figure 2. Remote sense circuit configuration.

If remote sensing is not required, the SENSE(-) pin must be connected to the Vout(-) pin (Pin 4), and the SENSE(+) pin must be connected to the Vout(+) pin (Pin 8) to ensure the converter will regulate at the specified output voltage. If these connections are not made, the converter will deliver an output voltage that is slightly higher than the specified value.

Because the sense leads carry minimal current, large traces on the end-user board are not required. However, sense traces should be located close to a ground plane to minimize system noise and insure optimum performance. When wiring discretely, twisted pair wires should be used to connect the sense lines to the load to reduce susceptibility to noise.

The converter's output over-voltage protection (OVP) senses the voltage across Vout(+) and Vout(-), and not across the sense lines, so the resistance (and resulting voltage drop) between the output pins of the converter and the load should be minimized to prevent unwanted triggering of the OVP.

When utilizing the remote sense feature, care must be taken not to exceed the maximum allowable output power capability of the converter, equal to the product of the nominal output voltage and the allowable output current for the given conditions. When using remote sense, the output voltage at the converter can be increased by as much as 10% above the nominal rating in order to maintain the required voltage across the load. Therefore, the designer must, if necessary, decrease the maximum current (originally obtained from the derating curves) by the same percentage to ensure the converter's actual output power remains at or below the maximum allowable output power.

### 2.4 OUTPUT VOLTAGE ADJUST / TRIM (PIN 6)

The converter's output voltage can be adjusted up 10% or down 20% relative to the rated output voltage by the addition of an externally connected resistor. Trim up to 10% is guaranteed only at  $V_{in} \geq 20$  V, and it is marginal (8% to 10%) at  $V_{in} = 18$  V.

The TRIM pin should be left open if trimming is not being used. To minimize noise pickup, a 0.1  $\mu$ F capacitor is connected internally between the TRIM and SENSE(-) pins.

To increase the output voltage, refer to Fig. 3. A trim resistor,  $R_{T-INCR}$ , should be connected between the TRIM (Pin 6) and SENSE(+) (Pin 7), with a value of:

$$R_{T-INCR} = \frac{5.11 \times (100 + \Delta) \times V_{O-NOM}}{1.225\Delta} - \frac{626}{\Delta} - 10.22 \text{ [k}\Omega\text{]},$$

where,

**R<sub>T-INCR</sub>** = Required value of trim-up resistor [kΩ]

**V<sub>O-NOM</sub>** = Nominal value of output voltage [V]

$$\Delta = \left| \frac{(V_{O-REQ} - V_{O-NOM})}{V_{O-NOM}} \right| \times 100 \quad [\%]$$

**V<sub>O-REQ</sub>** = Desired (trimmed) output voltage [V].

When trimming up, care must be taken not to exceed the converter's maximum allowable output power. See previous section for a complete discussion of this requirement.

To decrease the output voltage (Fig. 4), a trim resistor, **R<sub>T-DECR</sub>**, should be connected between the TRIM (Pin 6) and SENSE(-) (Pin 5), with a value of:

$$R_{T-DECR} = \frac{511}{|\Delta|} - 10.22 \quad [k\Omega]$$

where,

**R<sub>T-DECR</sub>** = Required value of trim-down resistor [kΩ] and **Δ** is defined above.

**Note:**

The above equations for calculation of trim resistor values match those typically used in conventional industry-standard quarter-bricks.

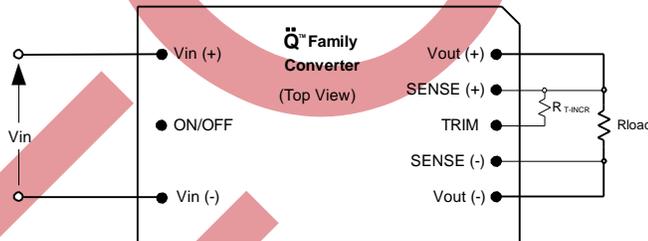


Figure 3. Configuration for increasing output voltage.

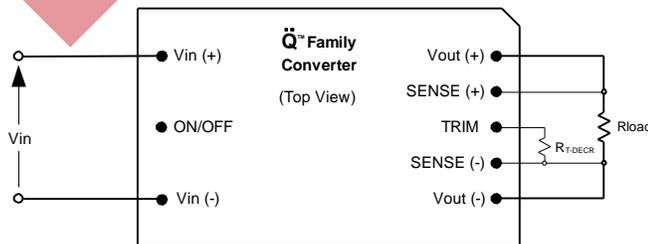


Figure 4. Configuration for decreasing output voltage.

Trimming/sensing beyond 110% of the rated output voltage is not an acceptable design practice, as this condition could cause unwanted triggering of the output over-voltage protection (OVP) circuit. The designer should ensure that the difference between the voltages across the converter's output pins and its sense pins does not exceed 0.33 V, or:

$$[V_{OUT(+)} - V_{OUT(-)}] - [V_{SENSE(+)} - V_{SENSE(-)}] \leq 0.33 \text{ [V]}$$

This equation is applicable for any condition of output sensing and/or output trim.

### 3. PROTECTION FEATURES

#### 3.1 INPUT UNDERVOLTAGE LOCKOUT

Input under-voltage lockout is standard with this converter. The converter will shut down when the input voltage drops below a pre-determined voltage.

The input voltage must be at least 17.5 V for the converter to turn on. Once the converter has been turned on, it will shut off when the input voltage drops below 15 V. This feature is beneficial in preventing deep discharging of batteries used in telecom applications.

#### 3.2 OUTPUT OVERCURRENT PROTECTION (OCP)

The converter is protected against over-current or short circuit conditions. Upon sensing an over-current condition, the converter will switch to constant current operation and thereby begin to reduce output voltage. When the output voltage drops below 1.2 Vdc, the converter will shut down (Fig. 24).

Once the converter has shut down, it will attempt to restart nominally every 100 ms with a 3% duty cycle (Fig 25). The attempted restart will continue indefinitely until the overload or short circuit conditions are removed or the output voltage rises above 1.2 Vdc.

#### 3.3 OUTPUT OVERVOLTAGE PROTECTION (OVP)

The converter will shut down if the output voltage across Vout(+) (Pin 8) and Vout(-) (Pin 4) exceeds the threshold of the OVP circuitry. The OVP circuitry contains its own reference, independent of the output voltage regulation loop. Once the converter has shut down, it will attempt to restart every 100 ms until the OVP condition is removed.

#### 3.4 OVERTEMPERATURE PROTECTION (OTP)

The converter will shut down under an over-temperature condition to protect itself from overheating caused by operation outside the thermal derating curves, or operation in abnormal conditions such as system fan failure. After the converter has cooled to a safe operating temperature, it will automatically restart.

#### 3.5 SAFETY REQUIREMENTS

The converters meet North American and International safety regulatory requirements per UL60950 and EN60950. Basic Insulation is provided between input and output.

To comply with safety agencies requirements, an input line fuse must be used external to the converter. A 10-A fuse is recommended for use with this product.

#### 3.6 ELECTROMAGNETIC COMPATIBILITY (EMC)

EMC requirements must be met at the end-product system level, as no specific standards dedicated to EMC characteristics of board mounted component dc-dc converters exist. However, di/dt tests its converters to several system level standards, primary of which is the more stringent EN55022, Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement.

With the addition of a simple external filter (see application notes), all versions of the Q24S30 converters pass the requirements of Class B conducted emissions per EN55022 and FCC, and meet at a minimum, Class A radiated emissions per EN 55022 and Class B per FCC Title 47CFR, Part 15-J. Please contact di/dt Applications Engineering for details of this testing.

3.7 STARTUP INFORMATION (USING NEGATIVE ON/OFF)

**Scenario #1: Initial Startup From Bulk Supply**

ON/OFF function enabled, converter started via application of  $V_{IN}$ . See Figure 5.

Time	Comments
$t_0$	ON/OFF pin is ON; system front-end power is toggled on, $V_{IN}$ to converter begins to rise.
$t_1$	$V_{IN}$ crosses Under-Voltage Lockout protection circuit threshold; converter enabled.
$t_2$	Converter begins to respond to turn-on command (converter turn-on delay).
$t_3$	Converter $V_{OUT}$ reaches 100% of nominal value.

For this example, the total converter startup time ( $t_3 - t_1$ ) is typically 2.5 ms.

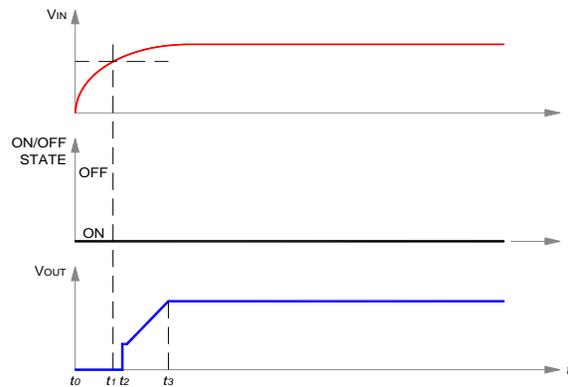


Figure 5. Start-up scenario #1.

**Scenario #2: Initial Startup Using ON/OFF Pin**

With  $V_{IN}$  previously powered, converter started via ON/OFF pin. See Figure 6.

Time	Comments
$t_0$	$V_{INPUT}$ at nominal value.
$t_1$	Arbitrary time when ON/OFF pin is enabled (converter enabled).
$t_2$	End of converter turn-on delay.
$t_3$	Converter $V_{OUT}$ reaches 100% of nominal value.

For this example, the total converter startup time ( $t_3 - t_1$ ) is typically 2.5 ms.

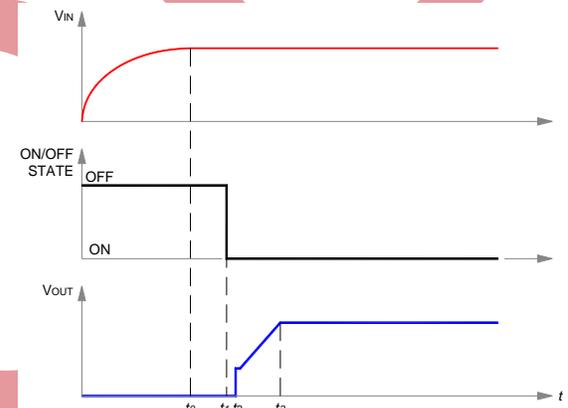


Figure 6. Startup scenario #2.

**Scenario #3: Turn-off and Restart Using ON/OFF Pin**

With  $V_{IN}$  previously powered, converter is disabled and then enabled via ON/OFF pin. See Figure 7.

Time	Comments
$t_0$	$V_{IN}$ and $V_{OUT}$ are at nominal values; ON/OFF pin ON.
$t_1$	ON/OFF pin arbitrarily disabled; converter output falls to zero; turn-on inhibit delay period (100 ms typical) is initiated, and ON/OFF pin action is internally inhibited.
$t_2$	ON/OFF pin is externally re-enabled. If $(t_2 - t_1) \leq 100$ ms, external action of ON/OFF pin is locked out by startup inhibit timer. If $(t_2 - t_1) > 100$ ms, ON/OFF pin action is internally enabled.
$t_3$	Turn-on inhibit delay period ends. If ON/OFF pin is ON, converter begins turn-on; if off, converter awaits ON/OFF pin ON signal; see Figure 5.
$t_4$	End of converter turn-on delay.
$t_5$	Converter $V_{OUT}$ reaches 100% of nominal value.

For the condition,  $(t_2 - t_1) \leq 100$  ms, the total converter startup time ( $t_5 - t_2$ ) is typically 102.5 ms. For  $(t_2 - t_1) > 100$  ms, startup will be typically 2.5 ms after release of ON/OFF pin.

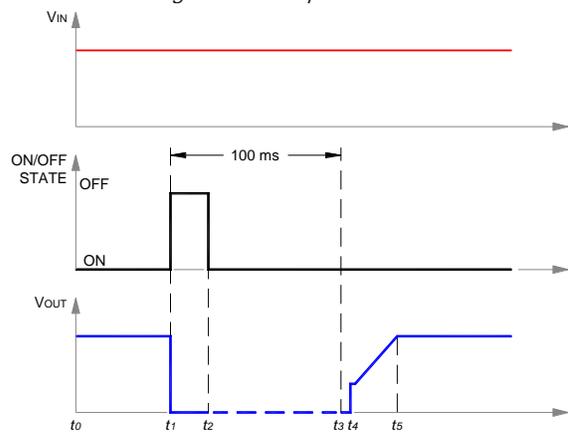


Figure 7. Startup scenario #3.



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## 4. CHARACTERIZATION

### 4.1 GENERAL INFORMATION

The converter has been characterized for many operational aspects, to include thermal derating (maximum load current as a function of ambient temperature and airflow) for vertical and horizontal mounting, efficiency, start-up and shutdown parameters, output ripple and noise, transient response to load step-change, overload and short circuit. The following pages contain specific plots or waveforms associated with the converter. Additional comments for specific data are provided below.

### 4.2 TEST CONDITIONS

All data presented were taken with the converter soldered to a test board, specifically a 0.060" thick printed wiring board (PWB) with four layers. The top and bottom layers were not metalized. The two inner layers, comprising two-ounce copper, were used to provide traces for connectivity to the converter.

The lack of metalization on the outer layers as well as the limited thermal connection ensured that heat transfer from the converter to the PWB was minimized. This provides a worst-case but consistent scenario for thermal derating purposes.

All measurements requiring airflow were made in di/dt's vertical and horizontal wind tunnel facilities using Infrared (IR) thermography and thermocouples for thermometry.

Ensuring components on the converter do not exceed their ratings is important to maintaining high reliability. If one anticipates operating the converter at or close to the maximum loads specified in the derating curves, it is prudent to check actual operating temperatures in the application. Thermographic imaging is preferable; if this capability is not available, then thermocouples may be used. di/dt recommends the use of AWG #40 gauge thermocouples to ensure measurement accuracy. Careful routing of the thermocouple leads will further minimize measurement error. Refer to Figure 26 for optimum measuring thermocouple location.

### 4.3 THERMAL DERATING

Load current vs. ambient temperature and airflow rates are given in Figs. 8 -11. Ambient temperature was varied between 25°C and 85°C, with airflow rates from 30 to 500 LFM (0.15 to 2.5 m/s), and vertical and horizontal converter mounting. For each set of conditions, the maximum load current was defined as the lowest of:

- (i) The output current at which either any FET junction temperature did not exceed a maximum specified temperature (either 105°C or 120°C) as indicated by the thermographic image, or
- (ii) The nominal rating of the converter (30 A)

During normal operation, derating curves with maximum FET temperature less than or equal to 120°C should not be exceeded. Temperature on the PCB at the thermocouple location shown in Fig. 26 should not exceed 118°C in order to operate inside the derating curves.

### 4.4 EFFICIENCY

Efficiency vs. load current plots are shown in Figs. 12 and 14 for ambient temperature of 25°C, airflow rate of 300 LFM (1.5 m/s), both vertical and horizontal orientations, and input voltages of 18 V, 27 V and 36 V. Also, plots of efficiency vs. load current, as a function of ambient temperature with  $V_{in} = 27$  V, airflow rate of 200 LFM (1 m/s) are shown for both a vertically and horizontally mounted converter in Figs. 13 and 15, respectively.

### 4.5 START-UP

Output voltage waveforms, during the turn-on transient using the ON/OFF pin for full rated load currents (resistive load) are shown without and with 10,000  $\mu$ F load capacitance in Figs. 16 and 17, respectively.

4.6 RIPPLE AND NOISE

Figure 20 shows the output voltage ripple waveform, measured at full rated load current with a 10  $\mu\text{F}$  tantalum and 1  $\mu\text{F}$  ceramic capacitor across the output. Note that all output voltage waveforms are measured across a 1  $\mu\text{F}$  ceramic capacitor. The input reflected ripple current waveforms are obtained using the test setup shown in Fig 21. The corresponding waveforms are shown in Figs. 22 and 23.

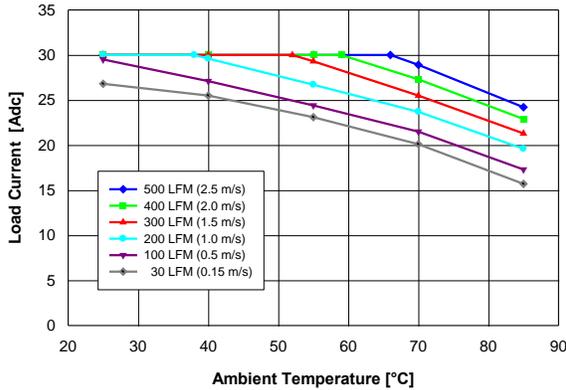


Figure 8. Available load current vs. ambient air temperature and airflow rates for converter mounted vertically with  $V_{in} = 27$  V, air flowing from pin 3 to pin 1 and maximum FET temperature  $\leq 120$  °C.

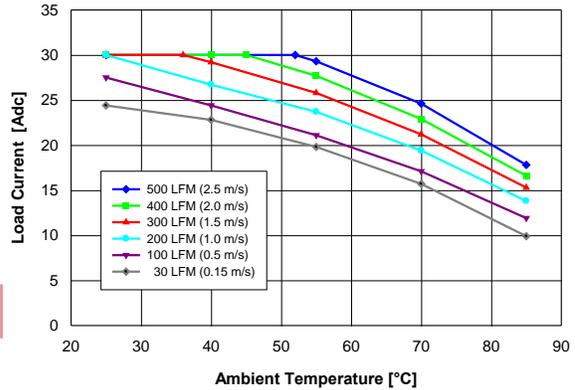


Figure 9. Available load current vs. ambient air temperature and airflow rates for converter mounted vertically with  $V_{in} = 27$  V, air flowing from pin 3 to pin 1 and maximum FET temperature  $\leq 105$  °C.

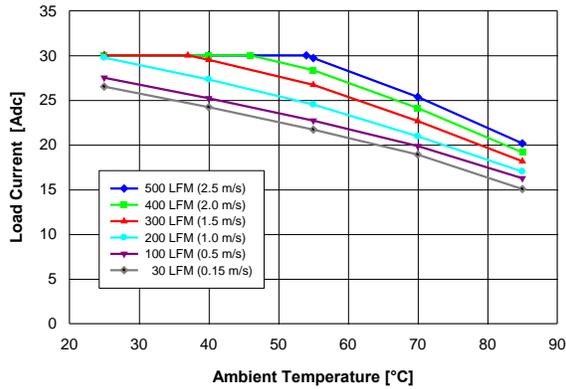


Figure 10. Available load current vs. ambient temperature and airflow rates for converter mounted horizontally with  $V_{in} = 27$  V, air flowing from pin 3 to pin 4 and maximum FET temperature  $\leq 120$  °C.

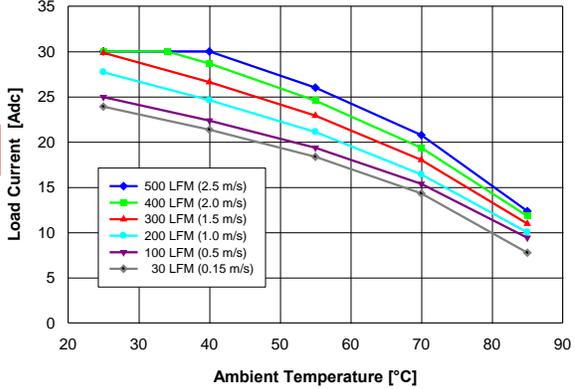


Figure 11. Available load current vs. ambient temperature and airflow rates for converter mounted horizontally with  $V_{in} = 27$  V, air flowing from pin 3 to pin 4 and maximum FET temperature  $\leq 105$  °C.

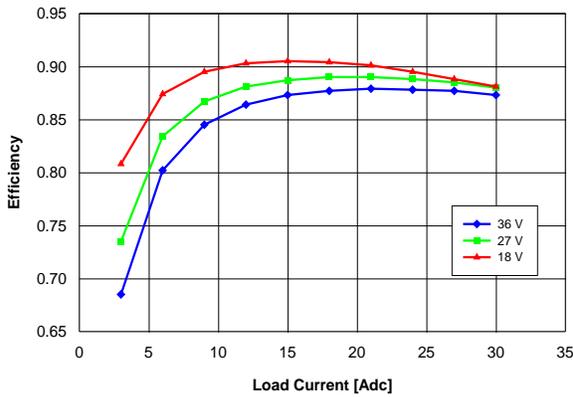


Figure 12. Efficiency vs. load current and input voltage for converter mounted vertically with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s) and  $T_a = 25\text{ }^\circ\text{C}$

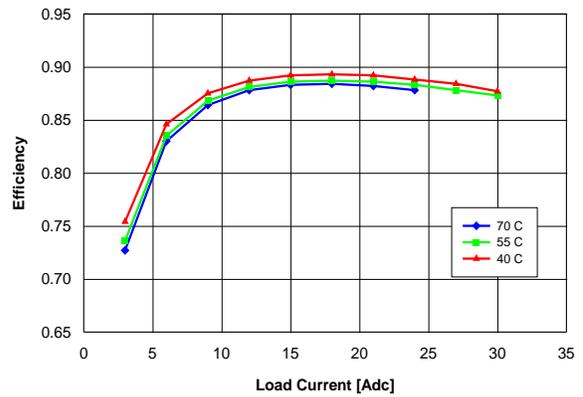


Figure 13. Efficiency vs. load current and ambient temperature for converter mounted vertically with  $V_{in} = 27\text{ V}$  and air flowing from pin 3 to pin 1 at a rate of 200 LFM (1.0 m/s).

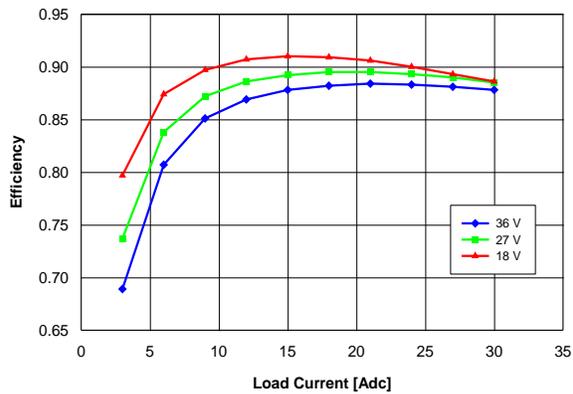


Figure 14. Efficiency vs. load current and input voltage for converter mounted horizontally with air flowing from pin 3 to pin 4 at a rate of 300 LFM (1.5 m/s) and  $T_a = 25\text{ }^\circ\text{C}$ .

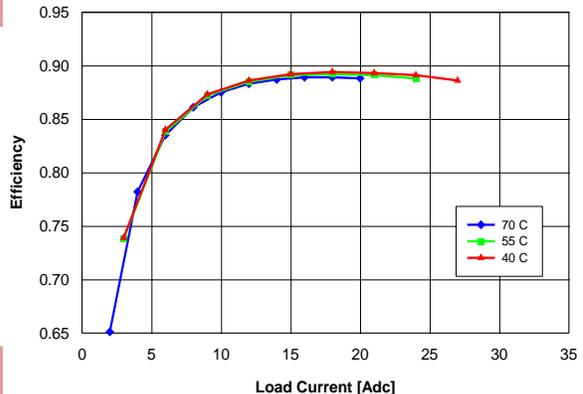


Figure 15. Efficiency vs. load current and ambient temperature for converter mounted horizontally with  $V_{in} = 27\text{ V}$  and air flowing from pin 3 to pin 4 at a rate of 200 LFM (1.0 m/s).

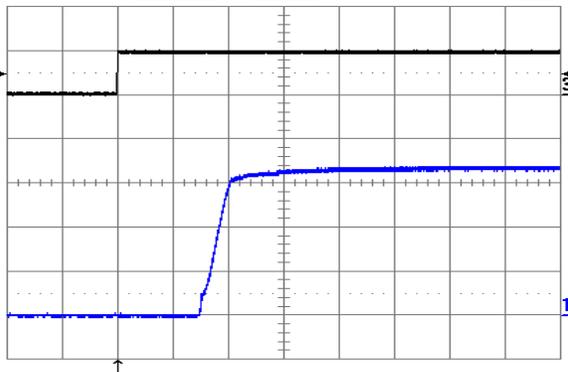


Figure 16. Turn-on transient at full rated load current (resistive) with no out-put capacitor at  $V_{in} = 24\text{ V}$ , triggered via ON/OFF pin. Top trace: ON/OFF signal (5 V/div.). Bottom trace: output voltage (1 V/div.). Time scale: 1 ms/div.

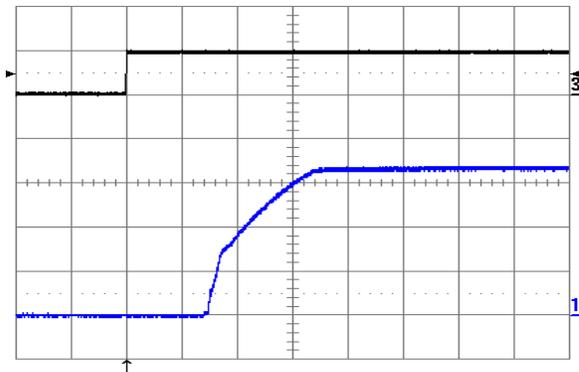


Figure 17. Turn-on transient at full rated load current (resistive) plus 10,000  $\mu\text{F}$  F at  $V_{in} = 24\text{ V}$ , triggered via ON/OFF pin. Top trace: ON/OFF signal (5 V/div.). Bottom trace: output voltage (1 V/div.). Time scale: 1 ms/div.

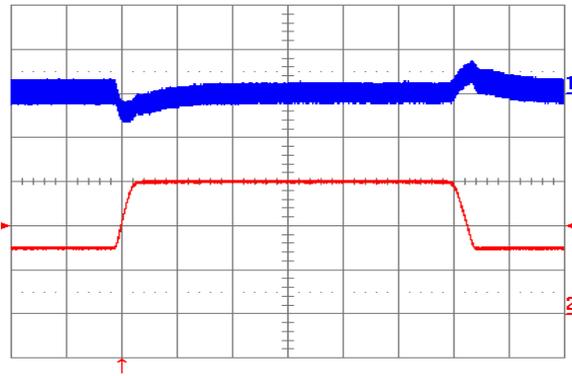


Figure 18. Output voltage response to load current step-change (7.5 A – 15 A – 7.5 A) at  $V_{in} = 24$  V. Top trace: output voltage (100 mV/div). Bottom trace: load current (5 A/div). Current slew rate: 0.1 A/ $\mu$ s.  $C_o = 1 \mu$ F ceramic. Time scale: 0.2 ms/div..

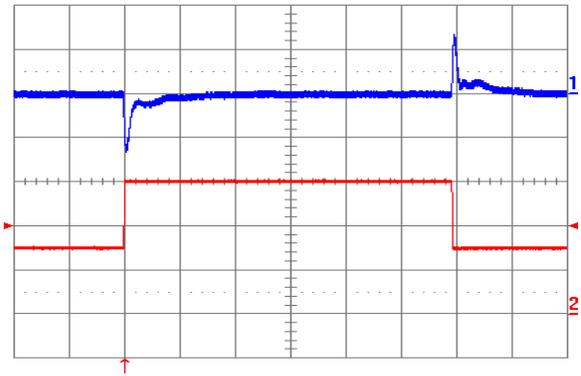


Figure 19. Output voltage response to load current step-change (7.5 A – 15 A – 7.5 A) at  $V_{in} = 24$  V. Top trace: output voltage (100 mV/div). Bottom trace: load current (5 A/div). Current slew rate: 5 A/ $\mu$ s.  $C_o = 450 \mu$ F tantalum + 1  $\mu$ F ceramic. Time scale: 0.2 ms/d

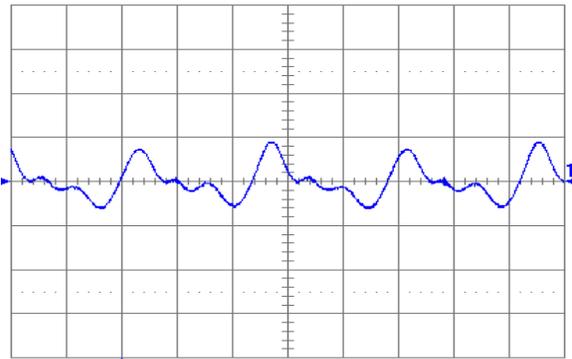


Figure 20. Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with  $C_o = 10 \mu$ F tantalum + 1 $\mu$ F ceramic and  $V_{in} = 24$  V. Time scale: 1  $\mu$ s/div.

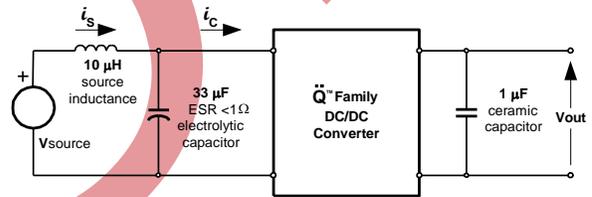


Figure 21. Test Set-up for measuring input reflected ripple currents,  $i_c$  and  $i_s$ .

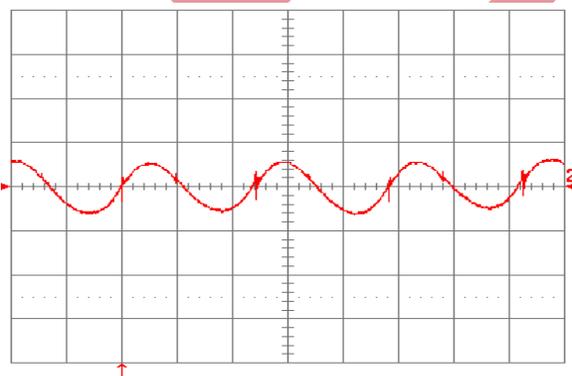


Figure 22. Input reflected ripple current,  $i_c$  (100 mA/div), measured at input terminals at full rated load current and  $V_{in} = 24$  V. Refer to Fig. 21 for test setup. Time scale: 1  $\mu$ s/div.

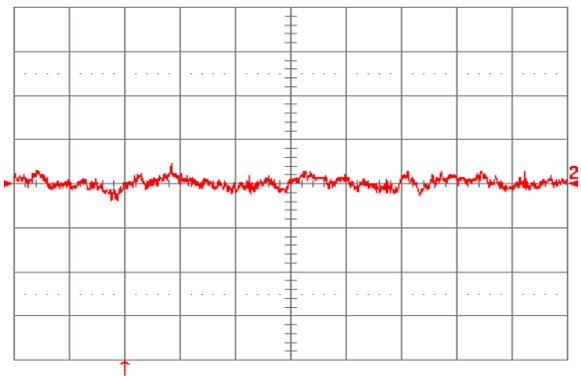


Figure 23. Input reflected ripple current,  $i_s$  (10 mA/div), measured through 10  $\mu$ H at the source at full rated load current and  $V_{in} = 24$  V. Re-fer to Fig. 21 for test setup. Time scale: 1  $\mu$ s/div.

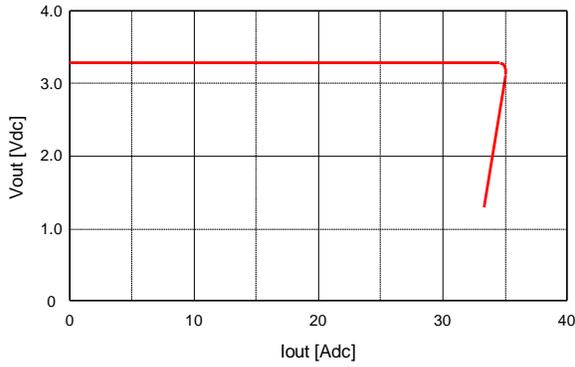


Figure 24. Output voltage vs. load current showing current limit point and converter shutdown point. Input voltage has almost no effect on current limit characteristic.

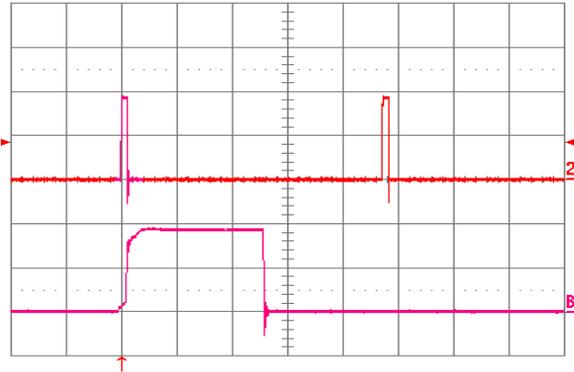


Figure 25. Load current (top trace, 20 A/div, 20 ms/div) into a 10 mΩ short circuit during restart, at  $V_{in} = 24\text{ V}$ . Bottom trace (20 A/div, 1 ms/div) is an expansion of the on-time portion of the top trace.

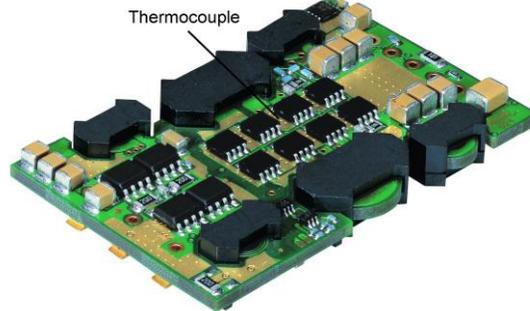
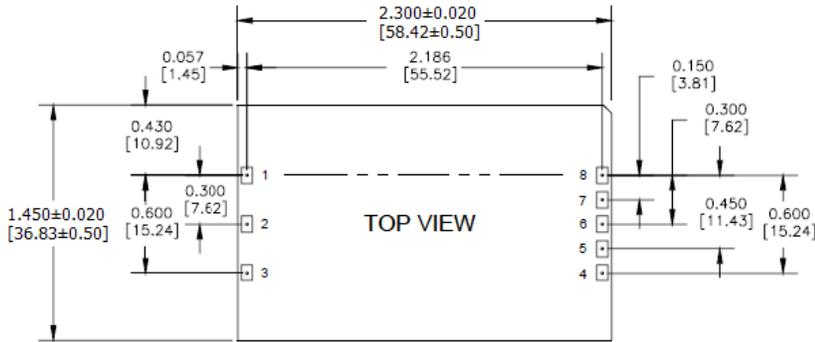


Figure 26. Location of the thermocouple for thermal testing.

## 5. MECHANICAL PARAMETERS



PAD/PIN CONNECTIONS	
Pad/Pin #	Function
1	Vin (+)
2	ON/OFF
3	Vin (-)
4	Vout (-)
5	SENSE(-)
6	TRIM
7	SENSE(+)
8	Vout (+)

- All dimensions are in inches [mm]
- Connector Material: Copper
- Connector Finish: Gold over Nickel
- Converter Weight: 1 oz [28 g] typical
- Recommended Surface-Mount Pads:  
Min. 0.080" x 0.112" [2.03 x 2.84]  
Max. 0.092" x 0.124" [2.34 x 3.15]

## 6. ORDERING INFORMATION

Product Series <sup>1</sup>	Input Voltage	Mounting Scheme	Rated Load Current	Output Voltage	ON/OFF Logic	Maximum Height [HT]	Pin Length [PL]	Special Features	RoHS
Q	24	S	30	033	- N	S	0	0	G
Quarter-Brick Format	18-36 V	Surface Mount	30 Adc	033 ⇒ 3.3 V	N ⇒ Negative P ⇒ Positive	S ⇒ 0.273"	0 ⇒ 0.00"	0 ⇒ STD	No Suffix ⇒ RoHS lead-solder-exemption compliant G ⇒ RoHS compliant for all six substances

The example above describes P/N Q24S30033-NS00G: 18-36 V input, surface mounting, 30 A @ 3.3 V output, negative ON/OFF logic, RoHS compliant for all six substances.

**For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)**

**NUCLEAR AND MEDICAL APPLICATIONS** - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

**TECHNICAL REVISIONS** - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.



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