PFD1600-12-054xA

AC-DC Power Supply

PFD1600-12-054xA is a series of 1600 Watt AC to DC power-factor-corrected (PFC) power supplies that convert standard AC or HVDC power into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

PFD1600-12-054xA series meet international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- Meet 80Plus Platinum Efficiency
- NEBS GR-1089 6 kV/ 2 Ohm CM & DM surge compliance
- Universal input voltage range: 90-264 VAC
- High voltage DC input: 180-350 VDC
- AC input with power factor correction
- Always-On standby output (Programmable 5V/5A or 12V/2.1A)
- Hot-plug capable
- Parallel operation with active digital current sharing
- Digital controls for improved performance
- High density design: 37 W/in^3
- Small form factor: 54.5(W) x 40(H) x 321(L) in mm
- I^{2}C communication interface for control, programming and monitoring with Power Management Bus protocol
- Over temperature, output over voltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- 1 Bi-color (Green/Red) LED to indicate power supply status
- IBM PLD
- Off-line bootloader function for ISP(In System Programmability)
- Support PSU health check when system request
- Blackbox recorder available

Applications

- High Performance Servers
- Routers
- Switches

1. ORDERING INFORMATION

MODELS WITH PROGRAMMABLE 5 V / 12 V STANDBY OUTPUT

PFD	1600	-	12	-	054	x	x
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PFD Front-End	1600 W		12 V		54 mm	N: Normal[1)] R: Reverse[2)]	A: C14 Socket AC: C16 Socket AF: HVDC Socket AH: Anderson 2006 Socket

1 "N" Normal Airflow from Output connector to Input AC socket
Ordering PN: PFD1600-12-054NA for C14 AC input connector, input range is 180 VDC ~ 350 VDC and 90 VAC ~ 264 VAC
Ordering PN: PFD1600-12-054NAC for C16 AC input connector, input range is 180 VDC ~ 350 VDC and 90 VAC ~ 264 VAC
Ordering PN: PFD1600-12-054NAF for both AC and HVDC (RF-203-D-1.0) input connector, input range is 180 ~ 350 VDC and 90 ~ 264 VAC
Ordering PN: PFD1600-12-054NAH for both AC and HVDC (Anderson) input connector, input range is 180 ~ 350 VDC and 90 ~ 264 VAC

2 "R" Reverse Airflow from Input AC socket to Output connector
Ordering PN: PFD1600-12-054RA for C14 AC input connector, input range is 180 VDC ~ 350 VDC and 90 VAC ~ 264 VAC
Ordering PN: PFD1600-12-054RAC for C16 AC input connector, input range is 180 VDC ~ 350 VDC and 90 VAC ~ 264 VAC
Ordering PN: PFD1600-12-054RAF for both AC and HVDC (RF-203-D-1.0) input connector, input range is 180 ~ 350 VDC and 90 ~ 264 VAC
Ordering PN: PFD1600-12-054RAH for both AC and HVDC (Anderson) input connector, input range is 180 ~ 350 VDC and 90 ~ 264 VAC

3 For difference of the AC socket and mechanical outline refer to section 13.

2. OVERVIEW

The PFD1600-12-054xA Series AC/DC power supply is combination of analog and DSP control, highly efficient front-end power supply. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range and minimal derating of output power with input voltage and temperature, the PFD1600-12-054xA maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow paths. The PFC stage is an analogue solution; MCU is used to communicate with DSP chip on secondary side. The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output, provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability. Status information is provided with front-panel LEDs. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

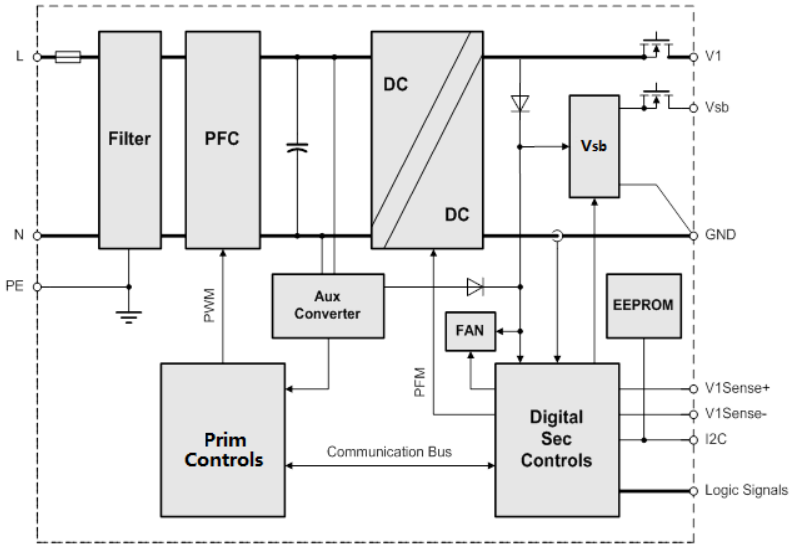


Figure 1. PFD1600-12-054xA Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,maxc}$	Maximum Input	Continuous			264	VAC

4. INPUT SPECIFICATIONS

General Condition: T_A = 0… 50°C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	Nominal Input Voltage		100		240	VAC
				240		VDC
V_i	Input Voltage Ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	90		264	VAC
			180		350	VDC
$I_{i\,max}$	Max Input Current	Vi = 100 VAC			12	A_{rms}
$I_{i\,p}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, T_{NTC} = 25°C *(Figure 4)*			40	A_p
F_i	Input Frequency		47	50/60	63	Hz
PF	Power Factor	$V_{i\,nom}$=230Vac, 50Hz, > 0.3 $I_{i\,nom}$	0.96			W/VA
$V_{i\,on}$	Turn-on Input Voltage[1]	Ramping up	84		89	VAC
			179	184	189	VDC
$V_{i\,off}$	Turn-off Input Voltage	Ramping down	75		84	VAC
			176	181	186	VDC
η	Efficiency without Fan at AC input	$V_{i\,nom}$=230Vac, 0.1·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C	82	90		%
		$V_{i\,nom}$=230Vac, 0.2·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C	90	92		
		$V_{i\,nom}$=230Vac, 0.5·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C	94	94		
		$V_{i\,nom}$=230Vac, $I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C	91	92		
	Efficiency without Fan at DC input	$V_{i\,nom}$=240VDC, 0.1·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C		89		
		$V_{i\,nom}$=240VDC, 0.2·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C		92		
		$V_{i\,nom}$=240VDC, 0.5·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C		93.5		
		$V_{i\,nom}$=240VDC, $I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C		92		
THD	Input total harmonic distortion	$V_{i\,nom}$=115Vac, 60Hz, 0.1·$I_{x\,nom}$, $V_{x\,nom}$	15			%
		$V_{i\,nom}$=115Vac, 60Hz, 0.2·$I_{x\,nom}$, $V_{x\,nom}$	10			
		$V_{i\,nom}$=115Vac, 60Hz, 0.5·$I_{x\,nom}$, $V_{x\,nom}$	5			
		$V_{i\,nom}$=115Vac, 60Hz, $I_{x\,nom}$, $V_{x\,nom}$	5			
		$V_{i\,nom}$=230Vac, 60Hz, 0.1·$I_{x\,nom}$, $V_{x\,nom}$	20			
		$V_{i\,nom}$=230Vac, 60Hz, 0.2·$I_{x\,nom}$, $V_{x\,nom}$	15			
		$V_{i\,nom}$=230Vac, 60Hz, 0.5·$I_{x\,nom}$, $V_{x\,nom}$	10			
		$V_{i\,nom}$=230Vac, 60Hz, $I_{x\,nom}$, $V_{x\,nom}$	5			
T_{hold}	Hold-up Time	After last AC zero point to V1 ≥ 11.4 V, VSB within regulation, Vi = 230 VAC, Po_ nom	12			ms
		80% nominal output power	16			
		50% nominal output power	20			

[1] The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges.

4.1 INPUT FUSE

Slow-acting 20A input fuse (5 x 20 mm) in series the L line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 1.5 µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current**.**

NOTE: Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

4.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. An analog controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage.

4.5 AC LINE TRANSIENT SPECIFICATION

Perform this test per table below for lowest nominal and highest nominal Vin. The lowest nominal shall be 100VAC. The highest nominal shall be 240VAC.Perform this test with output loads set to minimum. Repeat with output loads set to maximum, but do not exceed total power supply watts.

		DIP Time in ms												
		20	40	60	90	130	200	250	280	400	600	900	1300	2000
Lowest Nominal	-40%													
	-50%													
	-60%													
	-70%													
	-80%													
	-90%													
	-100%													
Highest Nominal	-40%													
	-50%													
	-60%													
	-70%													
	-80%													
	-90%													
	-100%													

Additional to above carry out following tests. Use 50% loading condition.
AC Drop Out Testing:

Setup 1: AC Input Voltage: 120Vac, F=60Hz, 100 cycles

Test 1: Period 1sec, 900ms on, 100ms off 100 cycles – verify power supply operates normally.
Test 2: Period 1sec, 880ms on, 120ms off 100 cycles – verify power supply operates normally.
Test 3: Period 1sec, 800ms on, 200ms off 100 cycles – verify power supply operates normally

Setup 2: AC Input Voltage: 220Vac F=50Hz, 100 cycles

Test 1: Period 1sec, 900ms on, 100ms off 100 cycles – verify power supply operates normally.
Test 2: Period 1sec, 880ms on, 120ms off 100 cycles – verify power supply operates normally
Test 3: Period 1sec, 800ms on, 200ms off 100 cycles – verify power supply operates normally.
AC 300VAC Transient Testing – models voltage surge after brown out

Setup 3: AC Input Voltage: 240Vac, F=50Hz

Test 1: Period 1sec, 900ms 264Vac, 100ms 240Vac – verify power supply operates normally.
Test 2: Period 1sec, 900ms 270Vac, 100ms 240Vac – verify power supply operates normally.
Test 3: Period 1sec, 900ms 280Vac, 100ms 240Vac – verify power supply operates normally.
Test 4: Period 1sec, 900ms 290Vac, 100ms 240Vac – verify power supply operates normally.
Test 5: Period 1sec, 900ms 300Vac, 100ms 240Vac – verify power supply operates normally.

4.6 EFFICIENCY

High efficiency (see Figure 2) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

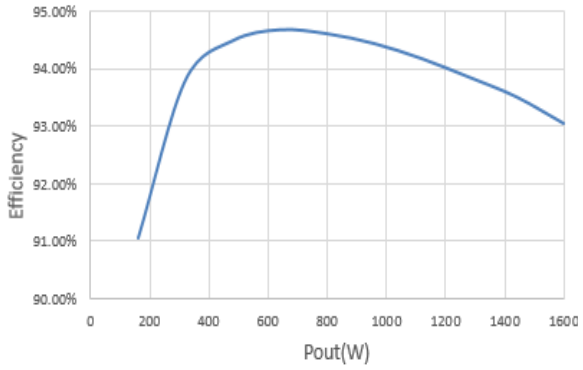


Figure 2. Efficiency vs. Pout, Vin = 230 VAC, External FAN

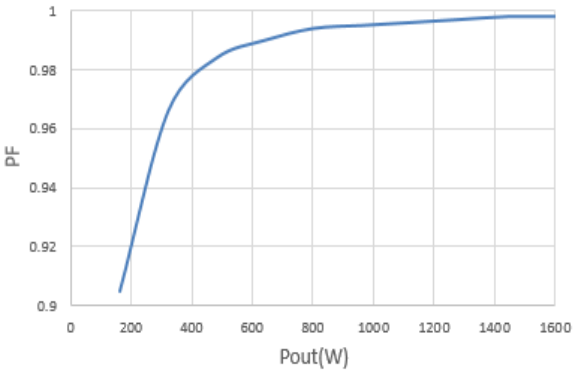


Figure 3. Power factor vs. Pout, Vin = 230 VAC

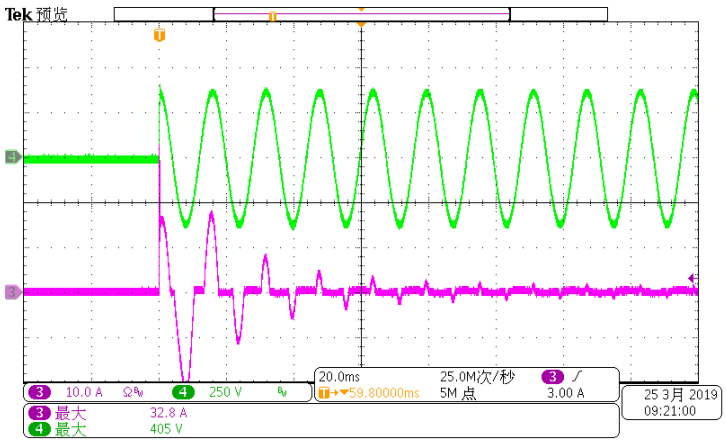


Figure 4. Inrush current, Vin = 264 VAC, 90°, CH3: Iin (10A/div), CH4: Vin (250V/div)

5. OUTPUT SPECIFICATIONS

General Condition: Ta = 0… 50°C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage			12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy	0.5 · $I_{1\ nom}$, T_{amb} = 25 °C	-0.5		+0.5	% $V_{1\ nom}$
$dV_{1\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	*264 VAC > V_{in} ≥ 180 VAC,* V_1 = 12 VDC *350 VDC > V_{in} ≥ 190 VDC,* V_1 = 12 VDC		1600		W
	Refer to Figure 7 for derating curve	*180 VAC > V_{in} ≥ 90 VAC,* V_1 = 12 VDC		1000		W
$I_{1\ nom}$	Nominal Output Current	*264 VAC > V_{in} ≥ 180 VAC,* V_1 = 12 VDC *350 VDC > V_{in} ≥ 190 VDC,* V_1 = 12 VDC		133.33		ADC
	Refer to Figure 7 for derating curve	*180 VAC > V_{in} ≥ 90 VAC,* V_1 = 12 VDC		83.33		ADC
$v_{1\ pp}$	Output Ripple Voltage	$V_{1\ nom}$, $I_{1\ nom}$, 20 MHz BW (See Section 5.1)			120	mVpp
$dV_{1\ Load}$	Load Regulation	V_1 = $V_{1\ nom}$, 0 - 100 % $I_{1\ nom}$	-200		+200	mV
$dV_{1\ Line}$	Line Regulation	V_1 = $V_{1\ min}$... $V_{1\ max}$	-100		+100	mV
dI_{share}	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%	-3		+3	A
V_{Ishare}	Current Share Bus Voltage	50% Load (single unit) 100% Load (single unit)		4 8		V
dV_{dyn}	Dynamic Load Regulation	ΔI_1 = 65% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1A/µs	-0.6		0.6	V
T_{rec}	Recovery Time	ΔI_1 = 65% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1A/µs, recovery within 1% of $V_{1\ nom}$			1	ms
$t_{AC\ V1}$	Start-up Time from AC				2	sec
$t_{V1\ rise}$	Rise Time	V_1 = 10…90% $V_{1\ nom}$	0.5		60	ms
C_{Load}	Capacitive Loading	T_a = 25°C	2200		22000	µF
5V_{SB} Standby Output						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} =25°C, VSB_SEL=1		5		VDC
$dV_{SB\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5%		+5%	V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power			25		W
$I_{SB\ nom}$	Nominal Output Current			5		ADC
$V_{SB\ pp}$	Output Ripple Voltage	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW (See Section 5.1)			80	mVpp
dV_{SB}	Droop	0 - 100 % $I_{SB\ nom}$			150	mV
$I_{SB\ max}$	Current Limitation		5.25		6.5	ADC
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 65% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_o/dt = 0.1 A/µs, recovery within 1% of $V_{1\ nom}$	-5%		5%	V_{SBnom}
T_{rec}	Recovery Time				0.5	ms
$t_{AC\ VSB}$	Start-up Time from AC	V_{SB} = 90% $V_{SB\ nom}$			2	sec
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$	0.5		30	ms
C_{Load}	Capacitive Loading	T_{amb} = 25°C			2200	µF

12 V_{SB} Standby Output						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C, VSB_SEL=0		12		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-1		+1	% $V_{SB\ nom}$
$dV_{SB\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	% $V_{SB\ nom}$
$P_{SB\ nom}$	Nominal Output Power	V_{SB} = 12 VDC		25		W
$I_{SB\ nom}$	Nominal Output Current	V_{SB} = 12 VDC		2.1		A
$V_{SB\ pp}$	Output Ripple Voltage	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW (See Section 5.1)		60	120	mVpp
dV_{SB}	Droop	0 - 100 % $I_{SB\ nom}$		270		mV
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_o/dt = 1 A/µs, recovery within 1% of $V_{1\ nom}$	-0.6		0.6	V
T_{rec}	Recovery Time				0.5	ms
$t_{AC\ VSB}$	Start-up Time from AC	V_{SB} = 90% $V_{SB\ nom}$			2	s
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$			20	ms
C_{Load}	Capacitive Loading	T_{amb} = 25°C			1,500	µF

5.1 OUTPUT VOLTAGE RIPPLE

Internal capacitance at the 12 V output (behind the OR-ing circuitry) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors (a parallel combination of 10 µF tantalum capacitor in parallel with 0.1 µF ceramic capacitors) should be added close to the power supply output.
The setup of Figure 6 has been used to evaluate suitable capacitor types. The capacitor combinations of Table 1 and Table 2 should be used to reduce the output ripple voltage. The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.

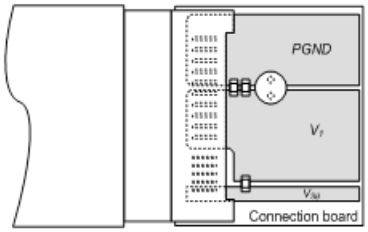


Figure 5. Output ripple test setup

NOTE: Care must be taken when using ceramic capacitors with a total capacitance of 0.1 µF to 50 µF on output V1, due to their high quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

EXTERNAL CAPACITOR V1	DV1MAX	UNIT
Standard test condition: 1 pcs 2200µF/16V/Low ESR Aluminum/ø10x20	120	mVpp
22000uF Low ESR Aluminum Caps	80	mVpp

Table 1. Suitable capacitors for V_1

EXTERNAL CAPACITOR 5Vsb	DV1MAX	UNIT
Standard test condition: 1 pcs 10 µF / 16V Low ESR Capacitor	100	mVpp
Add 1 pcs 100µF/16V OS-CON Capacitor	80	mVpp

Table 2. Suitable capacitors for 5VSB

6. PROTECTION SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuse (L)	Not user accessible, Time-lag (T)		20		A
$V_{1\ OV}$	OV Threshold V_1		110%		120%	V_{out}
Vsb OV	OV Threshold VSB		110%		120%	VSB
$I_{V1\ lim}$	Over Current Limitation V_1	V_i > 180 VAC, T_a < 50°C V_i > 90 VAC, T_a < 50°C	140 90		173.33 108.33	A
$I_{VSB\ lim}$	Over Current Limitation V_{SB}	T_a < 50°C for 5Vsb T_a < 50°C for 12Vsb	5.25 2.2		6.5 2.7	A

6.1 OVERVOLTAGE PROTECTION

The PFD1600-12-054xA provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.

6.2 VSB UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored.
LED and PWOK_H pin signal if the output voltage exceeds ±5% of its nominal voltage. Output under voltage protection is provided on the standby output only. When V_{SB} falls below 75% of its nominal voltage, the main output V_1 is inhibited.

6.3 CURRENT LIMITATION

6.3.1 MAIN OUTPUT

When main output runs in current limitation mode its output will turn OFF below 2 V but will retry to recover every 1 s interval. If current limitation mode is still present after the unit retry, output will continuously perform this routine until current is below the current limitation point. The supply will go through soft start every time it retry from current limitation mode.

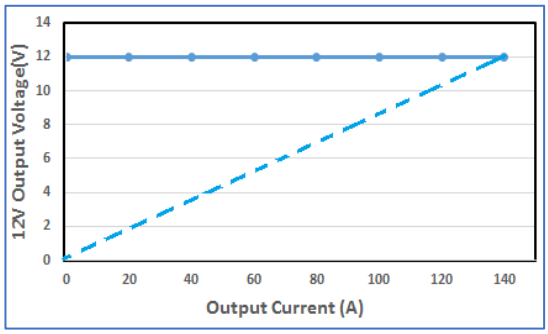


Figure 6. Current Limitation on V_1 (V_i = 230 VAC)

The main output current limitation will decrease if the ambient (inlet) temperature increases beyond 50°C or if the AC input voltage below 180 VAC (see Figure 7) for power supply applied in Canada and United States of America AC socket limit to (105°C and 12A) and other district respectively(120°C and 10A).

Note that the over current protection on V_1 specified in Figure 8 is typical value. (See also Chapter 9 Temperature and Fan Control for additional information.)

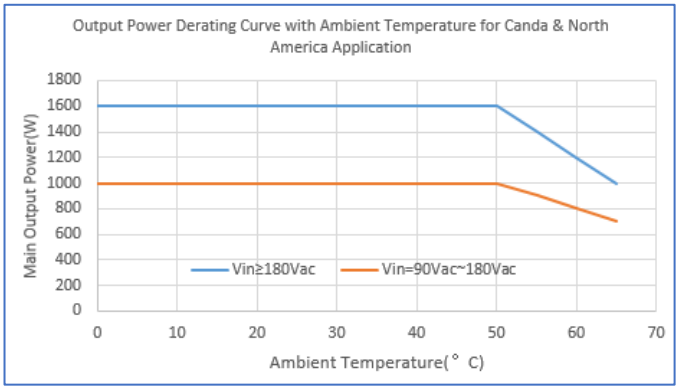


Figure 7. Iout Derating Curve for application in Canada and the USA at 50°C ambient

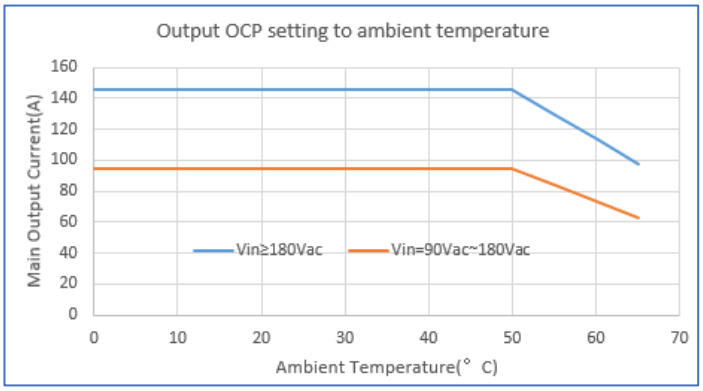


Figure 8. OCP Derating Curve with Vinac and Ambient Temperature

6.3.2 STANDBY OUTPUT

5Vsb

The standby output exhibits a substantially rectangular output characteristic down to 0V (no hiccup mode / latch off). If it runs in current limitation and its output voltage drops below the UV threshold, then the main output will be inhibited (standby remains on). The current limitation of the standby output is independent of the AC input voltage.

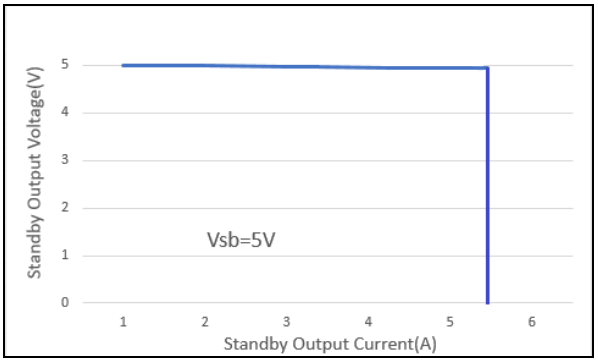


Figure 9. Current Limitation on $5V_{SB}$

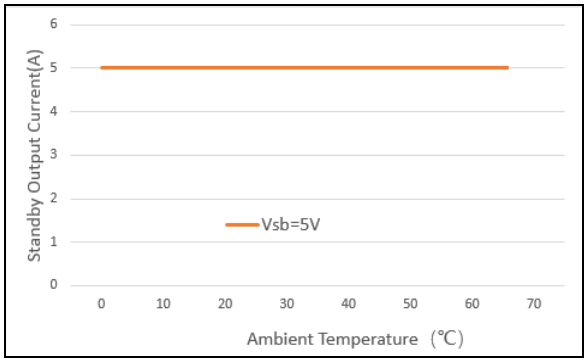


Figure 10. Temperature Derating on $5V_{SB}$

12Vsb

On the standby output, a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds $I_{SB\ lim}$. After an off-time of 1 s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly trying to restart with 1s intervals. A failure on the Standby output will shut down both Main and Standby outputs.

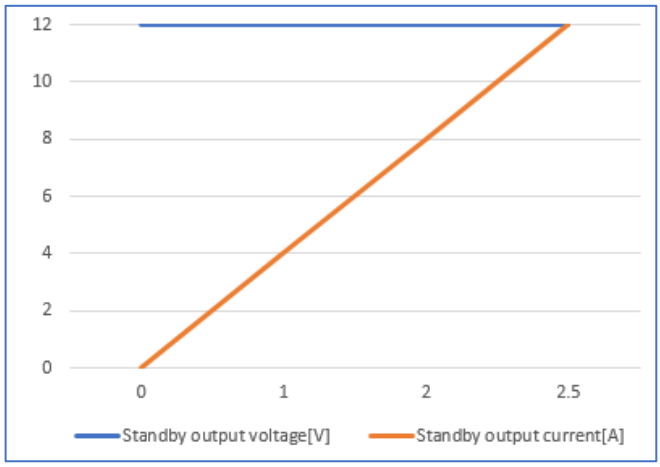


Figure 11. Current Limitation on 12 V_{SB}

6.4 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature.In an OTP condition, the PSU will shut down, when the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 5VSB remains always on, the OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition, the OTP trip temperature level shall be at least 5°C higher than over temperature warning threshold level.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	PMBUS REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Ambient temperature	Sensor located on control board close to DC end of power supply	8Dh	67	72

Table 3. Temperature Sensor Location and Thresholds

7. MONITORING

PARAMETER	DESCRIPTION / CONDITION			MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input RMS Voltage	$V_{i\ min} \le V_i \le V_{i\ max}$		-2.5		+2.5	%
$I_{i\ mon}$	Input RMS Current	$I_i > 2\ A_{rms}$		-5		+5	%
$P_{i\ mon}$	True Input Power	$I_i > 2\ A_{rms}$		-5		+5	%
$V_{1\ mon}$	V_1 Voltage			-2		+2	%
$I_{1\ mon}$	V_1 Current	I1 > 25 A		-2		+2	%
		I1 ≤ 25 A		-1		+1	A
$P_{o\ nom}$	Total Output Power	Po > 120 W		-5		+5	%
		Po ≤ 120 W		-12		+12	W
$V_{SB\ mon}$	Standby Voltage		5Vsb 12Vsb	-0.2 -0.5		+0.2 +0.5	V
$I_{SB\ mon}$	Standby Current	$I_{SB} \le I_{SB\ nom}$	5Vsb 12Vsb	-0.5		+0.5	A

8. SIGNAL & CONTROL SPECIFICATIONS

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
PSKILL / PSON_L / Inputs						
V_{IL}	Input Low Level Voltage		-0.2		0.8	V
V_{IH}	Input High Level Voltage		2.4		3.5	V
$I_{IL, H}$	Maximum Input Sink or Source Current		0		1	mA
$R_{puPSKILL\_H}$	Internal Pull Up Resistor on PSKILL_H			20		kΩ
R_{puPSON_L}	Internal Pull Up Resistor on PSON_L			20		kΩ
R_{LOW}	Resistance Pin to SGND for Low Level		0		1	kΩ
R_{HIGH}	Resistance Pin to SGND for High Level		50			kΩ
PWOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 0.5 mA	2.6		3.5	V
R_{puPWOK_H}	Internal Pull Up Resistor on PWOK_H			0.39		kΩ
ACOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 2 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 50 µA	2.6		3.5	V
R_{puACOK_H}	Internal Pull Up Resistor on ACOK_H			1		kΩ
SMB_ALERT_L Output						
V_{ext}	Maximum External Pull Up Voltage				12	V
V_{OL}	Output Low Level Voltage	I_{source} < 4 mA	0		0.4	V
I_{OH}	Maximum High Level Leakage Current				10	µA
$R_{puSMB\_ALERT\_L}$	Internal Pull Up Resistor on SMB_ALERT_L			None		kΩ

8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5 V. Therefore all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in (Figure 11) except for SMB_ALERT_L, ISHARE and I2C pins. SMB_ALERT_L pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15 V zener diode as protection device against positive voltage on pins. ISHARE pins must be interconnected without any additional components. This in-/output is disconnected from internal circuits when the power supply is switched off.

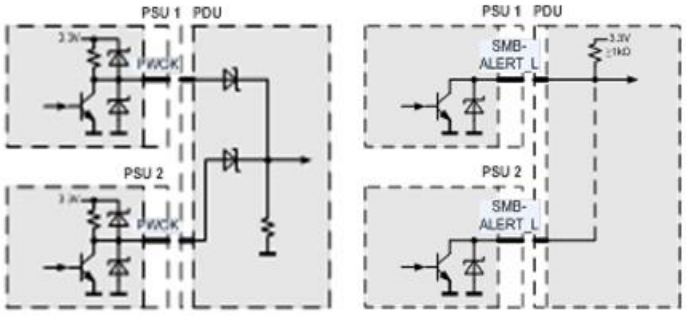


Figure 12. Interconnection of Signal Pins

8.3 FRONT LED

There is Bi-color (Green/Red) LED to indicate power supply status. Following are these definitions as:

POWER SUPPLY CONDITION	Power supply LED
No AC power to all power supplies	OFF
No AC power to this PSU only, FAN Fault	Flashing RED (1 Sec On/ 1 Sec Off)
AC Present/ only standby output on	Flashing GREEN (0.5 Sec On/ 0.5 Sec Off)
Power supply DC output ON and OK	GREEN
Power supply failure	RED
Power supply warning	Flashing RED/GREEN (0.5 Sec Red/ 0.5 Sec Green)

Table 4. LED Status

8.4 PRESENT_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT_L pin should not exceed 10 mA.

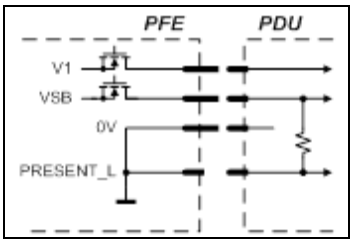


Figure 13. PRESENT_L signal pin

8.5 PSKILL_H INPUT

The PSKILL_H input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL_H input state.

8.6 AC TURN-ON / DROP-OUTS / ACOK_H

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON_L signal is pulled low and the AC line is within range. The ACOK_H signal is active-high. The timing diagram is shown in *Figure 13* and referenced in *Table 5.*

OPERATING CONDITION		MIN	MAX	UNIT
$t_{AC\ VSB}$	AC Line to 90% V_{VSB}		2	sec
$t_{AC\ V1}$	AC Line to 90% V_1		2	sec
$t_{ACOK\_H\ on1}$	ACOK_H signal on delay (start-up)		2000	ms
$t_{ACOK\_H\ on2}$	ACOK_H signal on delay (dips)		100	ms
$t_{ACOK\_H\ off}$	ACOK_H signal off delay		5	ms
$t_{VSB\ V1\ del}$	V_{SB} to V_1 delay	10	500	ms
$t_{V1\ holdup}$	Effective V_1 holdup time 50% Load 80% Load 100% Load	 20 16 12		 ms ms ms
$t_{VSB\ holdup}$	Effective V_{SB} holdup time	20		ms
$t_{ACOK\_H\ V1}$	ACOK_H to V_1 holdup	7		ms
$t_{ACOK\_H\ VSB}$	ACOK_H to V_{SB} holdup	15		ms
$t_{V1\ off}$	Minimum V_1 off time	1	2	sec
$t_{VSB\ off}$	Minimum V_{SB} off time	1	2	sec

Remark[3]: AC short dips means below 10ms; AC long dips means 10 ms to 100 ms

Table 5. AC Turn-on / Dip Timing

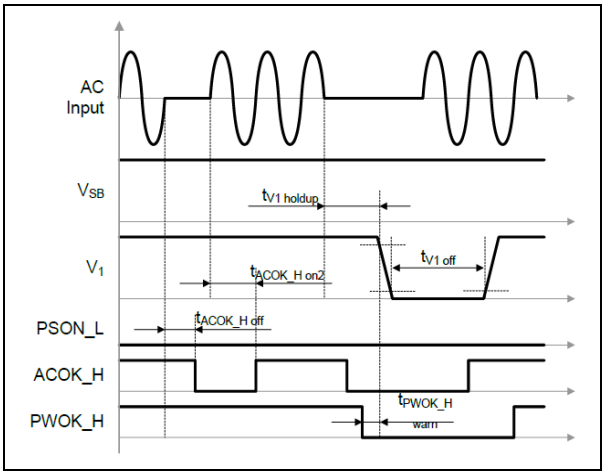


Figure 15. AC short dips

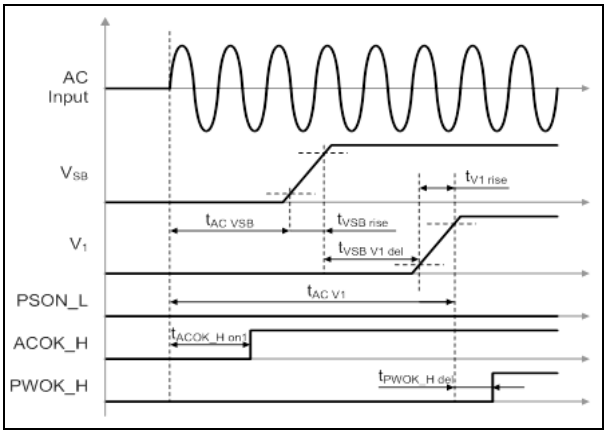


Figure 14. AC turn-on timing

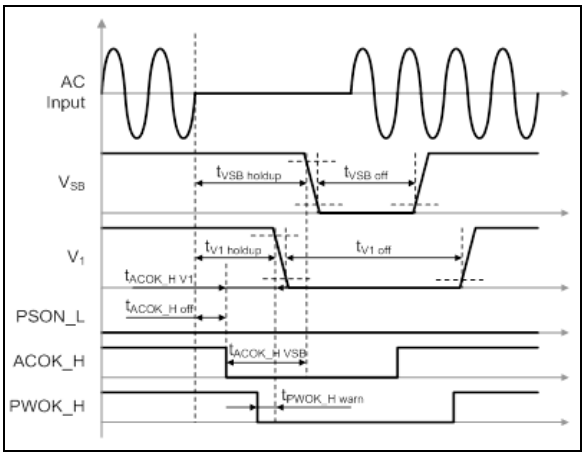


Figure 16. AC long dips

8.7 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. The timing diagram is given in *Figure 27* and the parameters in *Table 6*.

OPERATING CONDITION		MIN	MAX	UNIT
$t_{PSON\_L\ V1on}$	PSON_L to V_1 delay (on)	2	25	ms
$t_{PSON\_L\ V1off}$	PSON_L to V_1 delay (off)	2	25	ms
$t_{PSON\_L\ H\ min}$	PSON_L minimum High time	10		ms

Table 6. PSON_L timing

8.8 PWOK_H SIGNAL

The PWOK_H is an open drain output with an internal pull-up to 3.3 V indicating whether both V_{SB} and V_1 outputs are within regulation. This pin is active-low. The timing diagram is shown in Figure 17 and referenced in the Table 7.

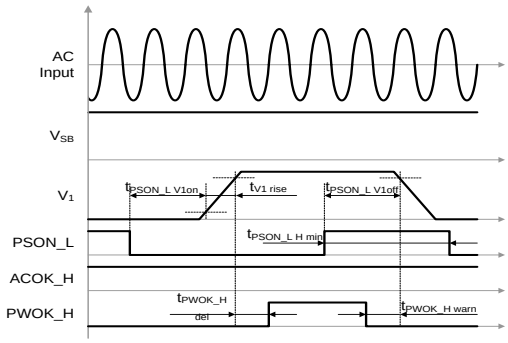


Figure 17. PSON_L and PWOK_H turn-on/off timing

OPERATING CONDITION		MIN	MAX	UNIT
$t_{PWOK\_H\ del}$	PWOK_H to V_1 delay (on)	100	500	ms
$t_{PWOK\_H\ warn}$*	PWOK_H to V_1 delay (off) caused by:			
	PSKILL_H	0	1	ms
	PSON_L, OT, Fan Failure	0.5	2.5	ms
	ACOK_H (time change with loading condition)	0.5	100	ms
	UV and OV on VSB	1	30	ms
	OC on V1 (Software trigger)	-11	0	ms
	OC on V1 (Hardware trigger)	-1	0	ms
	OV on V1	-3	0	ms

* A positive value means a warning time, a negative value a delay (after fact).

Table 7. PWOK_H timing

8.9 CURRENT SHARE

The standby output voltage can be configured to 2 different values: 5V and 12V by pulling VSB_SEL1 input pin either to GND (Logic Low) or to 3.3V.

VSB_SEL1	VSB_SEL2	VSB Voltage	UNIT
1	N/C	5	V
0	N/C	12	V

Table 8. VSB Voltage selection

8.10 CURRENT SHARE

The PFD1600-12-054xA have an active current share scheme implemented for V_1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses a digital bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.
The standby output uses a passive current share method (droop output voltage characteristic).

8.11 SENSE INPUTS

Main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 270 mV. Therefore, if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.12 VSB VOLTAGE SELECTION

The standby output voltage can be configured to two different values: 5V and 12V by pulling VSB_SEL input pin either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the VSB_SEL pin to be in High Level if left open.
NOTE: The VSB_SEL pins are only read at start-up of the power supply. Change of VSB_SEL signals during operation will result in latched fault state.

VSB_SEL	VSB Voltage
0	5V
1	12V

Table 9. VSB Voltage selection

8.13 I2C / SMBUS COMMUNICATION

The interface driver in the PFD1600-12-054xA supply is referenced to the V1 Return. The supply is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing is defined in Table 7 further characterized through:

- SCL/SDA pull-up resistor is 2kΩ in PSU side
- SCL/SDA pull-up resistor is 4.7kΩ in system side
- The SDA/SCL IOs are 3.3 tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

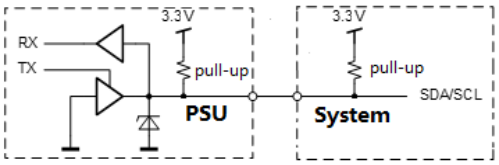


Figure 18. Physical layer of communication interface

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. The power supply responds to a read command on the general SMB_ALERT_L call address 25(0x19) by sending its status register.

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit). If only VSB is provided, communication is not possible.

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
V_{iL}	Input low voltage		-0.5		1.0	V
V_{iH}	Input high voltage		2.3		5.5	V
V_{hys}	Input hysteresis		0.15			V
V_{oL}	Output low voltage	3 mA sink current	0		0.4	V

t_r	Rise time for SDA and SCL(ViLmax-0.15V to ViHmin+0.15V)	0.65V to 2.25V $f_{SCL} \leq 100$ kHz	20+0.1Cb[2]	1000	ns
t_{of}	Output fall time (ViHmin+0.15V to ViLmax-0.15V)	2.25V to 0.65V $f_{SCL} \leq 100$ kHz	20+0.1Cb[3]	300	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
R_{pu}	External pull-up resistor	$f_{SCL} \leq 100$ kHz		1000 ns / Cb	Ω
t_{HDSTA}	Hold time (repeated) START	$f_{SCL} \leq 100$ kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	$f_{SCL} \leq 100$ kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	$f_{SCL} \leq 100$ kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	$f_{SCL} \leq 100$ kHz	4.7		µs
t_{HDDAT}	Data hold time	$f_{SCL} \leq 100$ kHz	0	3.45	µs
t_{SUDAT}	Data setup time	$f_{SCL} \leq 100$ kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	$f_{SCL} \leq 100$ kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	$f_{SCL} \leq 100$ kHz	5		ms

Table 10. I2C / SMBus Specification

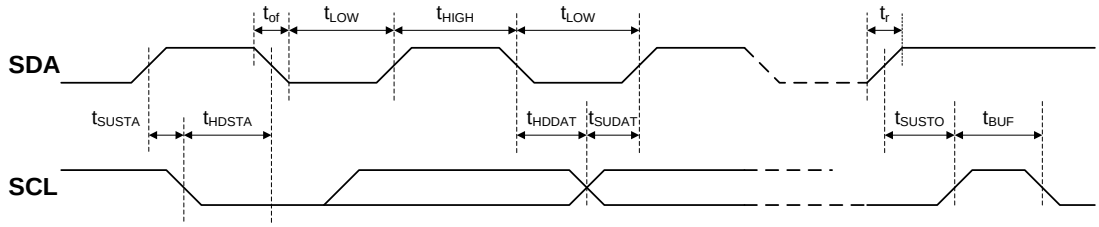


Figure 19. I2C / SMBus Timing

8.14 ADDRESS / PROTOCOL SELECTION (APS)

The address for I2C communication can be configured by pulling address input pins A0, A1 and A2 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor (10kohm) will cause the A0, A1 and A2 pin to be in High Level if left open. A fixed addressing offset exists between the Controller and the EEPROM.

A2	A1	A0	I2C Address	
			Power Management Bus Address	EEPROM Address
Reserved	0	0	0xB0	0xA0
Reserved	0	1	0xB2	0xA2
Reserved	1	0	0xB4	0xA4
Reserved	1	1	0xB6	0xA6
Reserved	0	0	Reserved	Reserved
Reserved	0	1	Reserved	Reserved
Reserved	1	0	Reserved	Reserved
Reserved	1	1	Reserved	Reserved

[2] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

8.15 CONTROLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 19). An I2C driver device assures logic level shifting (5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

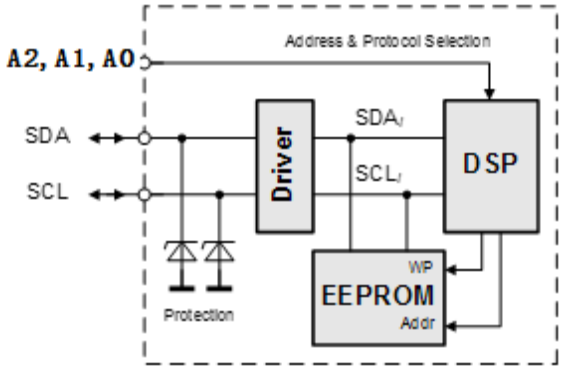


Figure 20. I2C Bus to DPS and EEPROM

8.16 EEPROM PROTOCOL

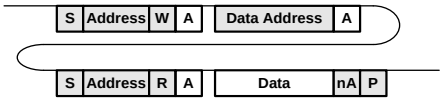
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



8.17 POWER MANAGEMENT BUS PROTOCOL

POWER MANAGEMENT BUS PROTOCOL

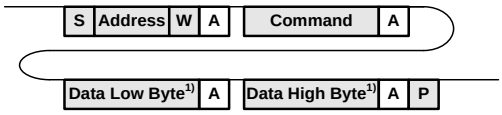
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PFD1600-12-054xA supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

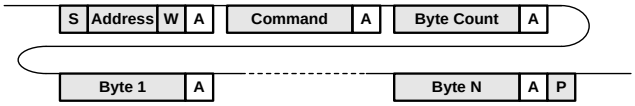
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



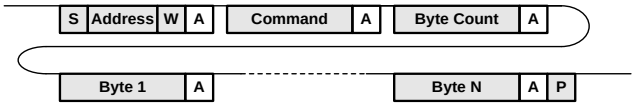
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See Programming Manual for further information.

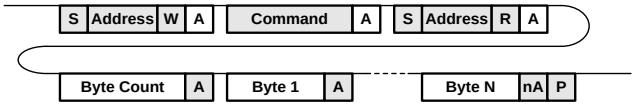


READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See Programming Manual BCA.00006 for further information.



8.18 GRAPHICAL USER INTERFACE

Bel Power Solutions provides with its “Bel Power Solutions I2C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of PFD1600-12-054XA Front-End. The utility can be downloaded on: belfuse.com/power-solutions and supports Power Management Bus™ protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the SNP-OP-BOARD-01 or YTM.G1Q01.0 Evaluation Kit it is also possible to control the PSON_L pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

NOTE: The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

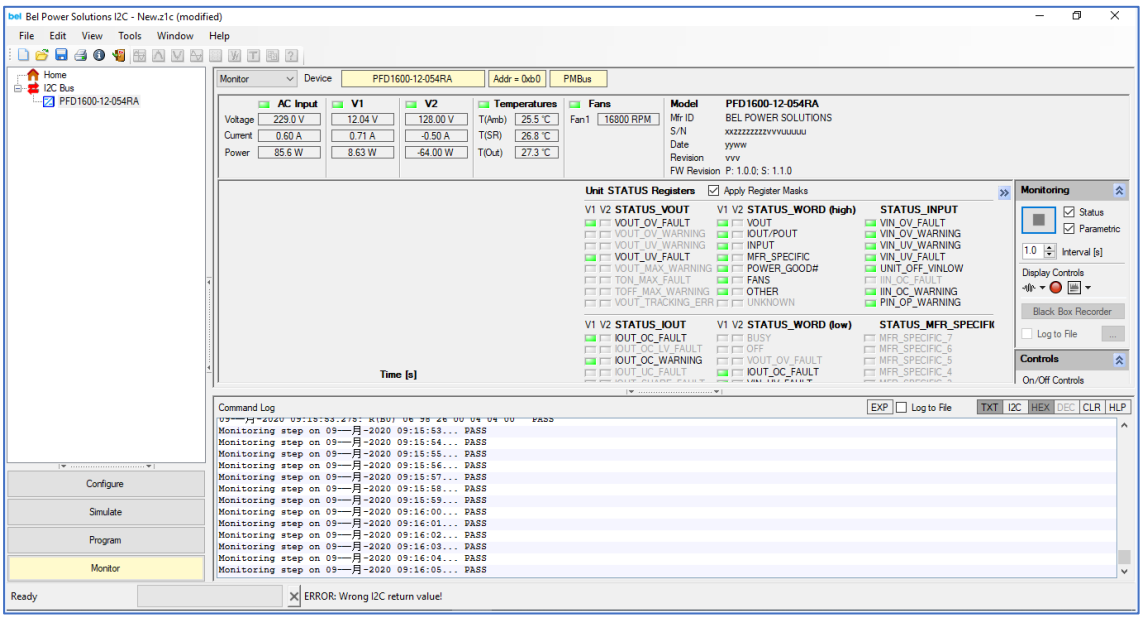


Figure 21. Monitoring dialog of the I2C Utility

9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. PFD1600-12-054NA is provided with normal airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. PFD1600-12-054NA has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the AC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the AC-inlet.

The IEC connector on the unit is rated 105°C. If 70°C mating connector is used then end user must derated the input power to meet a maximum 70°C temperature at the front, see Figure 7 in above section.

NOTE: It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

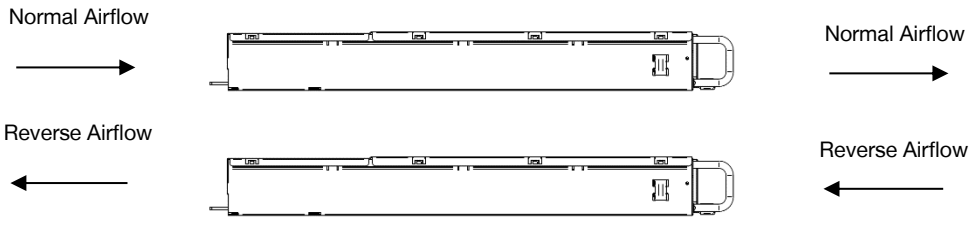


Figure 22. Airflow direction

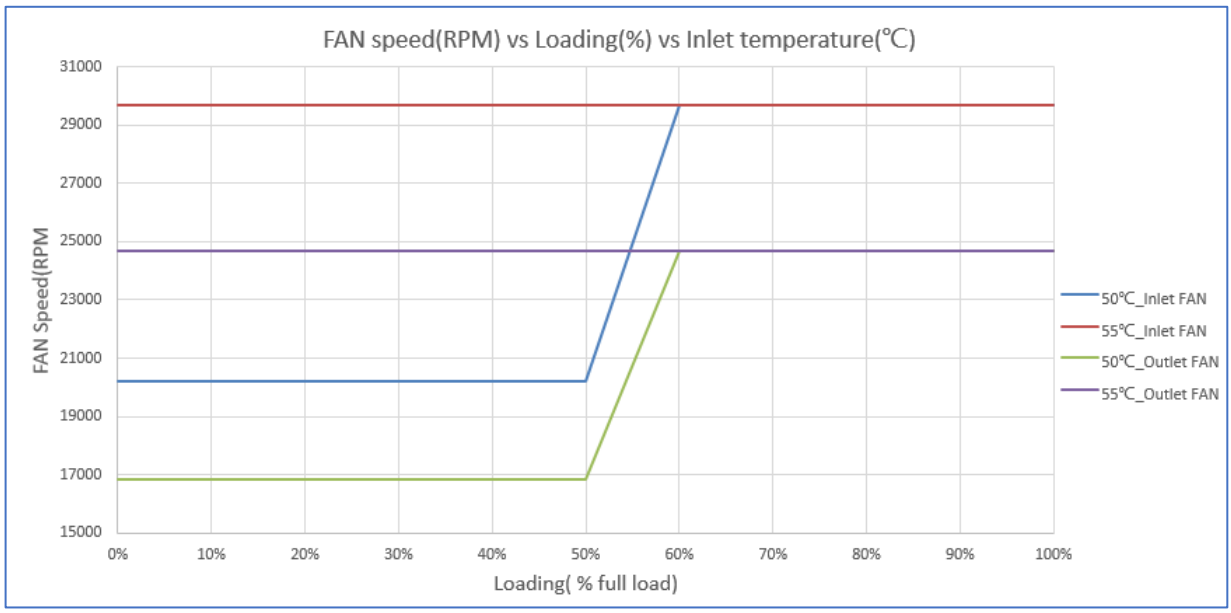


Figure 23. Fan speed vs. main output load

Note: FAN speed spec: Inlet FAN speed 29700+/-10%, Outlet FAN speed is 24700+/-10%.

Ambient/Load	0%	10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
25	20202	20202	20202	20202	20202	20202	29700	29700	29700	29700	29700
30	20202	20202	20202	20202	20202	20202	29700	29700	29700	29700	29700
35	20202	20202	20202	20202	20202	20202	29700	29700	29700	29700	29700
40	20202	20202	20202	20202	20202	20202	29700	29700	29700	29700	29700
45	20202	20202	20202	20202	20202	20202	29700	29700	29700	29700	29700
50	20202	20202	20202	20202	20202	20202	29700	29700	29700	29700	29700
55	29700	29700	29700	29700	29700	29700	29700	29700	29700	29700	29700
60	29700	29700	29700	29700	29700	29700	29700	29700	29700	29700	29700
65	29700	29700	29700	29700	29700	29700	29700	29700	29700	29700	29700

Table 11. Inlet FAN speed table

Ambient/Load	0%	10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
25	16817	16817	16817	16817	16817	16817	24700	24700	24700	24700	24700
30	16817	16817	16817	16817	16817	16817	24700	24700	24700	24700	24700
35	16817	16817	16817	16817	16817	16817	24700	24700	24700	24700	24700
40	16817	16817	16817	16817	16817	16817	24700	24700	24700	24700	24700
45	16817	16817	16817	16817	16817	16817	24700	24700	24700	24700	24700
50	16817	16817	16817	16817	16817	16817	24700	24700	24700	24700	24700
55	24700	24700	24700	24700	24700	24700	24700	24700	24700	24700	24700
60	24700	24700	24700	24700	24700	24700	24700	24700	24700	24700	24700
65	24700	24700	24700	24700	24700	24700	24700	24700	24700	24700	24700

Table 12. Outlet FAN speed table

10. ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation	A
Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute	A
Surge	NEBS GR-1089 6kV/2 Ohm CM&DM IEC6100-4-5 1kV/2 Ohm DM, 2kV/12Ohm CM	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW	A
Voltage Dips and Interruptions	IEC/EN 61000-4-11 1: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 10 ms(50HZ) 8.3ms(60HZ) 2: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 20 ms(50HZ) 16.6ms(60HZ), Redundant PSUs 3: Vi 230 V, 100% Load, Phase 0 °, Dip 30%, Duration 500ms(50HZ&60), Redundant PSUs 4: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 5000 ms 5: Vi 230 V, 100% Load, Phase 0 °, Dip 60%, Duration 100 ms 6: Vi 230 V, 100% Load, Phase 0 °, Dip 60%, Duration 200 ms 7: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 20 ms 8: Vi 200 V, 50% Load, Phase 0 °, Dip to 68Vac, Duration 500 ms	 A A A B A B V_{SB}: A, V_1: B A

10.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single unit under 4db EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, 2 units in rack system under 4db	Class A Class A
Radiated Emission	EN55022 / CISPR 22: 30 MHz … 1 GHz, QP, single unit under 4db EN55022 / CISPR 22: 30 MHz … 1 GHz, QP, 2 units in rack system under 4db	Class A Class A
Harmonic Emissions	IEC61000-3-2, Vin = 115 VAC / 60 Hz, & Vin = 230VAC/ 50 Hz, 100% Load	Class A
AC Flicker	IEC61000-3-3, Vin = 230 VAC / 60 Hz, 100% Load	Pass

11. SAFETY APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 62368-1 and UL/CSA 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Agency Approvals	cCSAus (62368-1) N+CB (62368-1) CQC /BSMI/KCC (safety +EMC) EAC /RCM (AS/NZ)		Approved by independent body (see CE Declaration)		
	Isolation Strength	Input (L/N) to case (PE)		Basic		
		Input (L/N) to output		Reinforced		
		Output to case (PE)		Connected		
d_C	Creepage / Clearance	Primary (L/N) to protective earth (PE)		According to safety standard		mm
		Primary to secondary		Meet CCC 5000 m requirement		
	Electrical Strength Test	Input to case		2.5		kVDC
		Input to output		4.0		
		Output and Signals to case				

12. ENVIRONMENTAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	$V_{i\,min}$ to $V_{i\,max}$, $I_{i\,nom}$, $I_{SB\,nom}$ below 5000 m Altitude (< 900m, keep maximum operation temperature. ≧ 900m, decrease 1° C per 300m See Table 8 or Figure 23)	0		+50	°C
T_{Aext}	Extended Temp. Range	Derating output	+50		+65	°C
T_S	Storage Temperature	Non-operational	-40		+70	°C
	Altitude	Operational, above Sea Level, refer derating to Ta	-		5000	m
	Audible Noise	Sound Pressure @$V_{i\,nom}$, 50% $I_{o\,nom}$, T_A = 25°C		65		dBA

POWER DE-RATING (LOW LINE / HIGH LINE)				
Ambient	50°C	55°C	61°C	65°C
Output Power	1000W/1600W	900W/1400W	800W/1200W	700W/1000W

Table 13. Power De-Rating

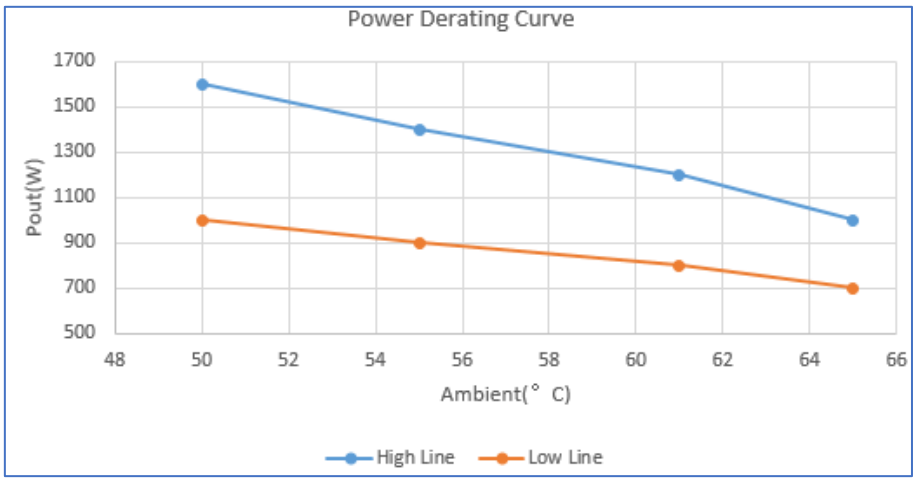


Figure 24. Power Derating curve

13. MECHANICAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		54.5		mm
		Height		40.0		
		Depth		321		
M	Weight			1.1		kg

NOTE: A 3D step file of the power supply casing is available on request.

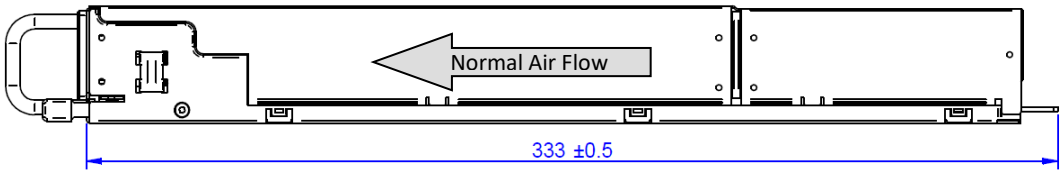


Figure 25. Side View 1

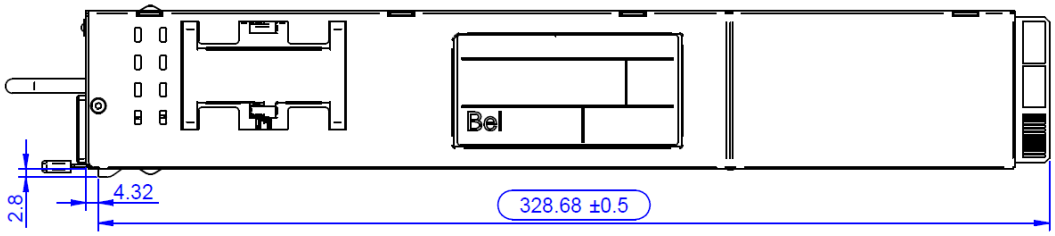


Figure 26 Top View

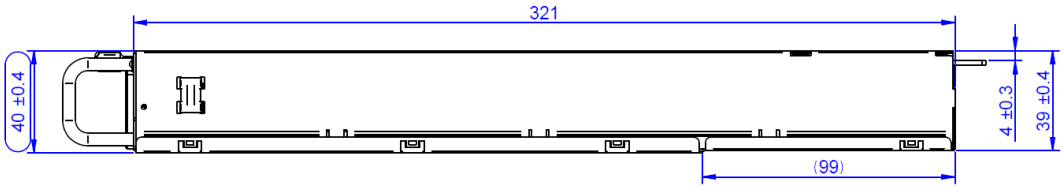


Figure 27. Side View 2

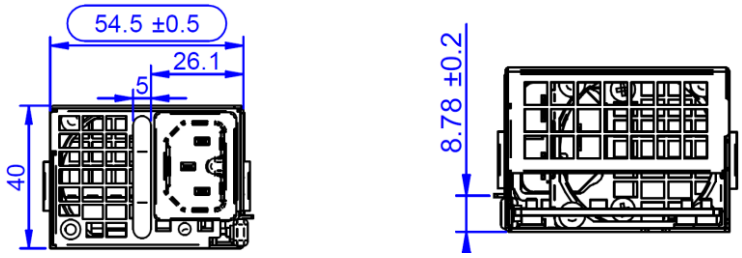


Figure 28. Front and Rear View

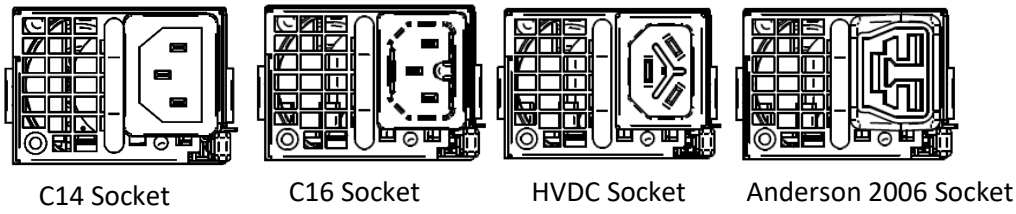
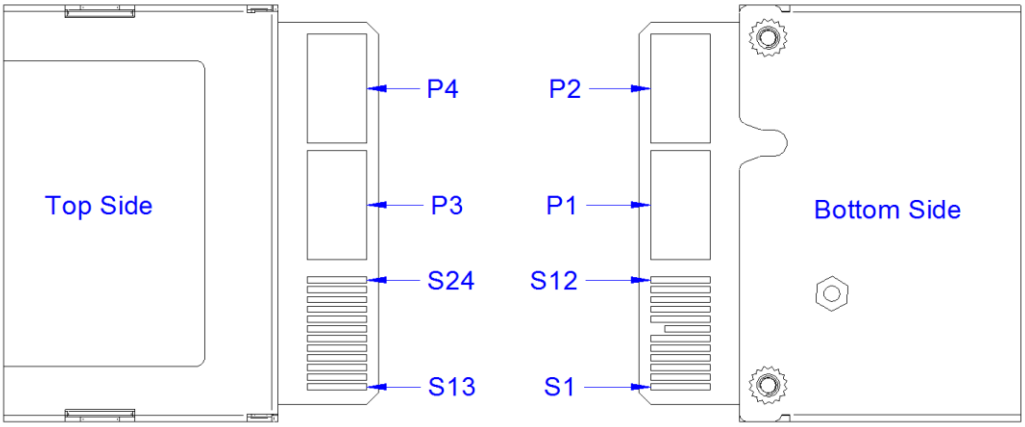


Figure 29. Front panel – input connector type

14. CONNECTIONS

AC input connector: Power supplier connector: IEC320 C16 type.
IEC320 C14 type is also available (will be different P/N).

DC output connector: GOLDEN FINGER



Mating Connector: ALLTOP TECHNOLOGY P/N: C20041-10831-T

PIN	NAME	DESCRIPTION
Output		
P1, P3	+12V	+12 VDC main output
P2, P4	GND	Power ground (return)
Control Pins		
S1	+12V Sense	Main output positive sense
S2	+12V RTN Sense	Main output negative sense
S3	+12V Current Share	Current share bus (lagging pin)
S4	SMB_ALERT/L	SMB Alert signal output: active-low
S5	SDA	I2C data signal line
S6	SCL	I2C clock signal line
S7	+PS Kill	Power supply kill (lagging pin): active-high, active High means with high voltage, PS Kill function will be active to turn off the PSU
S8	PSON/L	Power supply on input (connect to A2/B2 to turn unit on): active-low
S9	PW_OK	Power OK signal output (lagging pin): active-high
S10	PS_A1	I2C address setup pin
S11	+5V_STBY	Standby positive output
S12	+5V_STBY	Standby positive output
S13	N/C	Reserved
S14	PRESENT_L	Power supply present (lagging pin): active-low
S15	PS_A0	I2C address setup pin
S16	N/C	Reserved
S17	N/C	Reserved
S18	EEPROM_WP	
S19	ACOK/H	AC input OK signal: active-high
S20	N/C	Reserved
S21	VSB_SEL	Standby voltage selection
S22	PS_A2	I2C address setup pin (Reserved)
S23	+5V_STBY	Standby positive output
S24	+5V_STBY	Standby positive output

15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**Bel Power Solutions I2C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PFD1600-12-054xA (and other I2C units)	N/A	belfuse.com/power-solutions
	**Dual Connector Board** Connector board to operate 2 PFD1600-12-054xA units in parallel. Includes an on-board USB to I2C converter (use *Bel Power Solutions I2C Utility* as desktop software).	YTM.00117.0	belfuse.com/power-solutions

16. REVISION HISTORY

DATE	REVISION	SECTION	ISSUE	PREPARED BY	APPROVED BY
2019/08/05	1	/	First release	Rick Luo	Baojun Zeng
2019/08/13	1	10	Delete EEPROM Contents	Jack Zhou	Vim Tan
2021/04/02	2	1.5.6	Add 12Vsb parameters, update power derating curve	Rick Luo	Baojun Zeng
2021/08/20	3	8.12	Add Vsb voltage selection description	Rick Luo	Baojun Zeng
2022/01/14	4	7	Change input current/input power accuracy to 5% from 3%	ZC Wei	GT Zhang
2022/01/14	4	8.7	Change PSON_L max timing to 25ms from 20ms	ZC Wei	GT Zhang
2022/10/22	A	/	Upgrade the version to A	Xiaogang Luo	GT Zhang
2023-10-13	B	11	Update the safety approve standard and electrical strength test and isolation strength at section 11	Jason Li	Erick Su

For more information on these products consult: tech.support@psbel.com

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