TET3000 Series

TET3000-12-054xASxxx
TET3000-12xAS412
AC-DC Front-End Power Supplies



RoHS Compliant

The TET3000 is a 3000W AC to DC power-factor-corrected (PFC) power supply that converts standard AC or HVDC power into a main output of 12.0 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The TET3000 Series meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- High Efficiency, typ. 96% efficiency at half load
- Universal input voltage range: 90-305 VAC
- High voltage DC input: 190-400 VDC
- AC input with power factor correction
- Always-On standby output (Optional for 12VSB / 3A or 5VSB / 3A)
- Hot-plug capable
- Parallel operation with active analog current sharing
- Digital controls for improved performance
- High density design: 71 W/in^3
- Small form factor: 54.5 x 40.0 x 321.5 mm (2.14 x 1.57 x 12.66 in)
- I^{2}C communication interface for control, programming and monitoring with Power Management Bus Protocol
- Over temperature, output over voltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- Black Box recorder available
- Status LED with fault signaling

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

Please read our datasheet & drawing disclaimer here.

1. ORDERING INFORMATION

MODELS WITH 5V STANDBY OUTPUT

TET	3000	-	12	-	054	x	A	x
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input** [4]	**Specific code** [3]
TET Front-Ends	3000 W		12 V		54.0 mm	N: Normal [1] R: Reverse [2]	AC: C22 Socket AH: HVDC Socket	x = Blank x = S+3 digits

MODELS WITH 12V STANDBY OUTPUT

TET	3000	-	12	x	A	S412
Product Family	**Power Level**	**Dash**	**V1 Output**	**Airflow**	**Input** [4]	**VSB output**
TET Front-Ends	3000 W		12 V	N: Normal [1] R: Reverse [2]	AC: C22 Socket AH: HVDC Socket	12VSB

1 "N" Normal Airflow from Output connector to Input AC socket.
2 "R" Reverse Airflow from Input AC socket to Output connector.
3 Contact factory for availability of Specific code.
4 "AC" for C22 AC input connector, input range is 204 VDC ~ 288 VDC and 90 VAC ~ 264 VAC.
"AH" for both AC and HVDC input connector, input range is 190 VDC ~ 400 VDC and 90 VAC ~ 305 VAC.

2. OVERVIEW

The TET3000 Series AC/DC power supply is fully DSP controlled, highly efficient front-end power supply. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range and minimal derating of output power with input voltage and temperature, the TET3000 power supply maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee the best efficiency and unity power factor over a wide operating range. The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability. Status information is provided with front-panel LEDs.

In addition, the power supply can be controlled and the fan speed set via the I²C bus. The I²C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.

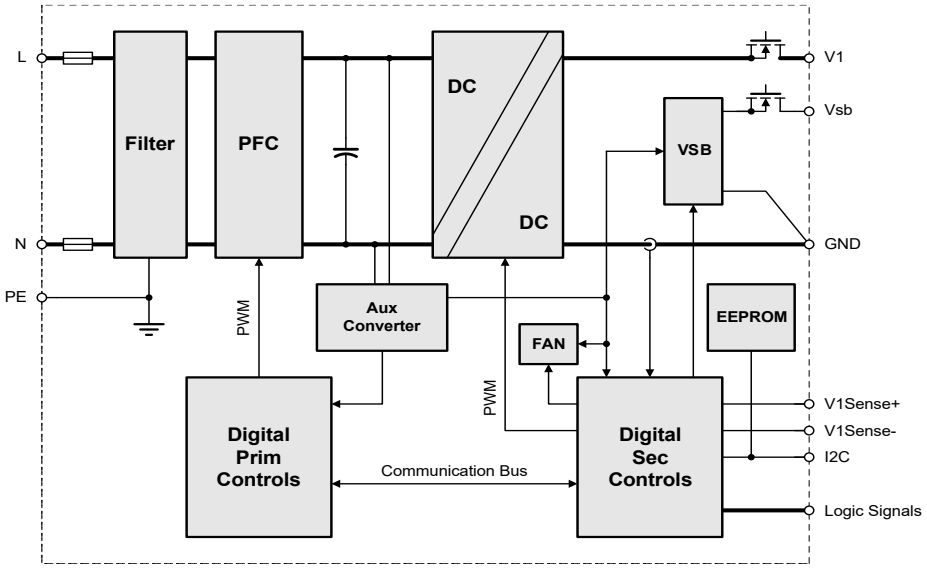


Figure 1. TET3000 Series Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi max	Maximum AC Input Voltage (Continuous)	TET3000-12-054xAC/TET3000-12xACS412 TET3000-12-054xAH/TET3000-12xAHS412			264 305	VAC
Vi max DC	Maximum DC Input Voltage (Continuous)	TET3000-12-054xAC/TET3000-12xACS412 TET3000-12-054xAH/TET3000-12xAHS412			288 400	VDC

4. INPUT SPECIFICATIONS

General Condition: T_A = -5°C … 50°C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
TET3000-12-054xAC/TET3000-12xACS412						
$V_{i\ LL\ nom}$	Low Line AC Nominal Input Voltage	Rated low line voltage	100		127	VAC
$V_{i\ LL}$	Low Line AC Input Voltage Range	Normal operating ($V_{i\ min\ LL}$ to $V_{i\ max\ LL}$)	90		140	VAC
$V_{i\ HL\ nom}$	High Line AC Nominal Input Voltage	Rated high line voltage	200		240	VAC
$V_{i\ HL}$	High Line AC Input Voltage Range	Normal operating ($V_{i\ min\ HL}$ to $V_{i\ max\ HL}$)	180		264	VAC
$V_{i\ nom\ DC}$	DC Nominal Input Voltage	Rated HVDC		240		VDC
$V_{i\ DC}$	DC Input Voltage Range	Normal operating ($V_{i\ min\ DC}$ to $V_{i\ max\ DC}$)	204		288	VDC
PARAMETER		**DESCRIPTION / CONDITION**	**MIN**	**NOM**	**MAX**	**UNIT**
TET3000-12-054xAH/TET3000-12xAHS412						
$V_{i\ LL\ nom}$	Low Line AC Nominal Input Voltage	Rated low line voltage	100		127	VAC
$V_{i\ LL}$	Low Line AC Input Voltage Range	Normal operating ($V_{i\ min\ LL}$ to $V_{i\ max\ LL}$)	90		140	VAC
$V_{i\ HL\ nom}$	High Line AC Nominal Input Voltage	Rated high line voltage	200		277	VAC
$V_{i\ HL}$	High Line AC Input Voltage Range	Normal operating ($V_{i\ min\ HL}$ to $V_{i\ max\ HL}$)	180		305	VAC
$V_{i\ nom\ DC}$	DC Nominal Input Voltage	Rated HVDC	240		380	VDC
$V_{i\ DC}$	DC Input Voltage Range	Normal operating ($V_{i\ min\ DC}$ to $V_{i\ max\ DC}$)	190		400	VDC

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PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,red}$	Derating Input Voltage Range	See Section 6.3.1	90		180	VAC
$I_{i\,max}$	Max Input Current	*90 VAC <Vi <140 VAC*		16	19	A_{rms}
		180 VAC <Vi <305 VAC		16	18.5	
		190 VAC <Vi <400 VDC		13.8	17.5	
$I_{i\,p}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, T_{PTC} = 25°C, exclude effects of X-caps			50	A_p
F_i	Input Frequency		47	50/60	63	Hz
PF	Power Factor	$V_{i\,nom}$, 50 Hz, > 0.2 $I_{i\,nom}$	0.95			W/VA
$V_{i\,on}$	Turn-on Input Voltage[1]	Ramping up	87	88.5	90	VAC
			185	187.5	190	VDC
$V_{i\,off}$	Turn-off Input Voltage	Ramping down	82	84.5	87	VAC
			180	182.5	185	VDC
η	Efficiency without Fan at 230VAC input (min Titanium levels)	$V_{i\,nom}$, 0.1·$I_{x\,nom}$, T_A = 25°C	90	93.8		%
		$V_{i\,nom}$, 0.2·$I_{x\,nom}$, T_A = 25°C	94	95.5		%
		$V_{i\,nom}$, 0.5·$I_{x\,nom}$, T_A = 25°C	96	96.2		%
		$V_{i\,nom}$, $I_{x\,nom}$, T_A = 25°C	91	94.1		%
$T_{V1\,hold}$	Hold-up Time V_i	After last AC zero point to $V_1 \geq$ 11.4 V, V_{SB} within regulation, V_i = 230 VAC, 3.0kW	10			ms
$T_{V1\,hold}$	Hold-up Time V_i	After last AC zero point to $V_1 \geq$ 11.4 V, V_{SB} within regulation, V_i = 230 VAC, 1.5kW	20			ms
$T_{VSB\,hold}$	Hold-up Time V_{SB}	All hold-up conditions	40			ms

4.1 INPUT FUSE

Fast acting 25A input fuses (5.0 × 20 mm) in series with both the L and N line inside the power supply protect against severe defects. The fuse is not accessible from the outside and is therefore not serviceable parts.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only *5.4* µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through a PTC which will limit the inrush current.

NOTE: Do not repeat plug-in/out operations within a short time, or else the internal in-rush current limiting device (PTC) may not cool sufficiently and may result in the inability to start the PSU.

4.3 INPUT UNDER-VOLTAGE

If the RMS value of input voltage (either AC or DC) stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform. At DC input voltage the PFC is still in operation, but the input current will be DC in this case.

[1] The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges.

4.5 EFFICIENCY

High efficiency is achieved by using state-of-the-art silicon and silicon carbide power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

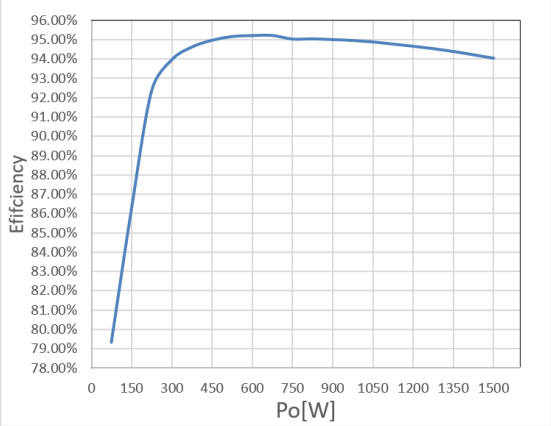


Figure 2. Typical Efficiency vs. Load Current at 115VAC Input

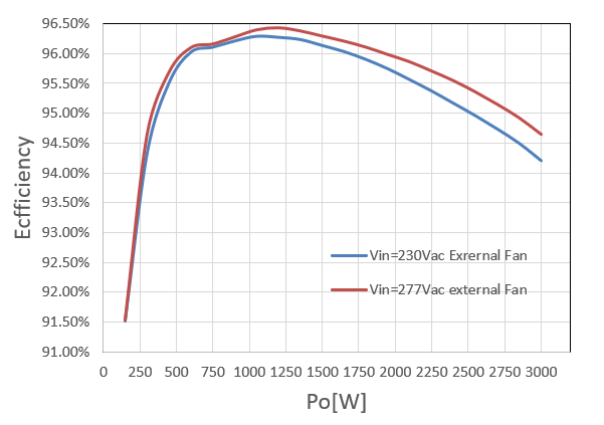


Figure 3. Typical Efficiency vs. Load Current at 230VAC/277VAC Input

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5. OUTPUT SPECIFICATIONS

General Condition: Ta = -5… 50°C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_{amb} = 25 °C		12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy		-0.5		+0.5	% $V_{1\ nom}$
$dV_{1\ Load}$	Load Regulation	V_i = $V_{i\ nom}$, 0 to 100 % $I_{1\ nom}$		150		mV
$dV_{1\ Line}$	Line Regulation	V_i = $V_{i\ min}$... $V_{i\ max}$		50		mV
$dV_{1\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$ $V_{i\ min\ DC}$ to $V_{i\ max\ DC}$	0		3000	W
	Refer to Figure 7 for derating	$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$	0		1500	W
$I_{1\ nom}$	Nominal Output Current	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$ $V_{i\ min\ DC}$ to $V_{i\ max\ DC}$	0		250	ADC
		$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$	0		125	ADC
$v_{1\ pp}$	Output Ripple Voltage	$V_{1\ nom}$, 0 to 100% $I_{1\ nom}$, 20MHz Bandwidth			150	mVpp
dI_{share}	Current Sharing	Deviation from I_1…I_N> 20A	-5		5	A
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ nom}$		8		VDC
dV_{dyn}	Dynamic Load Regulation	ΔI_1 = 40% $I_{1\ nom}$, I_1 = 5% … 100% $I_{1\ nom}$, dI_1/dt = 1A/µs	-5		+5	% $V_{1\ nom}$
T_{rec}	Recovery Time	Recovery within 1% of $V_{1\ nom}$		2		ms
$t_{V1\ rise}$	Rise Time	V_1 = 10…90% $V_{1\ nom}$			30	ms
$t_{VIN\ V1}$	Start-up Time from AC	V_1 = 90% $V_{1\ nom}$			3000	ms
$t_{V1\ over\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{1\ nom}$			0.6	V
C_{Load}	Capacitive Loading				30	mF
$dV_{1\ sense}$	Remote Sense	Compensation for cable drop, 0-100% $I_{1\ nom}$			250	mV

12 V_{SB} Standby Output						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C		12.0		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-0.5		+0.5	% $V_{SB\ nom}$
dV_{SB} load	Load Regulation	0 to 100% $I_{SB\ nom}$		100		mV
dV_{SB} line	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$		20		mV
$dV_{SB\ tot}$	Line and Load Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	% $V_{SB\ nom}$
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		36		W
$I_{SB\ nom}$	Nominal Output Current	$V_{i\ min}$ to $V_{i\ max}$		3		A
$V_{SB\ pp}$	Output Ripple Voltage	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, 20MHz Bandwidth			120	mVpp
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5% … 100% $I_{SB\ nom}$, dI_{SB}/dt = 1 A/µs,	-0.6		0.6	V
T_{rec}	Recovery Time	Recovery within 1% of $V_{1\ nom}$		2		ms
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$			30	ms
$t_{VIN\ VSB}$	Start-up Time from AC	V_{SB} = 90% $V_{SB\ nom}$			2700	ms
$t_{VSB\ over\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{SB\ nom}$			0.6	V
C_{Load}	Capacitive Loading				1000	µF

5.0V$_{SB}$ Standby Output						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C		5.0		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-1		+1	% $V_{SB\ nom}$
dV_{SB} load	Load Regulation	0 to 100% $I_{SB\ nom}$		100		mV
dV_{SB} line	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$		20		mV
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	% $V_{SB\ nom}$
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		15		W
$I_{SB\ nom}$	Nominal Output Current	$V_{i\ min}$ to $V_{i\ max}$		3		A
$V_{SB\ pp}$	Output Ripple Voltage	$V_{i\ min}$ to $V_{i\ max}$, $I_{SB\ nom}$, 20 MHz BW (See Section 5.1)			75	mVpp
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5% … 100% $I_{SB\ nom}$, dI_{SB}/dt = 1 A/µs,	-5		5	%V_{SBnom}
T_{rec}	Recovery Time	Recovery within 1% of $V_{1\ nom}$		2		ms
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$			30	ms
$t_{VIN\ VSB}$	Start-up Time from AC	V_{SB} = 90% $V_{SB\ nom}$			2700	ms
$t_{VSB\ over\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{SB\ nom}$			0.25	V
C_{Load}	Capacitive Loading				1000	µF

5.1 OUTPUT VOLTAGE RIPPLE

The test set-up shall be following *Figure 4.*

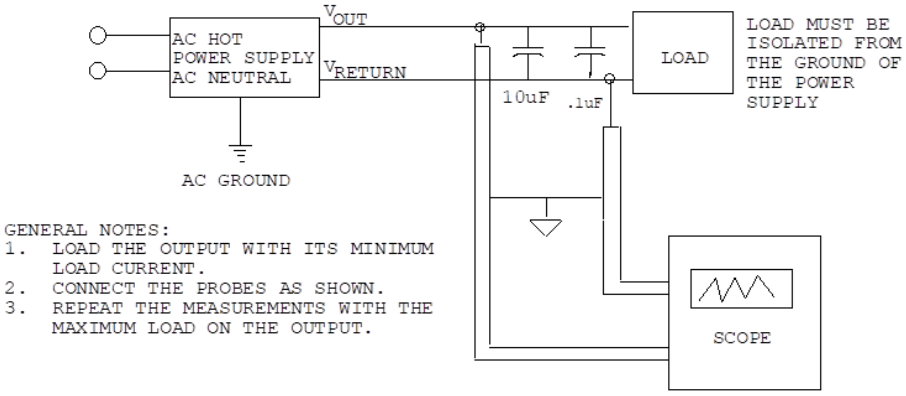


Figure 4. Output ripple test setup

NOTES: Load must be isolated from the safety ground to *Figure 4.*

When performing this test, the probe clips and capacitors should be located close to the load.

5.2 OUTPUT GROUND /CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop, a low impedance ground plane should be used as shown in Figure 5. Alternatively, separated ground signals can be used as sown in Figure 6.

NOTE:

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Within the power supply the output GND pins are not connected to the Chassis, which in turn is not connected to the Protective Earth terminal on the AC inlet. Therefore, it is possible to set the potential of the output return (GND) to any other than Protective Earth potential.

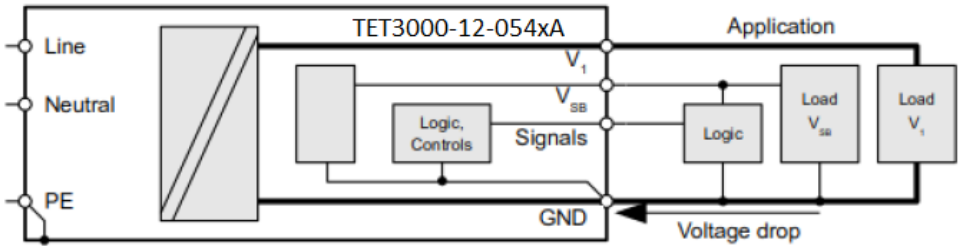


Figure 5. Common low impedance ground plane

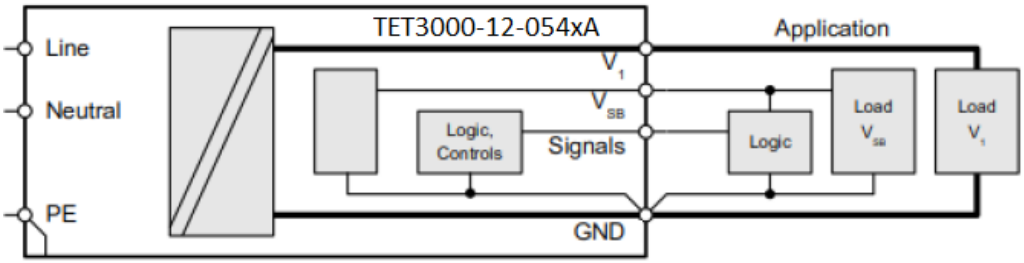


Figure 6. Separated power and signal ground.

6. PROTECTION SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuse (L+N)	Not user accessible, Fast Acting		25		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type	13.0		14.5	VDC
$V_{SB\ OV}$	OV Threshold V_{SB}	Over Voltage V_{sb} Protection, Automatic recovery type	105		120	% V_{SB}
$V_{1\ UV}$	UV Threshold V_1	Under Voltage V_1 Protection, Latch-off Type		11.2		VDC
$V_{VSB\ UV}$	UV Threshold V_{SB}	Under Voltage V_{sb} Protection, Automatic recovery type		90		%V_{SB}
$I_{V1\ lim}$	Over Current Limitation V_1	Over Current Limitation. Five "hiccup" auto recovery cycles, follow by a latched shutdown $V_{in} \geq$ 180 VAC/190 HVDC, $T_a \leq$ 50°C 180 VAC > $V_{in} \geq$ 90 VAC, $T_a \leq$ 50°C	 252 130		 288 144	A
$I_{VSB\ lim}$	Over Current Limitation V_{SB}	Over Current Limitation, Automatic recovery Type $T_a \leq$ 50°C for V_{SB}	3.1		4.5	A
T_{SD}	Over Temperature on Heat Sinks	Automatic shut-down		115		°C

6.1 OUTPUT OVERVOLTAGE PROTECTION

The TET3000 Series front-ends provide a fixed threshold overvoltage (OV) protection for both main and standby output. Once the 12V main output OV condition has been triggered, the main output will shut down and latch the fault condition. The standby output V_{SB} will turn off the whole power supply if standby output V_{SB} over-voltage protection has been triggered. The latch for main output and standby output V_{SB} can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.

6.2 OUTPUT UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_L pin signal if the output voltage exceeds ±5% of its nominal voltage. The main output will latch off if the main output voltage when V1 falls below 11.2 V (typically in an overload condition), the latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. If the standby output leaves its regulation bandwidth for more than 10ms then the main output is disabled to protect the system.

6.3 CURRENT LIMITATION

6.3.1 MAIN OUTPUT

When the main output runs in current limitation mode its output will turn OFF below 2V but will retry to recover every 1s interval. If current limitation mode is still present after the unit retry, after five "hiccup" auto recovery cycles, followed by a latched shutdown. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. A failure on the main output does not shut down the standby output.

The output power derating of V1 refers to Figure 7. The main output power of high line and low line will decrease if the ambient (inlet) temperature increases beyond 50°C.

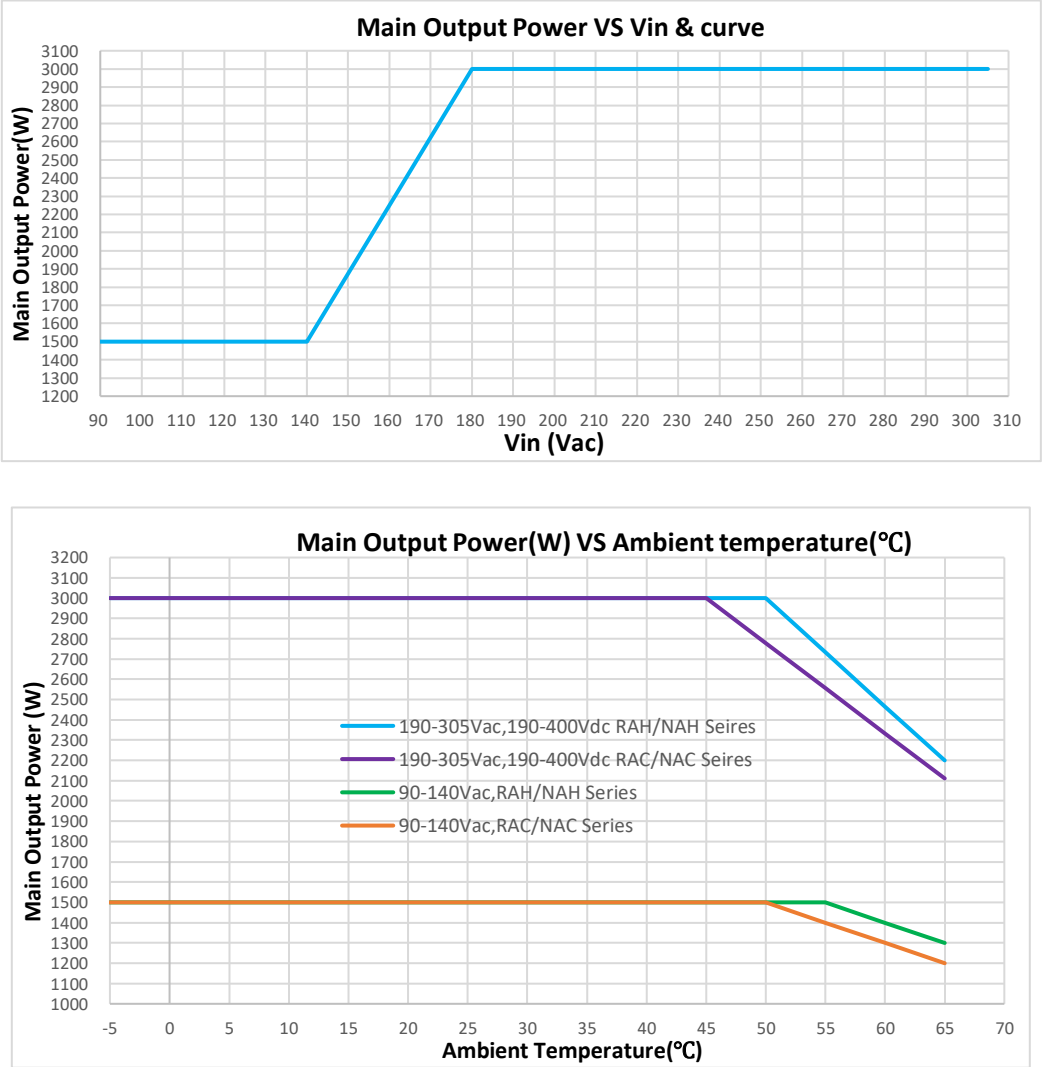


Figure 7. Power derating curve with Vin and Ambient Temperature

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Note:

1. The application of power supply should also refer to installation instructions document.

2. The power supply has no limitation on its output current/power in respect of meeting the operating conditions shown by the derating limits shown above. It is the responsibility of the end user to ensure operating conditions are maintained within their safety agency certification limits to assure safe and reliable operation.

6.3.2 STANDBY OUTPUT

On the standby output, a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds $I_{VSB\ lim}$. After an off-time of 1 s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly try to restart with 1s intervals. A failure on the Standby output will shut down both Main and Standby outputs.

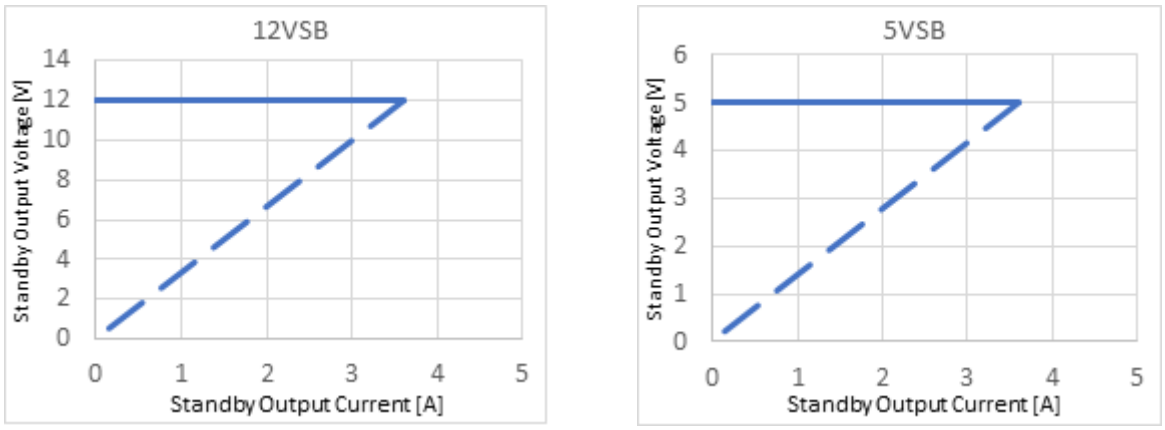


Figure 8. Current Limitation on 12VSB/5VSB

7. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to the Power Management Bus Communication Manual.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input RMS Voltage	$V_{i\ min} \le V_i \le V_{i\ max}$	-2		+2	%
$I_{i\ mon}$	Input RMS Current	$1\ A_{rms} \le I_i \le 7\ A_{rms}$ $I_i > 7\ A_{rms}$	-0.35 -5		+0.35 +5	A_{rms} %
$P_{i\ mon}$	True Input Power	100 W ≤ P_i ≤ 700 W P_i > 700 W	-35 -5		+35 +5	W %
$V_{1\ mon}$	V_1 Voltage		-1		+1	%
$I_{1\ mon}$	V_1 Current	I1 > 25 A	-5		+5	A
$P_{o\ nom}$	Output Power	120W ≤ P_o ≤ 700 W Po > 700 W	-42 -6		42 +6	W %
$V_{SB\ mon}$	Standby Voltage		-2		+2	%
$I_{SB\ mon}$	Standby Current	$I_{SB} \le I_{SB\ nom}$	-0.2		+0.2	A
T_{amb}	Ambient Temperature	-5℃ ≤ T_{amb} ≤ 50℃	-3		+3	℃

Power Management Bus Sensors Accuracy

8. SIGNAL & CONTROL SPECIFICATIONS

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
PSON_L						
V_{IL}	Input Low Level Voltage		-0.2		0.8	V
V_{IH}	Input High Level Voltage		2.4		3.5	V
$I_{IL, H}$	Maximum Input Sink or Source Current		0		1	mA
R_{puPSON_L}	Internal Pull Up Resistor on PSON_L			10		kΩ
PWOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 50 uA	2.6		3.5	V
R_{puPWOK_H}	Internal Pull Up Resistor on PWOK_H			1		kΩ
ACOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 50 µA	2.6		3.5	V
R_{puACOK_H}	Internal Pull Up Resistor on ACOK_H			1		kΩ
SMB_ALERT_L Output						
V_{ext}	Maximum External Pull Up Voltage				12	V
V_{OL}	Output Low Level Voltage	I_{source} < 4 mA	0		0.4	V
I_{OH}	Maximum High-Level Leakage Current				10	µA
$R_{puSMB_ALERT_L}$	Internal Pull Up Resistor on SMB_ALERT_L			NA		kΩ
ISHARE IO						
V_{SHARE}	Current Share Bus Voltage	*At* I_1 = 250 A		8.0		V

8.2 SENSE INPUT

The main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.3 CURRENT SHARE

The TET3000 front-ends have an active current share scheme implemented for V_1. All the ISHARE current share pins need to be interconnected to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output going down (or up) in such cases.

The current share function uses an analog bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other suppliers will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

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8.4 PRESENT_L OUTPUT

The PRESENT_L pin is wired to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low-level voltage if power supply is seated.

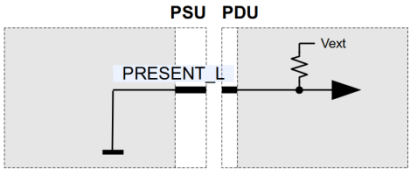


Figure 9. PRESENT_L connection

8.5 PSON_L INPUT

The PSON_L is an internal pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PSON_L can be either controlled by an open collector device or by a voltage source. The timing diagram is given in *Figure 10* and the parameters in *Table 1*.

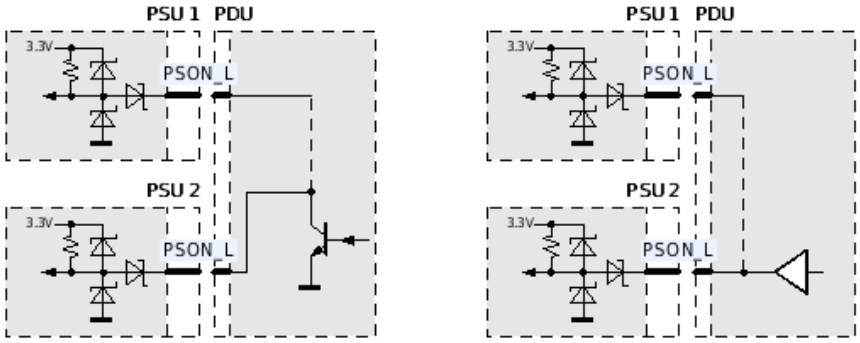


Figure 10. PSON_L connection

8.6 PWOK_H SIGNAL

The PWOK_H is an internal pull-up to 3.3V indicating whether both V_{SB} and V_1 outputs are within regulation. When any output voltage falls below regulation limits or when AC power has been removed for a sufficiently long time so that power supply operation is no longer guaranteed, PWOK_H will be de-asserted to a LOW state**.** The timing diagram is shown in *Figure 11* and referenced in *Table 1*.

8.7 ACOK_H OUTPUT

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON_L signal is pulled low, and the input voltage is within range. The ACOK_H signal is active-high. The timing diagram is shown in *Figure 11* and referenced in *Table 1.*

8.8 SMB_ALERT_L OUTPUT

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical signal of the Shutdown events. It is asserted (pulled Low) at Shutdown events such as reaching temperature shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits.

8.9 TIMING REQIREMENTS

These are the timing requirements for the power supply operation. All outputs must rise monotonically.

OPERATING CONDITION		MIN	MAX	UNIT
TVout_rise	Output voltage rise time for Vout		30	ms
TVsb_rise	Output voltage rise time for Vsb		30	ms
TVsb_on_delay	Delay from Vin being applied to Vsb being within regulation		2700	ms
TVout_on_delay	Delay from Vin being applied to Vout being within regulation		3000	ms
Tacok_on	Input voltage to ACOK_H signal delay time		2000	ms
Tacok_de-asserted	Delay from Vin drop being 0V to de-aseertion of ACOK		5	ms
TVsb_Vout	Delay from Vsb being in regulation to Vout being in regulation at Vin turn on	50	500	ms
TVout_holdup	Time of Vout output voltage stay within regulation after loss of Vin	10		ms
TVsb_holdup	Time of Vsb output voltage stays within regulation after loss of Vin	40		ms
Tpson_on_delay	Delay from PSON active to output voltages within regulation limits	100	400	ms
Tpson_off_delay	Delay from PSON de-asserted to power supply turning off	0	5	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted	100	400	ms
Tpwok_holdup	Delay from loss of Vin to de-assertion of PWOK	9		ms
Tpwok_off	Delay from PWOK de-asserted to output voltages dropping out of regulation limits	1		ms

Table 1. Signal Timings

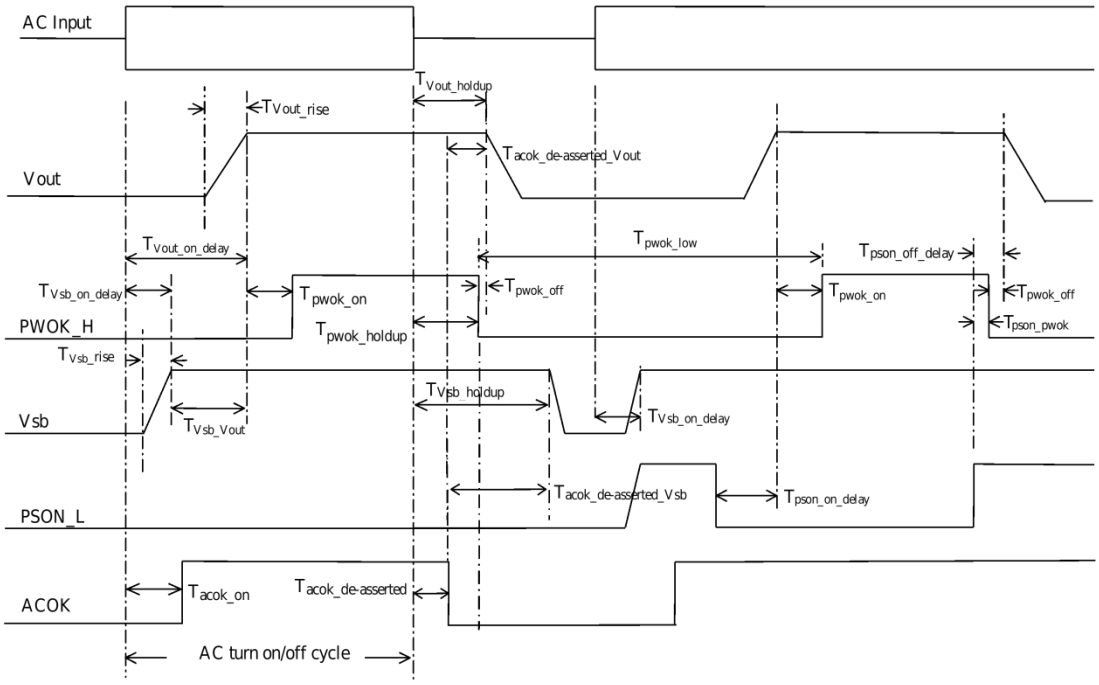


Figure 11. Timing Diagram

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8.10 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and yellow and indicates AC and DC power presence and warning or fault conditions. The LED are visible on the power supply's exterior face. The LED location meets ESD Requirements. *Table 2* lists the different LED status.

POWER SUPPLY CONDITION	LED STATUS
12V main on and in voltage regulation band (Active mode)	Solid Green
12V main off (Standby mode)	Green blinking (1Hz)
No AC input power to any of the system power supplies	OFF
No AC input power, but other PSU in the system operating	Solid Yellow
Warning event (Output OCW/ OTW/ Fan Warning)	Yellow blinking (1Hz)
Fault event (Input OVP, Output OVP/UVP, OCP, OTP, Fan Fail, Other internal fault)	Solid Yellow
FW update	Green blinking (2Hz)

Table 2. LED Status

8.11 I²C BUS

The TET3000 Series supplies are communication Slave devices only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing are defined in *Table 3* further characterized through.

- SCL/SDA pull-up resistor is 3kΩ in PSU side
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms.
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions.

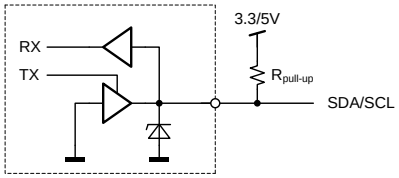


Figure 12. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 or VSB output (provided e.g., by the redundant unit).

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
V_{iL}	Input low voltage		-0.5		1.0	V
V_{iH}	Input high voltage		2.3		5.5	V
V_{hys}	Input hysteresis		0.15			V
V_{oL}	Output low voltage	3 mA sink current	0		0.4	V
t_r	Rise time for SDA and SCL		20+0.1Cb[2]		300	Ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < Cb[2] < 400 pF	20+0.1Cb[2]		250	Ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10		10	µA
C_i	Internal Capacitance for each SCL/SDA				0	pF
f_{SCL}	SCL clock frequency		0		100	kHz

[2] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

R_{pu}	External pull-up resistor	f_{SCL} ≤ 100 kHz			1000 ns / Cb	Ω
R_{pu_int}	Internal pull-up resistor			3k		Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0			µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7			µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0			µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7			µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0		3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250			ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0			µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5			ms

Table 3. I²C / SMBus Specification

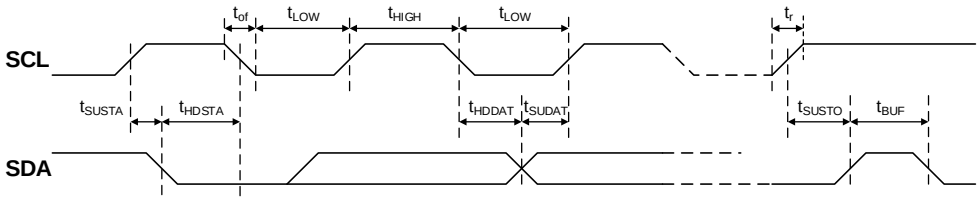


Figure 13. I²C / SMBus Timing

8.12 ADDRESS / PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the address by connecting a resistor to V1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

NOTE:

- If the APS pin is left open, the supply will operate with the Power Management Bus protocol at controller / EEPROM addresses 0xBE / 0xAE.

- The APS pin is only read at start-up of the power supply. Therefore, it is not possible to change address dynamically.

R_{APS} (Ω) [3]	Protocol	I²C Address [4]	
		Controller	EEPROM
820		0xB0	0xA0
2700	Power	0xB2	0xA2
5600	Management Bus	0xB4	0xA4
8200		0xB6	0xA6
15000		0xB8	0xA8
27000	Power	0xBA	0xAA
56000	Management Bus	0xBC	0xAC
180000		0xBE	0xAE

Table 4. Address and Protocol Encoding

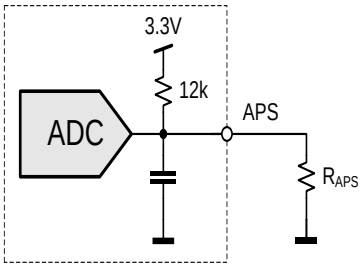


Figure 14. I²C address setting

3 E12 resistor values, use max 5% resistors, see also *Table 4*

4 The LSB of the address byte is the R/W bit

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8.13 DSP CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see *Figure 15*).

An I²C driver device assures logic level shifting (3.3/5V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I²C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, firstly the write protection needs to be disabled by sending the appropriate command to the DSP. By default, the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

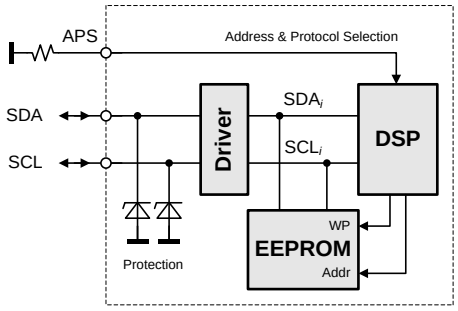


Figure 15. I²C Bus to DPS and EEPROM

8.14 EEPROM PROTOCOL

EEPROM device used is the AT24C02C or compatible alternative.

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

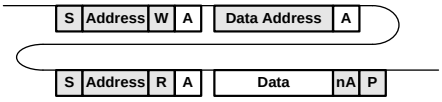
WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



8.15 POWER MANAGEMENT BUS PROTOCOL

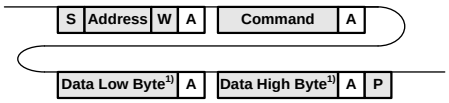
The Power Management Bus (Power Management Bus) is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The TET3000 Serie supplies supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

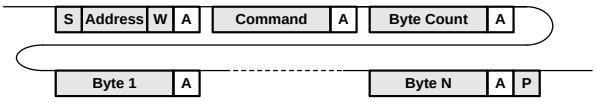
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



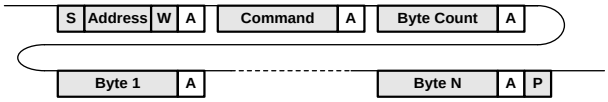
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes.

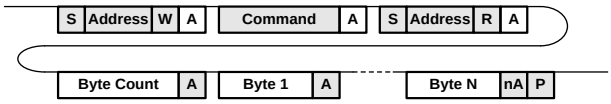


READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes.



8.16 POWER SUPPLY DIAGNOSTIC BLACK BOX

The power supply shall save the latest data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible via the Power Management Bus interface with an external source providing power to the 12V main output bus or standby by 12VSB output bus.
Critical Events to trigger an update to the Event Recorder includes.

- Output OVP
- Output OCP
- Input OV/UV Fault
- Fan fault
- OTP
- Other faults caused output shutdown.

Refer to BCA.20365_TET3000 series Power Manage Communication Protocol Application Note for further information about the Power Management Bus commands to support this function.

9. TEMPERATURE AND FAN CONTROL

To achieve the best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The TET3000 series supply has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.



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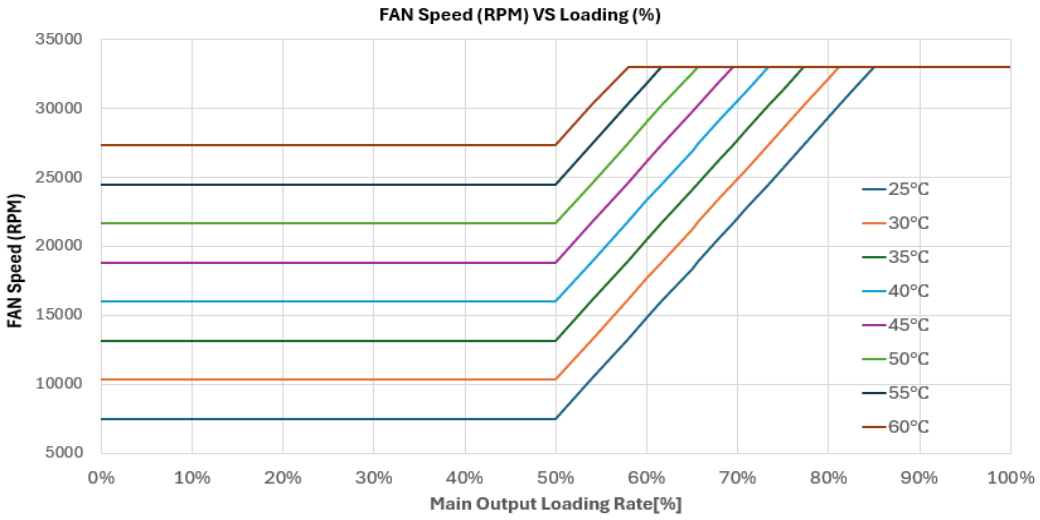


Figure 16. Fan speed vs Main output Load

10. ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV	A
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation	A
Electrical Fast Transients/Burst	IEC / EN 61000-4-4, Level 3 AC port ±2 kV	A
Surge	IEC / EN 61000-4-5, Level 3 Line to PE, ±2 kV 2R0 Line to line, ±2 kV 2R0	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms	A
Voltage Dips and Interruptions	IEC 61000-4-11 1. Vi 230Vac/100Vac, 100% Load, Phase 0 °, Dip 100%, Duration 10ms 2. Vi 230Vac, 85% Load, Phase 0 °, Dip 30%, Duration 500ms 3. Vi 100Vac, 80% Load, Phase 0 °, Dip 30%, Duration 500ms 4. Vi 230Vac/100Vac, 100% Load, Phase 0 °, Dip 100%, Duration 5000ms	 A A A B

10.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN55032/ CISPR 22: 0.15 … 30 MHz, QP and AVG	Class A
Radiated Emission	EN55032/ CISPR 22: 30 MHz … 1 GHz, QP	Class A
Harmonic Emissions	IEC61000-3-2, Vin = 230VAC/ 50 Hz, 100% Load	Class A
AC Flicker	IEC61000-3-3, Vin = 230 VAC / 50 Hz, 100% Load	Pass

11. SAFETY APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 62368-1, and UL/CSA 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Agency Approvals	Approved to the latest edition of the following standards: UL/CSA 62368-1 IEC/EN 62368-1 GB 4943.1, GB/T 9254.1, GB 17625.1 CNS15598-1, CNS15936		Approved		
Isolation Strength	Input (L/N) to case (PE) Input (L/N) to output Output to case (PE)		Basic Reinforced Functional		
Electrical Strength Test	Input to case Input to output		2.5 5.0		kVdc

12. ENVIRONMENTAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	$V_{i\,min}$ to $V_{i\,max}$, $I_{o\,nom}$, $I_{SB\,nom}$ at 3000 m Altitude	-5		+40	°C
		$V_{i\,min}$ to $V_{i\,max}$, $I_{o\,nom}$, $I_{SB\,nom}$ at 2000 m Altitude	-5		+50	°C
T_{Aext}	Extended Temp. Range	Derating output	+50		+65	°C
T_S	Storage Temperature	Non-operational	-40		+70	°C
N_a	Audible Noise	V_i nom, 50% Io nom, TA = 25°C measured at bystander position		45		dBA
	Operating humidity	Non-condensing	5		95	%
	Storage humidity	Non-condensing	5		95	%
	MTBF	Per Telcordia SR-332 issue 4 @ 40°C & 230 VAC	650 K			hrs.

13. MECHANICAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions (W x H x L)			54.5 x 40.0 x 321.5 2.13 x 1.57 x 12.66		mm in
M	Weight			1.3		kg
	Flammability	NEBS GR-63		V-0		

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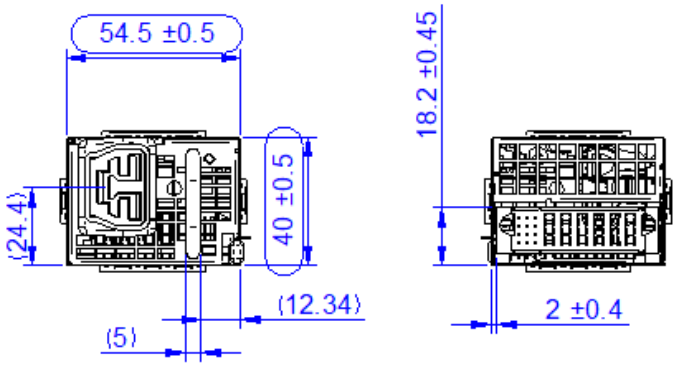


Figure 17. Front and back view

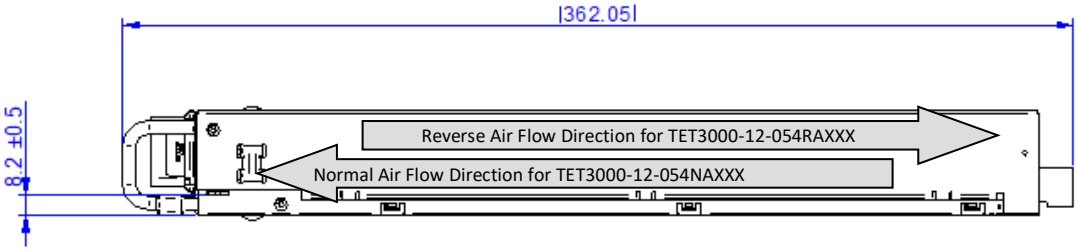


Figure 18. Side view 1

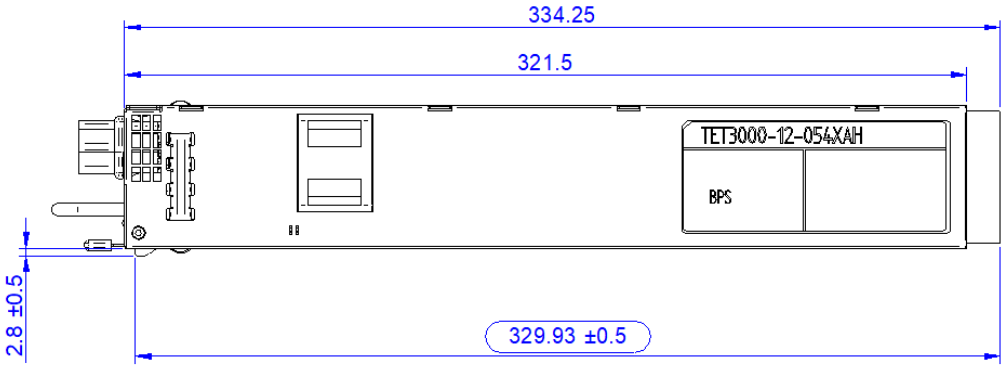


Figure 19. Top View

14. CONNECTIONS

14.1 AC INPUT CONNECTOR

TET3000-12-054xAC / TET3000-12xAC	TET3000-12-054xAH / TET3000-12xAH
IEC320 C22 type	ANDERSON POWER PRODUCTS 2006G1-BK

14.2 DC OUTPUT CONNECTOR

POWER SUPPLY CONNECTOR	MATING CONNECTOR
Amphenol 10106262-6003006LF or equivalent	**Amphenol** 10106264-6003003LF

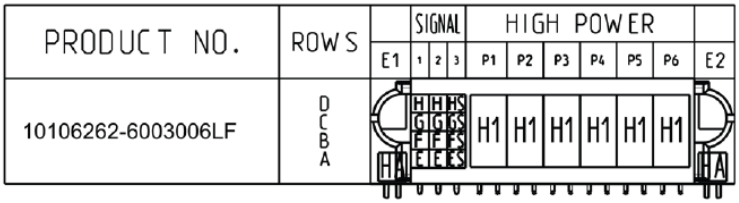
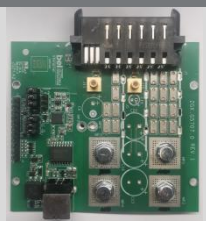


Figure 20. Power Supply Connector pinout

PIN	NAME	DESCRIPTION
Output		
P4, P5, P6	V1	+12 VDC main output
P1, P2, P3	V1&VSB_RETURN	+12 VDC / VSB Output Return
Control Pins		
A1	PRESENT_L	Power supply present pin: Active-low
B1	VSB	Standby Output
C1	ACOK_H	AC input OK signal: Active-high
D1	ISHARE	Current Share Bus
A2	V1_SENSE_R	Main output negative sense
B2	V1_SENSE	Main output positive sense
C2	PWOK_H	Power OK signal output (lagging pin): Active-high
D2	APS	I²C address (select by a pull-down resistor)
A3	SDA	I²C data signal line
B3	SCL	I²C clock signal line
C3	PSON_L	Power supply remote on input: Active-low
D3	SMB_ALERT_L	SMB Alert signal output: Active-low

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15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	Evaluation Board Connector board to operate TET3000-12-054xA. Includes an onboard USB to I²C converter (use I²C Utility as desktop software)	YTM.G5701.0	Bel Power Solutions

16. REVISION HISTORY

DATE	REVISION	CHANGE	PREPARED BY	APPROVED BY	ECO NO.
2023/03/15	1	First draft	Eisen Xu	Jemrry Zhang	
2025/07/08	A	Release to Version A	Eisen Xu	Jemrry Zhang	

For more information on these products consult: powersupport@belf.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.