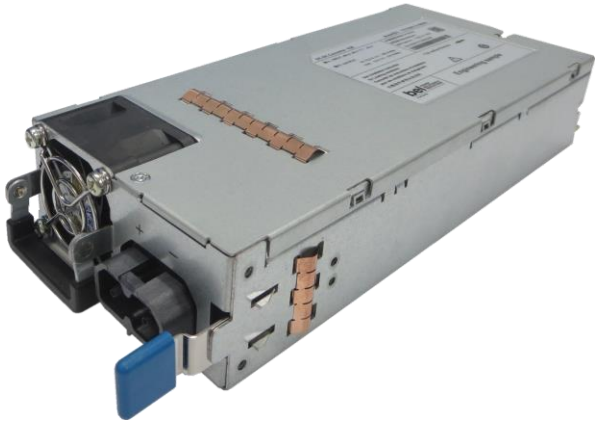
TET2200-12-086xD Series

DC-DC Front-End Power Supply

The TET2200-12-086xD is a 2200 Watt DC to DC power supply that converts -40 to -72 VDC voltage into an insulated main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The TET2200-12-086xD utilizes full digital control architecture for greater efficiency, control, and functionality.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



RoHS Compliant

Key Features & Benefits

- Wide input voltage range: -40 to -72 VDC
- 2200 W continuous output power capability
- Always-on 12 VSB / 3.5 A standby output
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- High power density design: 54.1 W/in^3
- Small form factor: 86.3 x 39.3 x 196.5 mm (3.4 x 1.5 x 7.7 in)
- Power Management Bus communication interface for control, programming and monitoring
- Status LED with fault signaling
- Black Box recorder available

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

Please read our datasheet & drawing disclaimer here.

1. ORDERING INFORMATION

TET	2200	-	12	-	086	x	D	x
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**	**Specific code [3]**
TET Front-Ends	2200 W		12 V		86.3 mm	N: Normal [1] R: Reverse [2]	D: DC	x = Blank x = S+3 digits

1 "N" Normal Airflow (NAF) from Output connector to Input DC connector
2 "R" Reverse Airflow (RAF) from Input DC connector to Output connector
3 Contact factory for availability of Specific code, e.g. Ordering PN as TET2200-12-086NDS507

2. OVERVIEW

The TET2200-12-086xD DC/DC power supply is a DSP controlled, highly efficient front-end power supply. It incorporates state of the art technology and uses an interleaved forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency.
With a wide input DC voltage range the TET2200-12-086xD maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.
An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.
The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.
Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.
Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

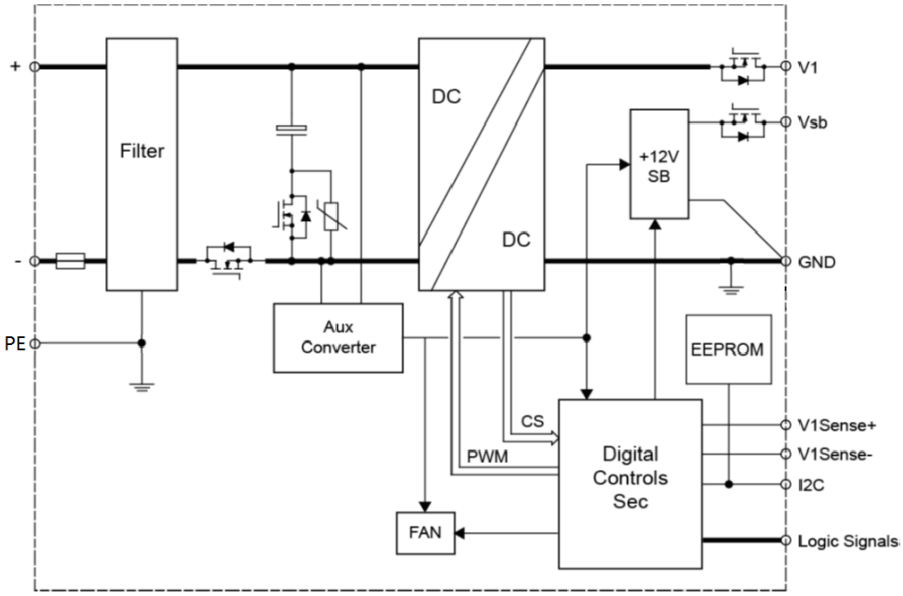


Figure 1. TET2200-12-086xD Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
Vi maxc	Maximum Input	Continuous		-78	VDC

4. INPUT

General Condition: T_A = 0… 55 °C, unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi start	Minimum operating input voltage	Stand-by output available, DSP running	-30			VDC
Vi nom	Nominal input voltage		-48		-60	VDC
Vi	Input voltage	Normal operation (from Vi min to Vi max)	-40		-72	VDC
Ii	Input current	Vi > Vi min			64	A
Ii pk	Inrush current limitation	From Vi min to Vi max, T_A = 25°C, cold start			50	A
Vi_{VSB_on}	Turn-on standby input voltage	Ramping up	-28		-30	VDC
Vi_{VSB_off}	Turn-off standby input voltage	Ramping down	-19		-21	VDC
Vi_{V1_on}	Turn-on V1 input voltage	Ramping up	-38		-40	VDC
Vi_{V1_off}	Turn-off V1 input voltage	Ramping down	-37		-39	VDC
η	Efficiency [1]	Vi = -48 VDC; -60 VDC; 10% load		82		%
		Vi = -48 VDC; -60 VDC; 20% load		90		%
		Vi = -48 VDC; -60 VDC; 50% load		94		%
		Vi = -48 VDC; -60 VDC; 100% load		91		%

4.1 INPUT FUSE

A fast-acting 80 A (or equivalent) input fuse in the negative voltage path inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

4.3 INPUT UNDER-VOLTAGE

If the input voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 EFFICIENCY

High efficiency (see *Figure 2*) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

[1] Efficiency measured without fan power per EPA server guidelines.

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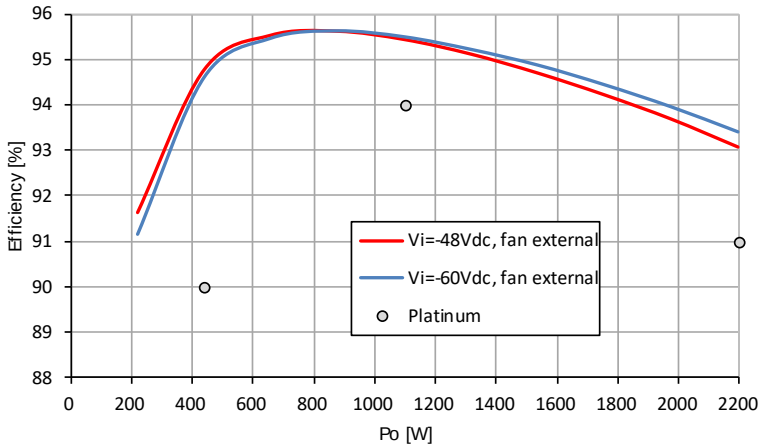

Figure 2. Efficiency vs. Load current (ratio metric loading)

4.5 DC LINE TRANSIENT TEST

MINUS 72 VDC LINE TRANSIENT TEST

A standard line voltage momentary transient test is shown below. This test simulates a momentary voltage overshoot. This should not affect the operation of the PSU; the output voltage should remain in regulation. This test shall be conducted every 10 secs for 30 min (180 times total).

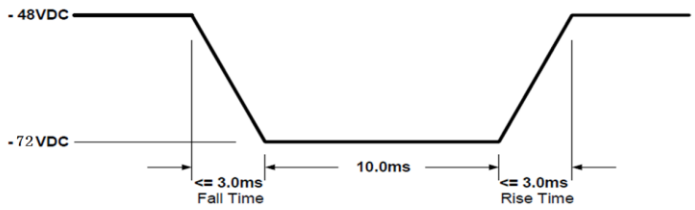

Figure 3. Minus 72 VDC Line Transient Test

0 V LINE TRANSIENT TEST

A standard line voltage momentary blackout test is shown below. This test simulates a momentary switch throw off-on, see graph below. The power supply should restart, not latch. This test shall be conducted 3 times in 10 min intervals.
Practically a blackout of any duration should not damage the power supply in any way and not cause a latch off condition.

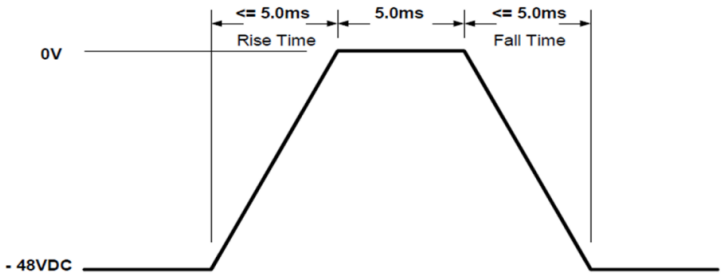

Figure 4. 0 V Line Transient Test

5. OUTPUT

General condition: T_A = 0…55 °C, V_i = -48 VDC unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.2		VDC
$V_{1\ set}$	Output Set Point Accuracy		-1		+1	%$V_{1\ nom}$
$dV1$ load	Load Regulation	0 to 100% $I_{1\ nom}$			240	mV
$dV1$ line	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$			120	mV
$dV_{1\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$	-5		+5	%$V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		2200		W
$I_{1\ peak}$	Peak Output Loading	$V_{i\ min}$ to $V_{i\ max}$ *(max 20 s)*			205	ADC
$I_{1\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$	0		183	ADC
$V_{1\ pp}$	Output Ripple Voltage [1]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, 20MHz Bandwidth			150	mVpp
$dI_{1\ share}$	Current Sharing	Difference between individual I_1, 0…4 power supplies in parallel, $I_{1\ total}$ / N > 10% $I_{1\ nom}$	-5		+5	A
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ nom}$		8		VDC
$dV_{1\ dyn}$	Dynamic Load Regulation	Test frequency between 50Hz and 5KHz at duty cycles from 10% to 90%, ΔI1 = 60% $I_{1\ nom}$, I1 = 6A … 100% $I_{1\ nom}$, dI1/dt = 0.25A/µs, 2000µF capacitive loading	11.48		12.92	VDC
t_{rec}	Recovery Time	recovery within 1% of $V_{1\ nom}$		2		ms
$t_{V1\ rise}$	Output Voltage Rise Time	V_1 = 10…90% $V_{1\ nom}$, C_{ext} < 10 mF	1		70	ms
$t_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{1\ nom}$			0.6	V
$dV_{1\ sense}$	Remote Sense	Compensation for cable drop, 0 to 100% $I_{1\ nom}$			0.25	V
$C_{V1\ load}$	Capacitive Loading [2]				22	mF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_A = 25°C		12.2		VDC
$V_{SB\ set}$	Output Set point Accuracy		-1		+1	%V_{SBnom}
dV_{SB} load	Load Regulation	0 to 100% $I_{SB\ nom}$			480	mV
dV_{SB} line	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$			120	mV
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$	-5		+5	%V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		42		W
$I_{SB\ peak}$	Peak Output Loading	$V_{i\ min}$ to $V_{i\ max}$			4	ADC
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$	0		3.5	ADC
$V_{SB\ pp}$	Output Ripple Voltage [1]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, 20 MHz bandwidth			120	mVpp
$dV_{SB\ dyn}$	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 0 … 100% $I_{SB\ nom}$, dI_{SB}/dt = 0.25 A/µs, recovery within 1% of $V_{SB\ nom}$	11.59		12.81	VDC
t_{rec}	Recovery Time			2		ms
$t_{VSB\ rise}$	Output Voltage Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$,	2		20	ms
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{SB\ nom}$			0.6	V
$C_{VSB\ load}$	Capacitive Loading [2]				3100	µF

[1] Ripple noise and dynamic load measured with a 10 µF low ESR capacitor in parallel with a 0.1 µF ceramic capacitor at the point of measurement.
[2] Hot swap tested with a minimal 6000 µF capacitive loading for V_1 and 150 µF capacitive loading for V_{SB}.

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5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 5*. Alternatively, separated ground signals can be used as shown in *Figure 6*. In this case the two ground planes should be connected together at the power supplies ground pins.

NOTE: Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal. Therefore, it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

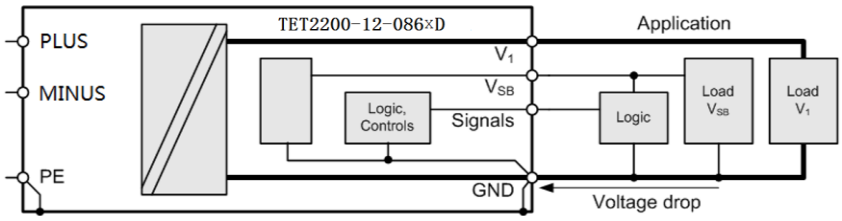

Figure 5. Common Low Impedance Ground Plane

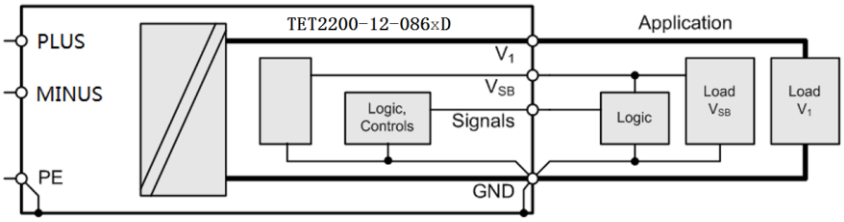

Figure 6. Separated Power and Signal Ground

5.2 CLOSED LOOP STABILITY

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of 45 degrees phase margin and -6 dB gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at 10%, 20%, 50% and 100% loads as applicable, 0% is just for reference.

5.3 RESIDUAL VOLTAGE IMMUNITY IN STANDBY MODE

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500 mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100 mV when DC voltage is applied and the PSON_L signal is de-asserted.

5.4 COMMON MODE NOISE

The common mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10 Hz to 20 MHz.

The measurement shall be made across a 100 Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure), the test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

5.5 SOFT STARTING

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the DC line or any power supply components at any specified DC line or load conditions.

5.6 ZERO LOAD STABILITY REQUIREMENTS

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.7 HOT SWAP REQUIREMENTS

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions.

5.8 FORCED LOAD SHARING

The PES front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The output will share within 10% at full load.

The 12 V_{SB} output is not required to actively share current between power supplies (passive sharing).

5.9 RIPPLE / NOISE

The test set-up shall be following *Figure 7.*

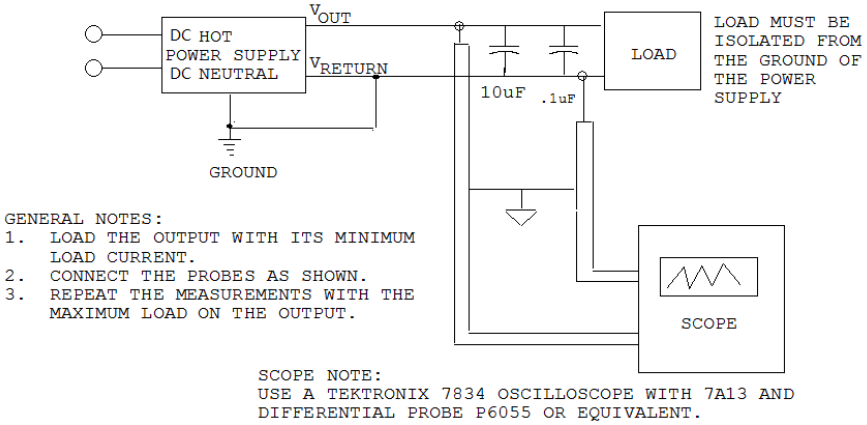

Figure 7. Differential Noise Test Setup

NOTES: Load must be isolated from the safety ground to *Figure 7.*

When performing this test, the probe clips and capacitors should be located close to the load.

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6. PROTECTION

General Condition: T_A = 0… 55 °C, unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)	Not use accessible, fast acting		80		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type	13.0	13.9	14.5	VDC
$V_{VSB\ OV}$	OV Threshold V_{SB}	Over Voltage V_{sb} Protection, Automatic recovery Type	13.0	13.9	14.5	VDC
$V_{1\ UV}$	UV Threshold V_1	Under Voltage V_1 Protection, Latch-off Type		11.2		VDC
$V_{VSB\ UV}$	UV Threshold V_{SB}	Under Voltage V_{sb} Protection, Automatic recovery Type		11.2		VDC
$I_{V1\ OC}$	OC Limit V_1	Over Current Limitation, Latch-off, $V_{i\ min}$ to $V_{i\ max}$	Refer to section 6.5			ADC
$I_{VSB\ OC}$	OC Limit V_{SB}	Over Current Limitation, Automatic recovery Type	4.5		5.5	A
T_{SD}	Over Temperature on Critical Points	Automatic shut-down	Refer to *Table 9*			°C

6.1 PROTECTION CIRCUITS

Protection circuits inside the power supply shall cause only the power supply's main output to shut down. If the power supply latches off due to a protection circuit tripping, a DC OFF for 15sec and a PSON_L cycle HIGH for 1sec shall be able to reset the power supply.

6.2 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature.
In an OTP condition the PSU will shut down, when the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on, the OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition, the OTP trip temperature level shall be at least 5°C higher than over temperature warning threshold level.

6.3 OVER VOLTAGE PROTECTION

The TET2200-12-086xD front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input. 12VSB will be auto-recovered after removing OVP limit.

6.4 UNDER VOLTAGE DETECTION

Both main and standby outputs are monitored. PWOK_H pin signal if the output voltage exceeds ±5% of its nominal voltage. The main output will latch off if the main output voltage when V1 falls below 11.2 V (typically in an overload condition), the latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input.
If the standby output leaves its regulation bandwidth for more than 10ms then the main output is disabled to protect the system.

6.5 OVER CURRENT LIMIT & OVER POWER PROTECTION (OCP & OPP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in *Table 1*. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared only by a DC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

NORM	DESCRIPTIOIN	CURRENT THRESHOLD (A)		TRIP TIMING		TESTING RANGE	COMMENTS
		MIN	MAX	MIN	MAX		
OPP	Over power protection (voltage foldback)	238	252	100 µs	NA	OPP to V fold back to 8 V	
OCP	Slow over current protection (shutdown, latch)	207	219	50 ms	100 ms		
OCPstby	Standby over current protection (shutdown, hiccup mode)	4.5	5.5				10 ms minimum delay

Table 1. OCP & OPP

6.6 PEAK LOAD WITH ADDED SYSTEM BUFFER CAPACITANCE

The power supply shall be able to support higher peak power levels with added system buffer capacitance for up to 100 µsec. *Table 2* are PMAX testing conditions.

PEAK POWER	PEAK CURRENT	SYSTEM CAPACITANCE	PEAK LOAD DURATION
2856 W	238 A	6,150 µF	100 µs

Table 2. PMAX Testing Conditions

7. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to chapter I2C / POWER MANAGEMENT BUS COMMUNICATION and document TET2200-12-086xD Power Management Bus Communication Manual.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,mon}$	Input Voltage	$V_{i\,min\,LL} \leq V_i \leq V_{i\,max}$	-1		+1	VDC
$I_{i\,mon}$	Input Current		-0.7		+0.7	ADC
$P_{i\,mon}$	True Input Power	$I_1 \leq 10\%\ I_{1\,nom}$	-22		+22	W
		$10\%\ I_{1\,nom} < I_1 \leq 20\%\ I_{1\,nom}$	-8		+8	%
		$I_1 > 20\%\ I_{1\,nom}$	-4		+4	%
$E_{i\,mon}$	Total Input Energy	$I_1 \leq 10\%\ I_{1\,nom}$	-22		+22	W
		$10\%\ I_{1\,nom} < I_1 \leq 20\%\ I_{1\,nom}$	-8		+8	%
		$I_1 > 20\%\ I_{1\,nom}$	-4		+4	%
$V_{1\,mon}$	V_1 Voltage		-1		+1	%
$I_{1\,mon}$	V_1 Current	$I_1 \leq 10\%\ I_{1\,nom}$	-1		+1	ADC
		$10\%\ I_{1\,nom} < I_1 \leq 20\%\ I_{1\,nom}$	-5		+5	%
		$I_1 > 20\%\ I_{1\,nom}$	-2		+2	%
P_{nom}	V_1 Output Power	$I_1 \leq 10\%\ I_{1\,nom}$	-15		+15	W
		$10\%\ I_{1\,nom} < I_1 \leq 20\%\ I_{1\,nom}$	-6		+6	%
		$I_1 > 20\%\ I_{1\,nom}$	-3		+3	%
E_{nom}	V_1 Output Energy	$I_1 \leq 10\%\ I_{1\,nom}$	-15		+15	W
		$10\%\ I_{1\,nom} < I_1 \leq 20\%\ I_{1\,nom}$	-6		+6	%
		$I_1 > 20\%\ I_{1\,nom}$	-3		+3	%
T_{ambmon}	*Ambient Temperature*	$0°C \leq T_{amb} \leq 55°C$	-5		+5	°C
F_S	*Fan speed*		-500		+500	RPM

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8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PSON_L						
V_{IL}	Input Low Level Voltage	PSON_L: Main output enabled	0		0.8	V
V_{IH}	Input High Level Voltage	PSON_L: Main output disabled	2		5.25	V
$I_{IL,H}$	Maximum Source Current	V_I = - 0.2 V to + 3.5 V			4	mA
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply			10		kΩ
PWOK_H						
V_{OL}	Output Low Level Voltage	$Vi < V_{i\ min\ LL}$, $I_{sink} = 400\ \mu A$	0		0.4	V
V_{OH}	Output High Level Voltage	$Vi > V_{i\ min\ LL}$, $I_{source} = 200\ \mu A$	2.4		3.46	V
I_S	Maximum Sink Current Maximum Source Current	PWOK_H = low PWOK_H = high			400 2	µA mA
SMB_ALERT_L						
V_{ext}	Maximum External Pull up Voltage				3.46	V
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4 mA	0		0.4	V
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply			10		kΩ
I_S	Sink Current	SMB_ALERT_L = low SMB_ALERT_L= high			4 50	mA µA
VIN_OK_H						
V_{ext}	Maximum External Pull up Voltage				3.46	V
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4 mA	0		0.4	V
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply			1		kΩ
I_S	Sink Current	VIN_OK_H = low			4	mA

8.2 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.
With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.3 PS_KILL INPUT

The PS_KILL input is an active-high and normally a trailing pin in the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND on the system. The standby output will remain on regardless of the PS_KILL input state.

8.4 PRESENT_L OUTPUT

The PRESENT_L pin is wired through a 100 Ohm resistor to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low level voltage if power supply is seated.

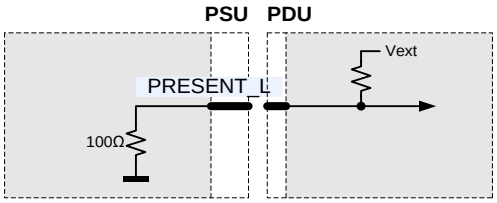

Figure 8. PRESENT_L Connection

8.5 PSON_L INPUT

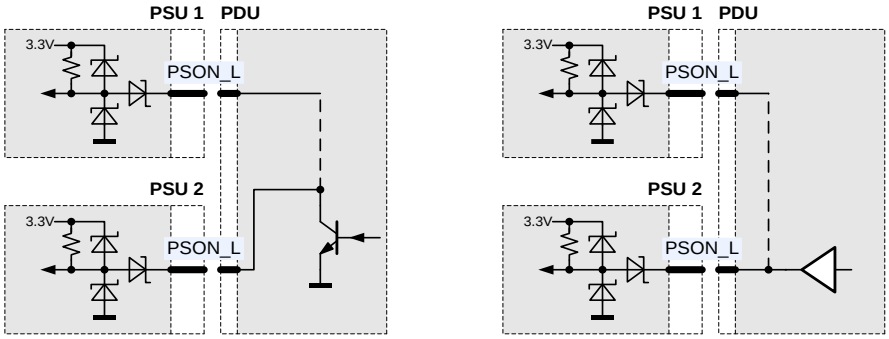

Figure 9. PSON_L connection

8.6 PWOK_H OUTPUT

PWOK_H is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when DC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK_H will be de-asserted to a LOW state. The start of the PWOK_H delay time shall be inhibited as long as any power supply output is in current limit.
The PWOK_H and I2C bus of PSU are connected together on the redundant system. The below block diagram was shown the wiring on the system. The internal PWOK_H circuit of power supply is designed so that the PWOK_H bus is the wire-ORed function of the individual PWOK_H signals of all the power supply in parallel. Suggest system Pull-up to 3V3 and pull-up resistance is 10K. The PWOK_H signal also can be separated for each PSU design in system side to indicate each PSU output state.

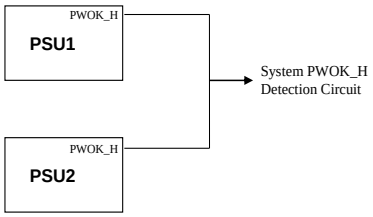

Figure 10. PWOK_H connection

8.7 SMB_ALERT_L OUTPUT

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, over-current, under voltage. This signal may also indicate the power supply is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid Yellow.

The inlet temperature warning threshold must be set at 60°C, preventing exhaust air and cord temperatures temperature exceeding safety ratings. The warning gets de-asserted once inlet air temperature returns into specified operating temperature range. Fan speed control algorithm shall ramp up the fan speed to the maximum prior to the OT_WARNING bit set in STATUS_TEMPERATURE (7Dh) register.

In case exhaust air temperature exceeds 70°C higher temp rating cord must be used.

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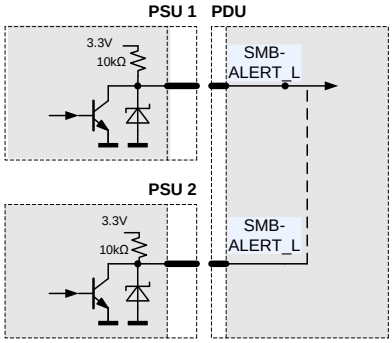

Figure 11. SMB_ALERT_L Connection

8.8 VIN_OK_H OUTPUT

This signal will be asserted, driven high, by the power supply to indicate that the input voltage meets the minimum requirements of the parametric PSU specification.

The PSU shall de-assert (drive low) under input over-voltage condition.

DC LINE AND DC LOSS DETECTION ALGORITHM

DC line voltage detection for power on:

The power supply will use Vrms to determine if the input voltage is within the specified requirements for turning on the power supply unit as called out by the individual power supply specification for DC input voltage range. The Vrms of the input must be determined within 100 ms after the application of DC & Standby has reached regulation. Assertion requirements for VIN_OK_H remain the same.

DC line voltage detection for a DC brownout and dropout:

PSU shall detect both DC brown out and dropout conditions and issue a power down warning to the end system. The PSU shall de-assert (drive low) VIN_OK_H upon input conditions that fall below the Vin (turn-off) specification of the PSU parametric specification. Under such conditions. After VIN_OK_H de-assertion, the PSU shall derive an average RMS input voltage, measured over a moving average window equal to T1, to establish if conditions meet the requirements for assertion of VIN_OK_H. Refer to *Figure 12*.

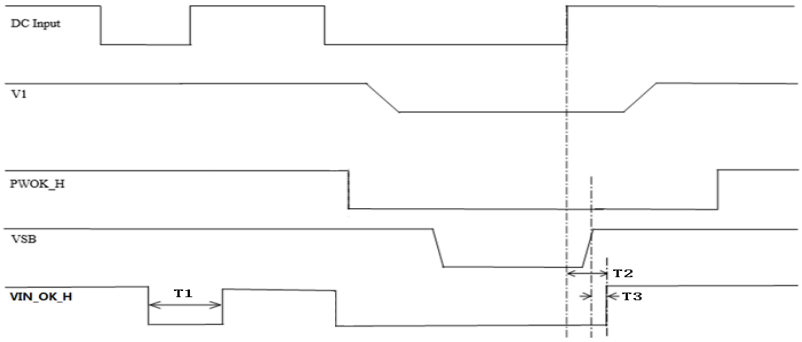

Figure 12. VIN_OK_H Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T1	VIN_OK_H Dwell Time	75		120	ms
T2	VIN_OK_H delay to DC			1700	ms
T3	VIN_OK_H to 12VSB			20	ms

NOTE: T1 is the minimum VIN_OK_H de-assertion dwell time that is initiated when the PSU has declared a loss of input voltage.

Table 3. VIN_OK_H Timing Requirements

8.9 TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{V1_rise}) within 1.0 ms to 70 ms. For 12 VSB, it is allowed to rise from 5ms between 20 ms. All outputs must rise monotonically. *Table* shows the timing requirements for the power supply being turned on and off two ways; 1) via the DC input with PSON_L held low; 2) via the PSON_L signal with the DC input applied. The PSU needs to remain off for 1 second minimum after PWOK_H is de-asserted.

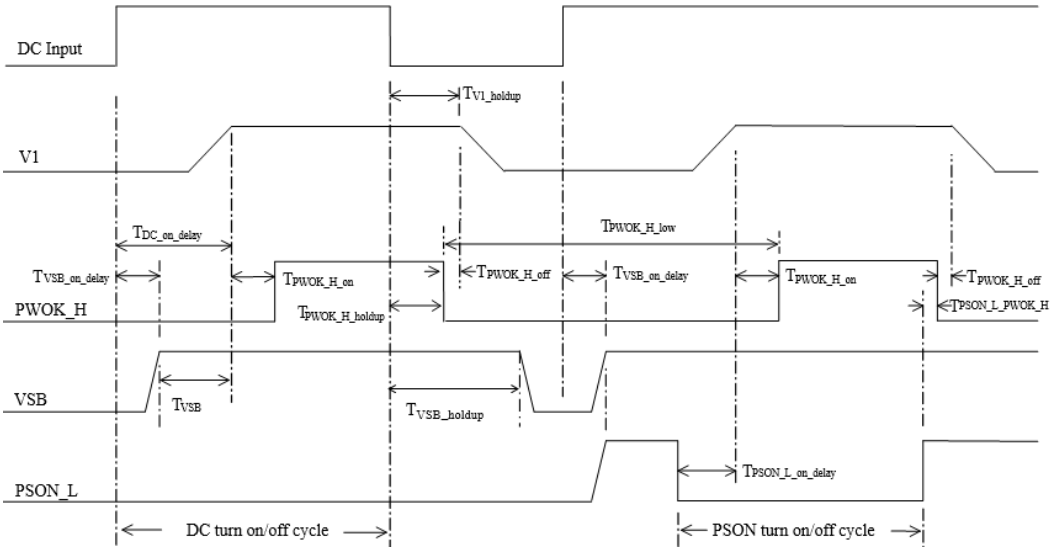

Figure 13. Turn On/Off Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_{V1_rise}	Output voltage rise time	1.0 *		70 *	ms
$T_{VSB_on_delay}$	Delay from DC being applied to 12 VSB being within regulation.			1500	ms
$T_{DC_on_delay}$	Delay from DC being applied to all output voltages being within regulation.			3000	ms
T_{V1_holdup}	Time 12 V output voltage stay within regulation after loss of DC (48VDC input).	0.3			ms
$T_{PWOK_H_holdup}$	Delay from loss of DC to de-assertion of PWOK_H (48VDC input).	0.3			ms
$T_{PSON_L_on_delay}$	Delay from PSON_L active to output voltages within regulation limits.	5		400	ms
$T_{PSON_L_PWOK_H}$	Delay from PSON_L deactivate to PWOK_H being de-asserted.			5	ms
$T_{PWOK_H_on}$	Delay from output voltages within regulation limits to PWOK_H asserted at turn on.	100		500	ms
$T_{PWOK_H_low}$	Duration of PWOK_H being in the de-asserted state during an off/on cycle using DC or the PSON_L signal.	100			ms
T_{VSB}	Delay from 12 VSB being in regulation to O/Ps being in regulation at DC turn on.	50		1000	ms
T_{VSB_holdup}	Time the 12VSB output voltage stays within regulation after loss of DC (48VDC input).	3			ms
$T_{DC_off_SMB_ALERT_L}$	The power supply shall assert the SMB_ALERT_L signal quickly after a loss of DC input voltage.			2	ms

* The 12VSB output voltage rise time shall be from 5.0 ms between 20 ms.

Table 4. Timing Requirements

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8.10 HOT_STANDBY

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable Oring gate, to make sure into hot standby mode. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency.

8.11 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and amber and indicates DC and DC power presence and warning or fault conditions. *Table 6* lists the different LED status.

	MIN λd WAVELENGTH	NOMINAL λd WAVELENGTH	MAX λd WAVELENGTH	UNITS
Green		570		nm
Super Bright Yellow		590		nm

Table 5. LED Characteristics

OPERATING CONDITION	LED STATE
Output ON and OK	Solid GREEN
No DC input power to all power supplies; 12 VSB power failed, OCP, SC, OVP and UVP.	OFF
DC input present / Only 12 VSB on (Standby mode)	0.5 Hz Blink GREEN
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1 Hz Blink AMBER
12 V1 critical event causing a shutdown; failure eg. OCP, OVP, OTP, Fan Fail, Input OVP	Solid AMBER
Power supply in FW upload mode; Sleep PS in Hot standby state/off line mode	2 Hz Blink GREEN

Table 6. LED Status

9. I²C / POWER MANAGEMENT BUS COMMUNICATION

The PES front-end is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in *Table 7* further characterized through:

- The SDA/SCL IOs use 3V3 logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

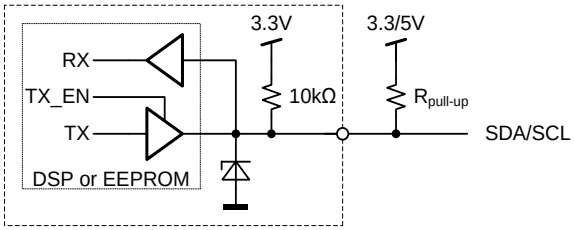

Figure 14. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input DC voltage is provided. If no DC is present, communication to the unit is possible as long as it is connected to a life V_{SB} output or V_1 output (provided e.g. by the redundant unit).

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b [1]	1000	ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b [1]	300	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull\text{-}up}$	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 7. I²C / SMBus Specification

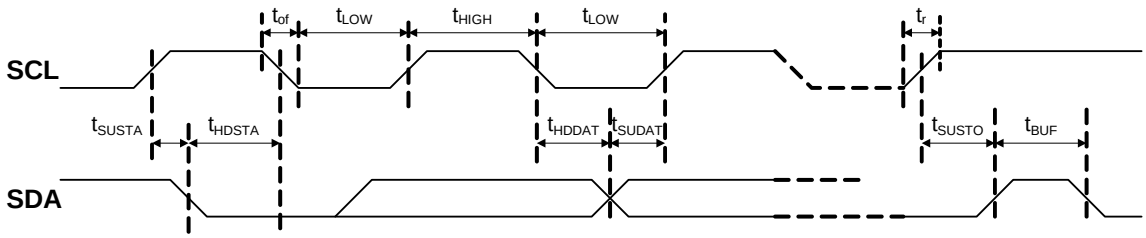

Figure 15. I²C / SMBus Timing

ADDRESS SELECTION

The address for I²C communication can be configured by pulling address input pin A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A0 pin to be in High Level if left open.

A fixed addressing offset exists between the Controller and the EEPROM.

A0	I2C Address	
	Controller	EEPROM
0	0xB0	0xA0
1	0xB2	0xA2

Table 8. Address and Protocol Encoding

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9.1 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see *Figure 16*) and can be accessed under different addresses, see ADDRESS SELECTION.

The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3V3.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

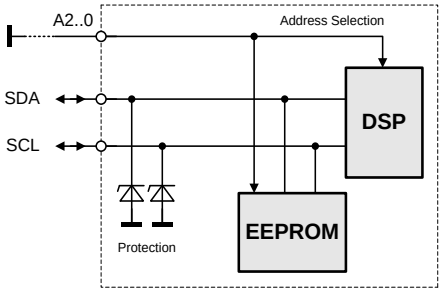


Figure 16. I2C Bus to DSP and EEPROM

9.2 EEPROM PROTOCOL

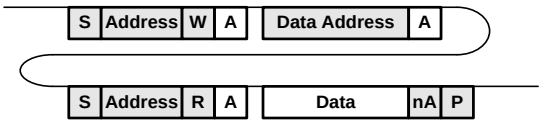
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



9.3 POWER MANAGEMENT BUS PROTOCOL

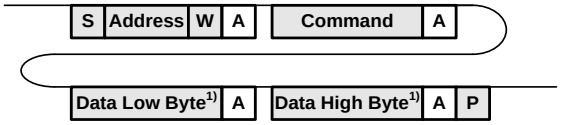
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed.
The TET2200-12-086xD supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

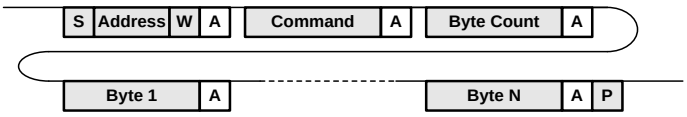
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



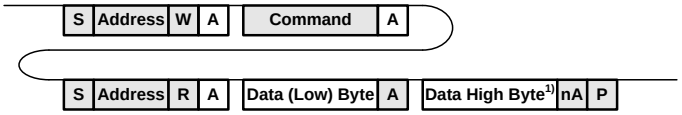
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See TET2200-12-086xD Power Management Bus Communication Manual BCA.00297 for further information.



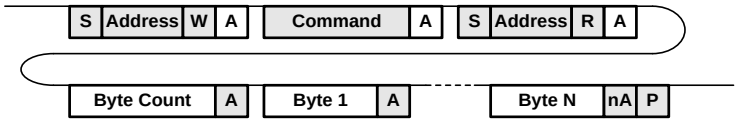
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See TET2200-12-086xD Power Management Bus Communication Manual BCA.00297 for further information.



9.4 POWER SUPPLY BLACK BOX RECORDER

The power supply shall save the latest data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible via the Power Management Bus communication interface with an external source providing power to the 12Vstby output.
Critical Events to trigger an update to the Event Recorder includes:

- Output OVP
- Output OCP
- Input OV/UV Fault
- Fan fault
- OTP
- Other faults to cause output shutdown.

Refer to BCA.00297 Power Management Bus Communication Application Note for further information about the Power Management Bus commands to support this function.

9.5 FIRMWARE UPDATE

The power supply shall have the capability to update its firmware via the Power Management Bus interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 12Vstby pins. BPS standard GUI supports the firmware upgrade function.

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9.6 GRAPHICAL USER INTERFACE

Bel Power Solutions provides with its "I²C Utility" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the TET2200-12-086xD Front-End. The utility can be downloaded on: belfuse.com/power-solutions and supports both the PSMI and Power Management Bus protocols.
The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.
If the GUI is used in conjunction with the YTM.G2M01.0 Evaluation Board it is also possible to control the PSON_L pin(s) of the power supply.

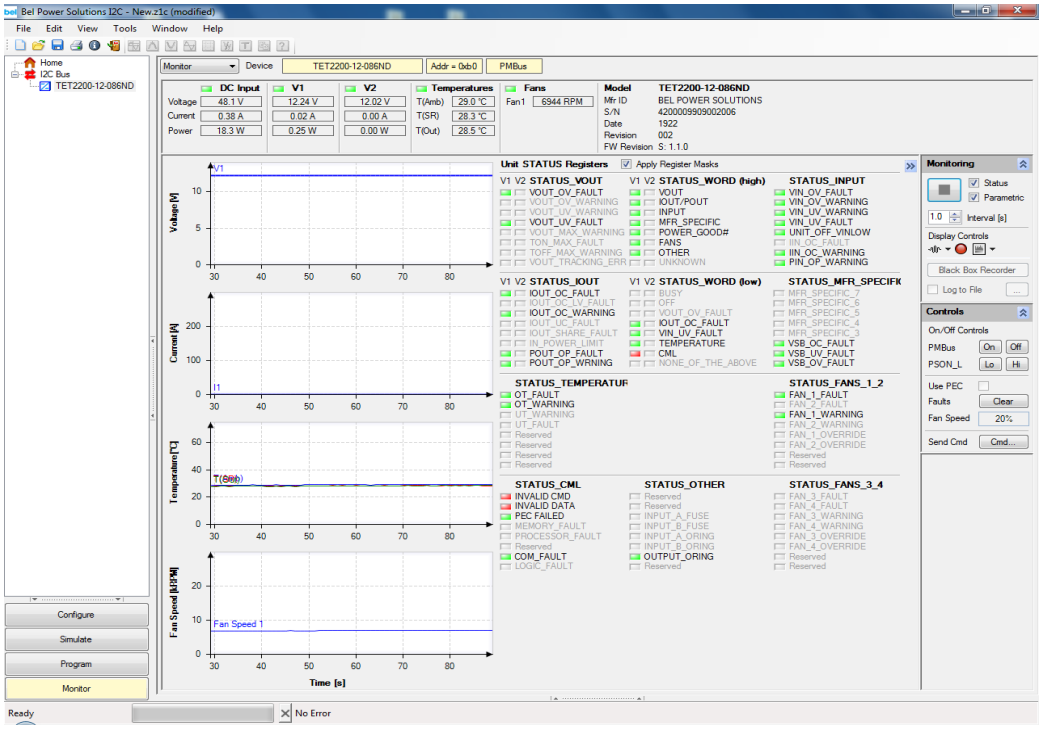

Figure 17. Monitoring dialog of the I²C Utility

10. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the air-flow at the rear of the supply by placing large objects directly at the output connector. The TET2200-12-086ND is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the DC-inlet and TET2200-12-086RD is reversed. The TET2200-12-086xD supply has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

The fan oscillation shall be controlled such that associated sound power level variation falls within a band of 2.0 dBA (roughly 10% mean speed). This condition may be treated as steady state fan speed condition.

After the new load and/or cooling condition steady state is established, transition to the steady state fan speed shall take place within 60 s.

The TET2200-12-086xD provides access via I²C to the measured temperatures of in total 3 sensors within the power supply, see *Table 9*. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V1 (or VSB if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signalized accordingly through LED, PWOK_H and SMB_ALERT_L.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	POWER MANAGEMENT BUS REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet air temperature	Sensor located on control board close to DC end of power supply (NAF) Sensor located on main board close to DC front of power supply (RAF)	8Dh	60°C (NAF) 65°C (RAF)	65°C (NAF) 70°C (RAF)
Syn rectifier Mosfet 1	Sensor located close to Syn rectifier Mosfet group 1	8Eh	115°C (NAF) 106°C (RAF)	120°C (NAF) 112°C (RAF)
Syn rectifier Mosfet 2	Sensor located close to Syn rectifier Mosfet group 2	EAh	115°C (NAF) 106°C (RAF)	120°C (NAF) 112°C (RAF)

Table 9. Temperature Sensor Location and Thresholds

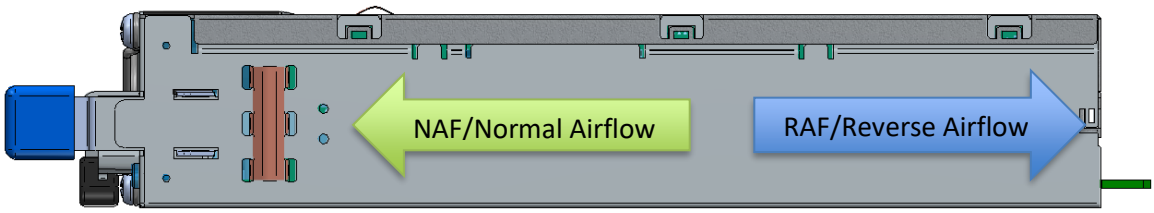

Figure 18. Airflow Direction

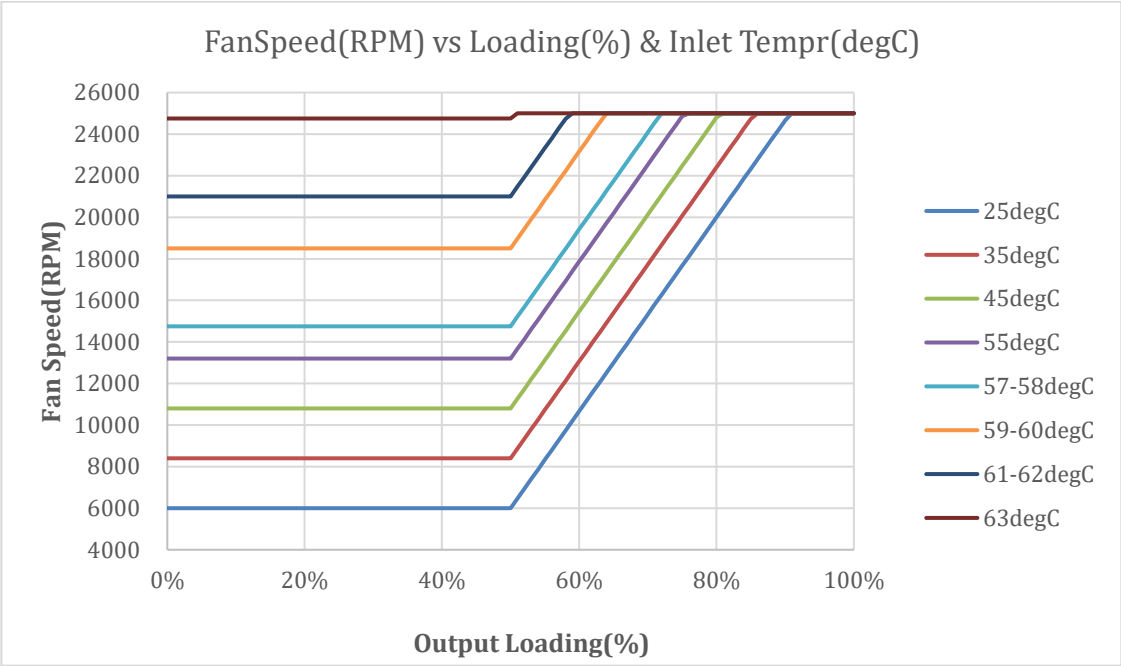

Figure 19. Fan Speed vs. Main Output Load

Comment: The fan minimum speed is 6000 RPM.

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11. ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LED, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetics Filed	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1µs Pulse Modulation, 10 kHz ... 2.7 GHz	A
Burst	IEC / EN 61000-4-4, ±1 kV, 1 minute	A
Surge*	IEC / EN 61000-4-5, Line to earth: ±1 kV Line to line: ±1 kV	A
RF Conducted Immunity	IEC / EN 61000-4-6, Level 3, 10 Vrms, CW, 0.15 … 80 MHz	A

* The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.
The power supply shall be tested in accordance with IEC 61000-4-5: 2005, more criteria details refer to *Table 10*.

LEVEL	DESCRIPTION
A	During and after the test, the EUT shall continue to operate as intended without operator intervention.
B	Degradation of performance is allowed during test and the EUT shall continue to operate as intended without operator intervention after the test. And EUT can recover without operator intervention when test condition removed.
C	Temporary loss of function is allowed, provided the function is self-recoverable or can be restored by the operation of the controls or cycling of the power to the EUT by the user in accordance with the manufacturer's instructions.

Table 10. Performance Criteria

11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55032:2015 / CISPR 32:2015: 0.15 … 30 MHz, QP and AVG	Class A 6 dB margin
Radiated Emission	EN 55032:2015 / CISPR 32:2015: 30 MHz … 1 GHz, QP	Class A 6 dB margin

12. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 62368-1, and UL/CSA 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to latest edition of the following standards: UL/CSA 62368-1 (USA / Canada) IEC/EN 62368-1 (International/ Europe) CB Certificate & Report, IEC62368-1 (report to include all country national deviations) CE - Low Voltage Directive 2014/35/EC (Europe) GB4943.1- CNCA Certification (China)	Approved
Isolation Strength	Input (L/N) to chassis (PE) Input (L/N) to output Output to chassis	Basic Basic None (Direct connection)
Electrical Strength Test	Input to output Input to chassis	1500 VDC 1500 VDC

Comment: All printed wiring boards and all connectors meet UL94V-0 level.

13. ENVIRONMENTAL

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as "Handle, knobs, grips, etc. held for short periods of time only".

In case the exit air temperature requirement cannot be met, the power supply must have a warning label for high touch temperature that is in compliance with IEC/UL 60950-1 and additionally 85°C rated power cords must also be used with this power supply.

ITEM	DESCRIPTION	MIN	MAX	UNITS
Load	Maximum typical load under redundant configurations		1320	W
Top1	Operating temperature range; 900 m	0	55	°C
Top2	Operating temperature range; 3050 m	0	50	°C
Texit	Maximum exit air temperature		68	°C
Tnon-op	Non-operating temperature range	-40	70	°C
Altitude1	Maximum operating altitude; 50°C inlet		3050	meters
Altitude2	Maximum operating altitude; 55°C inlet		900	meters
Acoustical Noise	A-weighted sound power, 25°C, 50% Load		50	dB

Table 11. Requirements for Redundant Power Supply Configuration

ITEM	DESCRIPTION	MIN	MAX	UNITS
Load	Maximum rated output load		2200	W
Top1	Operating temperature range; 900 m	0	55	°C
Top2	Operating temperature range; 3050 m	0	50	°C
Texit	Maximum exit air temperature		68	°C
Tnon-op	Non-operating temperature range	-40	70	°C
Altitude1	Maximum operating altitude; 50°C inlet		3050	meters
Altitude2	Maximum operating altitude; 55°C inlet		900	meters
Acoustical Noise	A-weighted sound power, 25°C, 50% Load		50	dB

Table 12. Requirements for Non-Redundant Power Supply Configuration

13.1 HUMIDITY

Operating: To 85% relative humidity (non-condensing)
Non-Operating: To 95% relative humidity (non-condensing)
NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

13.2 ALTITUDE

Operating: To 3050 m (Maximum operating altitude 5000 meters and the Maximum operating temperature to 40°C.)
Non-operating: To 15200 m

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13.3 SHOCK AND VIBRATION

13.3.1 RANDOM VIBRATION – OPERATING

Sample Size: For all product classes and categories, the minimum number of samples shall be 3 devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing - Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance. Each device shall be tested in three axes for a minimum of 30 minutes per axis. The device shall be powered for the duration of the test at nominal input voltage and no load. For operating vibration testing, see *Figure 20*.

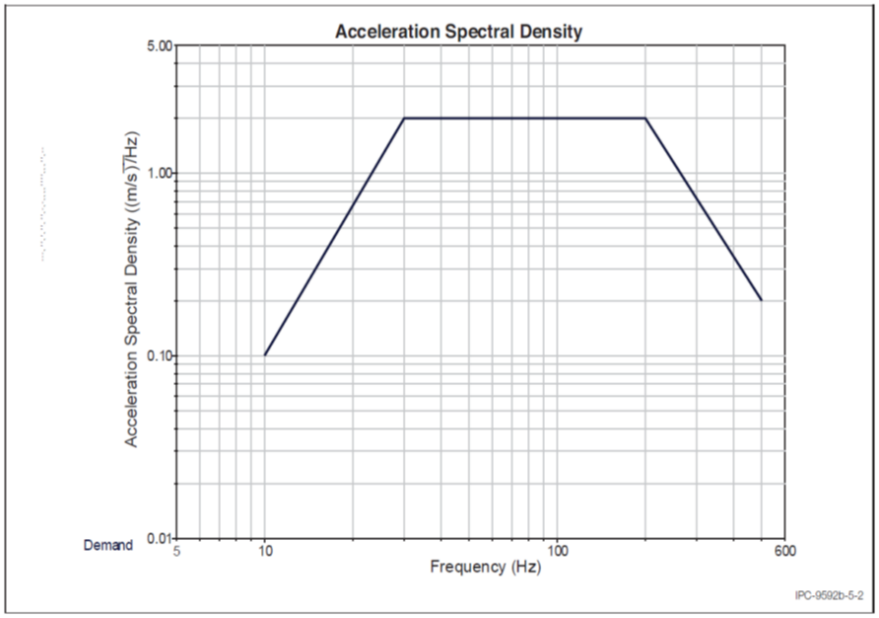

Figure 20. Class II PCDs Operating Vibration Test: Acceleration vs Frequency

The total acceleration for Class II PCDs is approximately 2.4 grms, see *Table 13*.

Frequency	Class I Acceleration Specification		Class II Acceleration Specification	
Hz	$(m/s^2)^2/Hz$	G^2/Hz	$(m/s^2)^2/Hz$	G^2/Hz
10	0.022	0.000229	0.1	0.00046
30	0.20	0.0021	2	0.0052
200	0.20	0.0021	2	0.0052
500	0.0052	0.000054	0.2	0.0001
Grms = 0.71			Grms = 2.40	

Table 13. Operation Vibration Profile Charts

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

13.3.2 RANDOM VIBRATION - NON-OPERATING

Sample Size: For all product categories and product classes, the minimum number of samples shall be 3 devices packaged in their fully populated, bulk shipping package or individual packages of product.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing –

Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance, with the acceleration spectral density curves provided in this document. The products are in the shipping packaging for this test. For non-operating vibration testing, see *Table 14*. Each shipping package shall be tested in three axes for a minimum of 30 minutes per axis.

The total acceleration for Class II PCDs is approximately 3.8Grms, see *Table 14*.

Frequency	Class I Acceleration Specification		Class II Acceleration Specification	
Hz	$(m/s^2)^2/Hz$	G^2/Hz	$(m/s^2)^2/Hz$	G^2/Hz
5	1	0.01	5	0.0052
200	1	0.01	5	0.0052
500	0.03	0.003	0.3	0.003
	Grms = 1.90		Grms = 3.80	

Table 14. Non-Operating Vibration Profile Charts

Pass Criteria: At the conclusion of all three axes of testing, the products shall be unpackaged and visually inspected for any signs of damage. Only minor cosmetic damage that does not affect form, fit or function is allowed. Bent connector pins, damaged switches, damaged handles, labels with impaired readability, or bent or deformed sheet metal are not allowed. All units shall also pass a functional test.
There are no requirements on the condition of the shipping package.

13.3.3 SHOCK – OPERATING

Sample Size: For all product types and product classes, the minimum number of samples shall be three (3) devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-27, Environmental Testing-Part 2.27 Test Ea and guidance: Shock. Each tested device shall be exposed to three shocks in each of three axes. The amplitude of each shock shall be no less than 30 g with a half sine wave shape and a duration of 11 ms.

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

13.3.4 THERMAL SHOCK (SHIPPING)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

14. RELIABILITY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	Mean time between failure	T_A = 40°C, 75% load, according Telcordia SR-332, issue 3	250			kh

Comment: All components de-rating follows IPC9592B.

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15. MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		86.3		mm
	Heigth		39.3		mm
	Depth		196.5		mm
Weight			1.0		kg

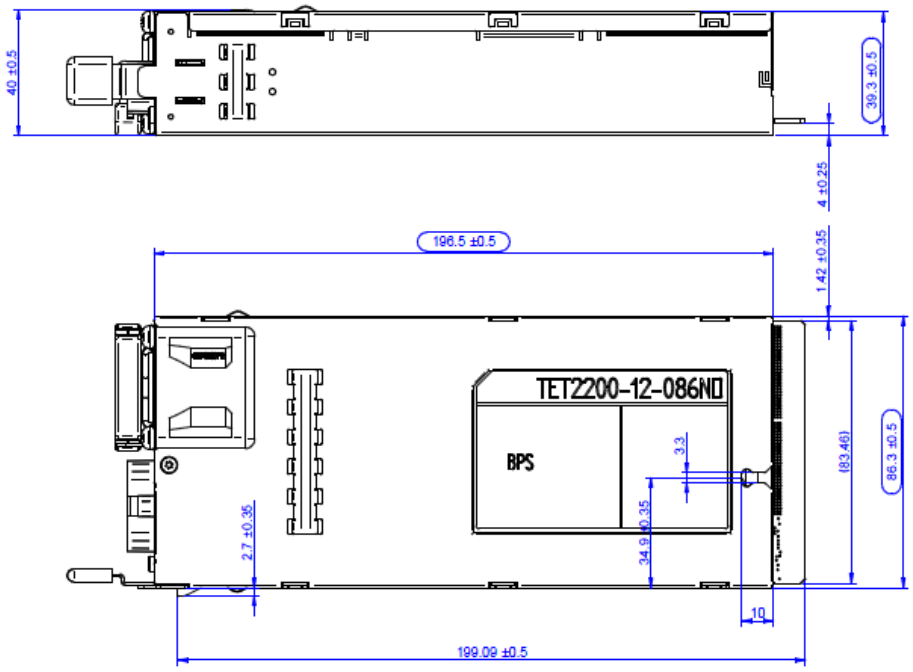


Figure 21. Top, bottom and side view

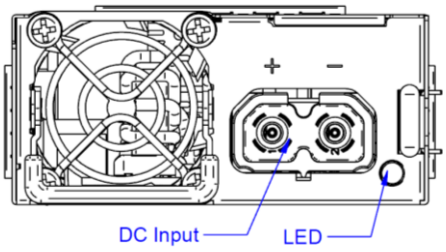


Figure 22. Front view

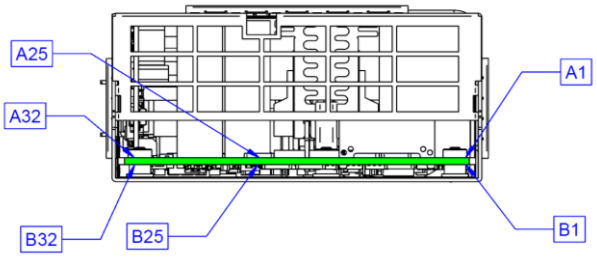
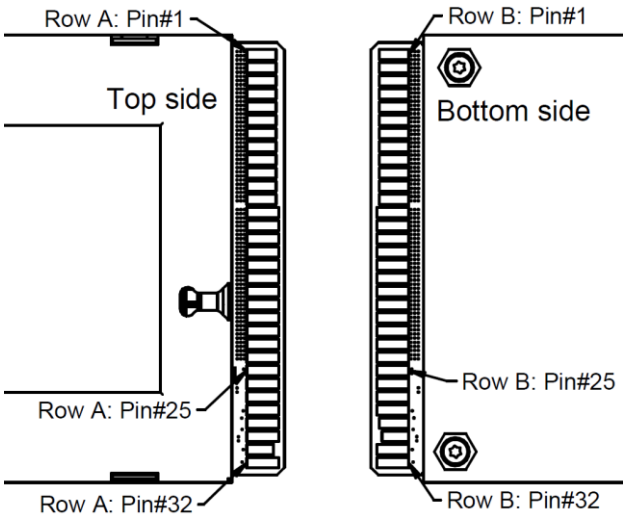


Figure 23. Rear view

16. CONNECTORS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Input connector	Amphenol, RADSOK® Receptacle C10-752109-000 or equivalent				
Input DC cord requirement	Wire size		6		AWG
Mating Input connector	Manufacturer : Amphenol Manufacturer P/N : C10-752158-000 Or equivalent				
Output connector	PCB card edge				
Mating output connector	Manufacturer : FCI Electronics Manufacturer P/N: 10053363-200LF, 10046971-001LF Refer to *Table 15* respectively for the pin assignment				



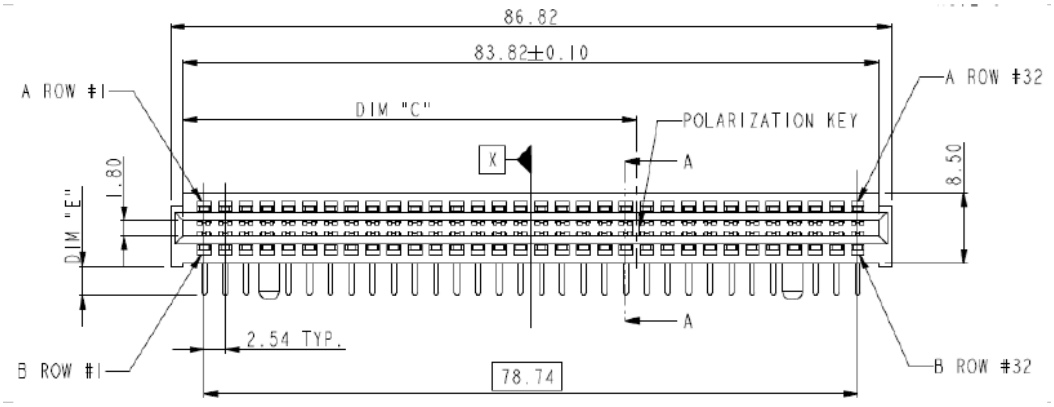


Figure 24. Mating output connector

NOTE: For Mating output connector FCI 10053363-200LF or 10046971-001LF Pin assignment see Figure 24

Row A	DESCRIPTION

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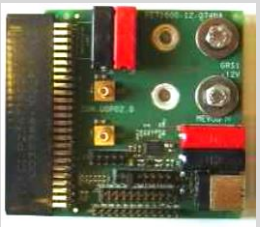
PIN	NAME	PIN TYPE	Mating Sequence	
P1-12	12 V Output	12V Main Output	STD	+12 V Main Output
P13-24	PWR Return		Long	+12 V Main and +12VSB Output return (GND)
P25	12V Remote Sense	Input	Long	12 V Output Remote Sense; +VE lead; compensates for voltage drops to POL
P26	12 VSTBY	Aux/Standby Power	Long	+12VSTANDBY output
P27	A0	Input	Long	Power Management Bus address A0
P28	PWOK_H	Output	Long	Active high; indicates +12V Main is valid and within operational limits
P29	Signal Return Output	Signal GND	Long	Signal GND; (MFBL) long connection
P30	SCL	Bi-Directional; I/O	Long	I²C / SMBus / Power Management Bus Clock Line
P31	PRESENT_L	Output	Short	Power Supply Present; passive signal to Signal Return
P32	SDA	Bi-Directional; I/O	Long	I²C / SMBus / Power Management Bus Data Line

PIN	Row B NAME	PIN TYPE	Mating Sequence	DESCRIPTION
P1-12	12V Output	12V Main Output	STD	+12 V Main Output
P13-24	PWR Return		Long	+12 V Main and +12 VSB Output return (GND)
P25	Hot_ Standby	I/O	Long	Hot standby Bus for system efficiency performance
P26	Return Sense	Analogue Input	Long	12 V Main Output Remote Sense Return
P27	VIN_OK_H	Output	Long	Indicate DC input voltage is present and within operational limits.
P28	12 V Load Share Bus	Bi-Direction Analogue I/O	Long	+12V Main Output Current Share Signal (bus)
P29	PSON_L	Input	STD	Active low; +12 V Main output on/off control
P30	PS_KILL	Input	Short	Turns power module on/off, short (MLBF) contact
P31	No Connection		Long	No End User Connection
P32	SMB_ALERT_L	Output	Long	Active low; I²C alert signal (interrupt)

All signal pins are referred to SGND

Table 15. Output connector pin assignment

17. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	I²C Utility Windows XP/Vista/7 compatible GUI to program, control and monitor TET2200-12-086xD Front-Ends (and other I²C units)	N/A	belfuse.com/power-solutions
	**Evaluation Board** Connector board to operate TET2200-12-086xD. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).	YTM.G2M01.0	belfuse.com/power-solutions

It is recommend adding each a width 18 mm x thickness 1 mm x length 35 mm busbar for 12 V+/- on loading board as such high output current density.

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

18. REVISION HISTORY

DATE	REVISION	SECTION	CHANGES / UPDATES	PREPARED BY	ECO/MCO REFERENCE NO.
2019/03/06	001	/	First draft	Zaipeng Wei	
2019/03/20	002	11	Update Immunity and Emission requirement	Zaipeng Wei	
2019/04/11	003	15 16 8.4	Update drawing Update output connector Pin assignment Update Figure adding 100 Ohm resistor	JG Yu Zaipeng Wei	
2019/05/31	004	8.11 6.5 5 4 9 5	Update Table 6 LED Status Remove OCW requirement Update Dynamic Load start point Update Max Input current Update Table 9 OTP thresholds *Change $V_{SB\ nom}$ to 12.2V*	Zaipeng Wei	C94777
2019/09/24	5	5 8.1&8.7 15 /	Change V_{SB} Capacitive Loading and rise time Update SMB_ALERT_L pull-up resistor Update drawing Add series model	Zaipeng Wei JG Yu	
2020/08/05	A	9.4 5	Add EVENT RECORDER function Update minimum $t_{VSB\ rise}$	Zaipeng Wei	
2020/12/15	B	9.4 13/16	Change to POWER SUPPLY BLACK BOX RECORDER Change the power density to 54.1W/inch3 Change the Acoustic noise to 50dB Change the picture of the gold finger	Jemrry Zhang Ryan Li	CO109065
2023/07/11	C	11,15,16	Add or equivalent for input connector at section 16 and correct input connector to C10-752109-000 Remove the tolerance spec at section 15 Update the safety approve standard at section 11	Xiao Xue	

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

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