Powerline Test Fixture

0804-EVALB02

The Bel 0804-EVALB02 Powerline test fixture lets you quickly get started testing the 200 and 500 Mbps HomePlug® AV Bel Powerline modules.

The 0804-EVALB02 Powerline test fixture provides all the required circuitry (mains coupler, power supply, zero-crossing detection, protection and Ethernet interface) for interfacing a Bel Powerline module.

You just need an Ethernet cable and a two conductor medium to make the Powerline test fixture operate as a gateway between an Ethernet network and a powerline network.

Key Features & Benefits

- Compatible with Bel 0804-5000-18/-24/-25/A50/E50 Powerline modules
- Fully configurable AC/DC/Dry Wire operation
- Wide range 19-75V DCDC Convertor included
- Led status indicators
- Push buttons for Pairing, Reset & Factory defaults
- 5 Ethernet ports

RoHS Compliant

Models

Part Number	Description
0804-EVALB02	HomePlug® AV Powerline Test Fixture (200/500Mbits)

bel POWER SOLUTIONS & PROTECTION
a bel group

Bel Modules
28 Turkey Court, Turkey Mill, Ashford Road
Maidstone ME14 5PP UK

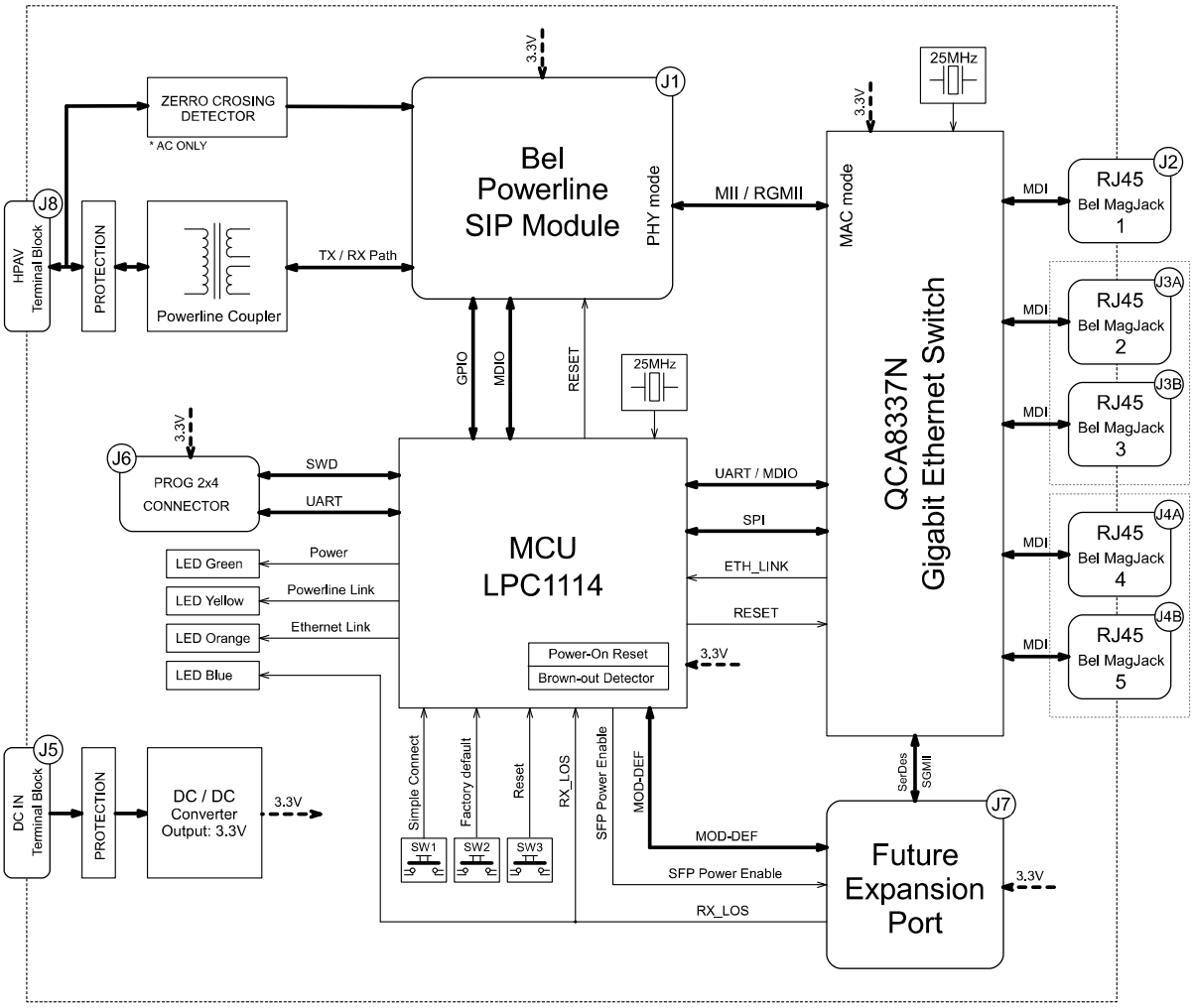
+44 1622 757 395
techhelp@belf.com
belfuse.com

© 2017 Bel Power Solutions, Inc

Rev F

Please read our datasheet & drawing disclaimer here.

Evaluation board block diagram



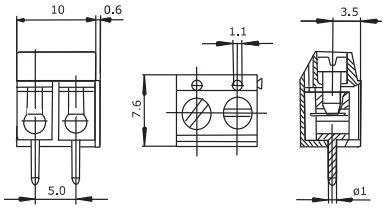
LED Indicators

Reference	Colour	Signal route	Default Behavior
D5	Green	Powerline Module: GPIO11 (when SIP is present)	Power
D4	Yellow	Powerline Module: GPIO8	Powerline Tx/Rx Link
D3	Orange	Ethernet Switch	Ethernet Tx/Rx Link
D2	Blue	Expansion Port	Reserved

Push Buttons

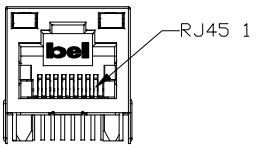
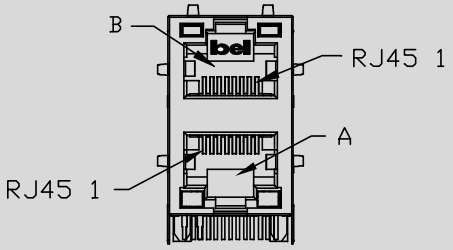
Reference	Name	Signal route	Use
SW1	Simple connect	Powerline Module: GPIO1	Simple connect – pairing button.
SW2	Factory default	Powerline Module: GPIO2	Restoring the factory default PIB.
SW3	Reset	RESET	Press this button to reset the board.

5mm Pitch Spacing Terminal Block

Reference	Use	View
J5	DC Power IN (support range 19-75V DC/DC)	
J8	HPAV communication terminal	

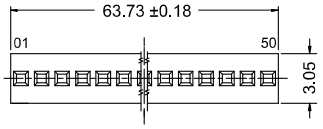
** Use under safety cover. With exposed board due to safety reason please do not use higher voltage than 24V.*

Ethernet Connectors

Reference	Description	View
J2	RJ45 Magjack® 10/100/1000Base-T Ethernet shielded connector.	
J3, J4	2 Port RJ45 Magjack® 10/100/1000Base-T Ethernet shielded connector.	

Pin Number	Pin Name	Direction	Electrical Characteristics
1	BI_DA+	Bi-directional pair A +	Standard IEEE 802.3
2	BI_DA-	Bi-directional pair A -	Standard IEEE 802.3
3	BI_DB+	Bi-directional pair B +	Standard IEEE 802.3
4	BI_DC+	Bi-directional pair C +	Standard IEEE 802.3
5	BI_DC-	Bi-directional pair C -	Standard IEEE 802.3
6	BI_DB-	Bi-directional pair B -	Standard IEEE 802.3
7	BI_DD+	Bi-directional pair D +	Standard IEEE 802.3
8	BI_DD-	Bi-directional pair D -	Standard IEEE 802.3

Powerline Module Connector

Manufacturer's part number	Reference	Description	View
Samtec SMS-150-01-G-S	J1	50 ways, 1 row, through holes micro socket. Pitch 1.27mm. Insertion force 8oz; withdrawal force 6 oz.	

This connector is to be directly connected to 200Mbps Powerline module: 0804-5000-18, 0804-5000-24, 0804-5000-25 or 500Mbps Powerline module: 0804-5000A50 or 0804-5000E50. The pin 1 of the Powerline module must be connected to pin 1 of J1.

Pin Number	Pin Name MII 200Mbps	RGMII 500Mbps	Type	Description
1	VDD	VDD	PWR	+3.3V
2	VSS	VSS	PWR	Ground
3	VDD	VDD	PWR	+3.3V
4	VSS	VSS	PWR	Ground
5	VDD	VNET_IO	PWR	200Mbps: VDD +3.3V 500Mbps: RGMII voltage level: +2.5V / +3.3V
6	TX+	TXRX+	I/O	200Mbps: Differential TX+ signal, connects to coupling transformer 500Mbps: Differential TXRX+ signal, connects to coupling transformer
7	TX-	TXRX-	I/O	200Mbps: Differential TX- signal, connects to coupling transformer 500Mbps: Differential TXRX- signal, connects to coupling transformer
8	VSS	VSS	PWR	Ground
9	RX+	RESERVED	I/O	200Mbps: Differential RX signal, connects to coupling transformer 500Mbps: Reserved pin
10	RX-	RESERVED	I/O	200Mbps: Differential RX signal, connects to coupling transformer 500Mbps: Reserved pin
11	RESET#	RESET#	I	Resets all IC logic when low
12	GPIO0	GPIO0	I/O	200Mbps: Strap - N/A 500Mbps: Strap - ENET_SEL[0]
13	GPIO1	GPIO1	I/O	200Mbps: Strap - N/A; Push-button: Simple connect 500Mbps: Strap: ENET_SEL[1]; Push-button: Simple connect
14	GPIO2	GPIO2	I/O	200Mbps: Strap - N/A; Push-button: Factory default 500Mbps: Strap - ANEN; Push-button: Factory default
15	**GPIO3**	**RESERVED**	I/O	200Mbps: Strap - ISODEF 500Mbps: Reserved pin
16	GPIO4	GPIO4	I/O	200Mbps: Strap - SPEED 500Mbps: Strap - SPEED_SEL[0]
17	GPIO5	GPIO5	I/O	200 / 500Mbps: Strap - MD_A3
18	GPIO6	GPIO6	I/O	200 / 500Mbps: Strap - CFG_SEL
19	GPIO7	GPIO7	I/O	200 / 500Mbps: Strap - MD_A4
20	GPIO8	GPIO8	I/O	200 / 500Mbps: Strap - MP_SEL; LED: Powerline Tx/Rx Link

Pin Number	Pin Name MII 200Mbps	RGMII 500Mbps	Type	Description
21	**GPIO9**	**GPIO3**	I/O	200Mbps: Strap - N/A (Pull-Down); LED: Ethernet Tx/Rx Link 500Mbps: Strap - ISODEF; LED: Ethernet Tx/Rx Link
22	GPIO10	GPIO10	I/O	200 / 500Mbps: Strap - BM_SEL
23	GPIO11	GPIO11	I/O	200Mbps: Strap - N/A 500Mbps: Strap - SPEED_SEL[1]; LED: Power
24	ZC_IN	ZC_IN	I/O	Zero-cross detection signal
25	MDIO	MDIO	I/O	Management Data Interface Data Line
26	MDC	MDC	O_{MAC}/I_{PHY}	Management Data Interface Clock Line
27	RESERVED	RESERVED	-	Reserved pin
28	RESERVED	RESERVED	-	Reserved pin *(pull-down for 200Mbps powerline module)*
29	VSS	VSS	PWR	Ground
30	MRX_D0	RD0	I_{MAC}/O_{PHY}	MII / RGMII: Receive Data Bits (MAC)
31	MRX_D1	RD1	I_{MAC}/O_{PHY}	MII / RGMII: Receive Data Bits (MAC)
32	MRX_D2	RD2	I_{MAC}/O_{PHY}	MII / RGMII: Receive Data Bits (MAC)
33	MRX_D3	RD3	I_{MAC}/O_{PHY}	MII / RGMII: Receive Data Bits (MAC)
34	COL	-	I_{MAC}/O_{PHY}	MII: Collision Detected
35	MRX_CLK	RXC	I_{MAC}/O_{PHY}	MII / RGMII: Receive Clock (MAC)
36	VSS	VSS	Ground	Ground
37	MRX_ERR	-	I_{MAC}/O_{PHY}	MII: Receive Error (MAC)
38	MRX_DV	RX_CTL	I_{MAC}/O_{PHY}	MII: Receive Data Valid (MAC)
39	MTX_D0	TD0	O_{MAC}/I_{PHY}	MII / RGMII: Transmit Data Bits (MAC)
40	MTX_D1	TD1	O_{MAC}/I_{PHY}	MII / RGMII: Transmit Data Bits (MAC)
41	MTX_D2	TD2	O_{MAC}/I_{PHY}	MII / RGMII: Transmit Data Bits (MAC)
42	MTX_D3	TD3	O_{MAC}/I_{PHY}	MII / RGMII: Transmit Data Bits (MAC)
43	CRS	-	I_{MAC}/O_{PHY}	MII: Carrier Sense
44	MTX_CLK	TXC	MII: I_{MAC}/O_{PHY} RGMII: O_{MAC}/I_{PHY}	MII: Transmit Clock (MAC) RGMII: Transmit Clock (MAC)
45	MTX_EN	TX_CTL	O_{MAC}/I_{PHY}	MII: Transmit Enable (MAC) RGMII: Transmit Control Signal (MAC)
46	VSS	VSS	PWR	Ground
47	PHY_RST#	PHY_RST#	O	Reset Ethernet PHY
48	VSS	VSS	PWR	Ground
49	PHY_CLK	PHY_CLK	O	Strap: DUPLEX; 25MHz Clock for Ethernet PHY
50	VSS	VSS	PWR	Ground

The pin-strapping for 200Mbps Powerline modules

Header J1 Pin No	Signal Name	Strap Function	0804-EVALB02 Strap	0804-EVALB02 Strap Description
12	GPIO0	N/A	Pull-Up	N/A
13	GPIO1	N/A	Pull-Up	N/A
14	GPIO2	N/A	Pull-Up	N/A
15	GPIO3	ISODEF	Pull-Down*	MII PHY Mode Isolate Selection: Normal Operation
16	GPIO4	SPEED	Pull-Up	MII PHY Mode Speed Selection: 100Mbps
17	GPIO5	MD_A3	Pull-Up	MII PHY Mode Management Address Selection MD_A[4:3]: 0x08
19	GPIO7	MD_A4	Pull-Down	
22	GPIO10	BM_SEL	Pull-Up*	Boot and SDRAM Configuration Straps [BM_SEL/CFG_SEL]: Load SDRAM configuration and boot code from flash
18	GPIO6	CFG_SEL	Pull-Up*	
20	GPIO8	MP_SEL	Pull-Down*	MII Mode Selection: PHY mode
21	GPIO9	N/A	Pull-Down	Pull down
23	GPIO11	N/A	Pull-Down	N/A
49	PHY_CLK	DUPLEX	Pull-Up	MII PHY Mode Duplex Selection: Full Duplex

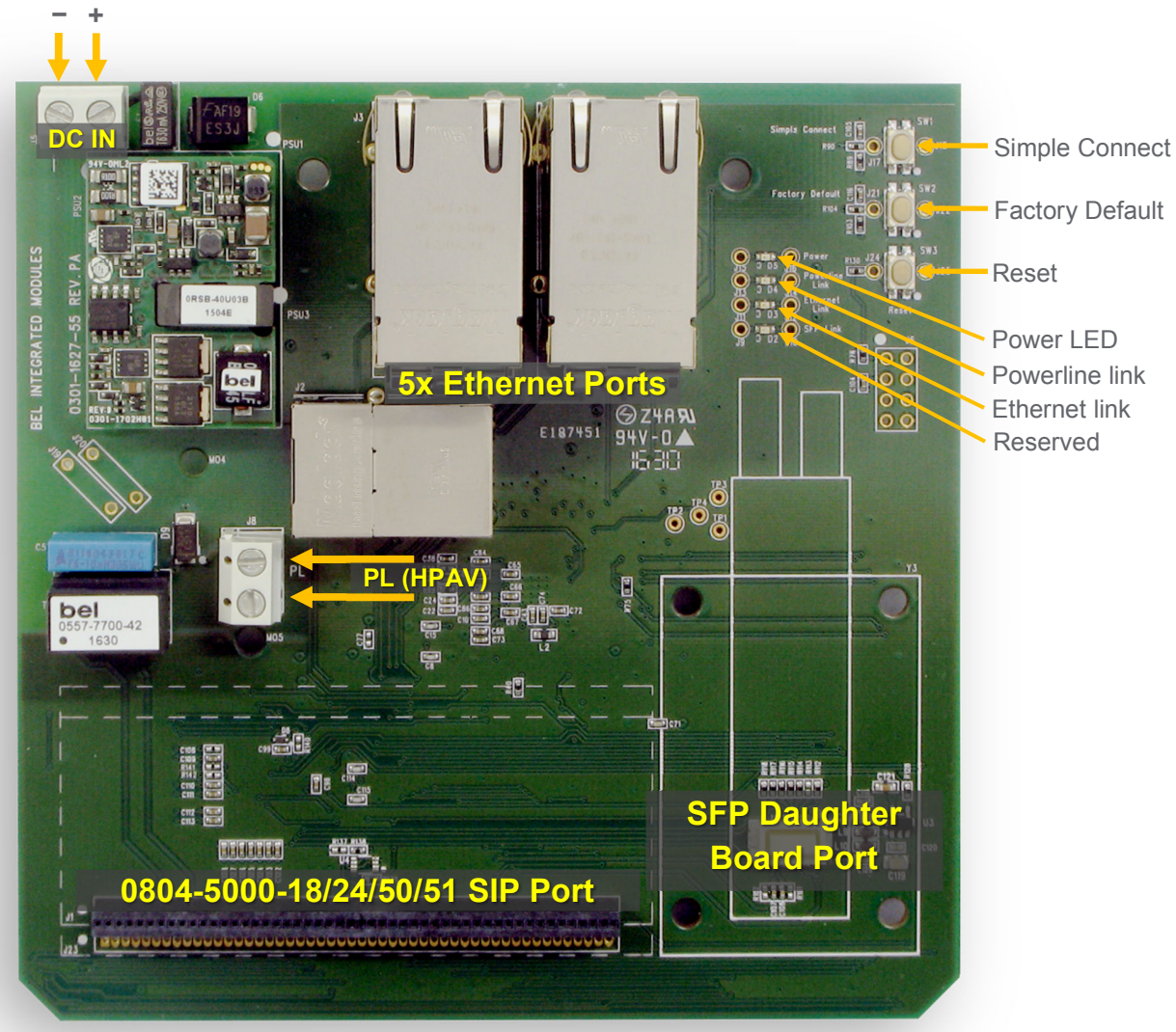
** Powerline module default strapping changed, (configuration forced by 0804-EVALB02)*

The pin-strapping for 500Mbps Powerline modules

Header J1 Pin No	Signal Name	Strap Function	0804-EVALB02 Strap	0804-EVALB02 Strap Description
12	GPIO0	ENET_SEL[0]	Pull-Down*	10/100/1000 RGMII – No delay on Rx clock
13	GPIO1	ENET_SEL[1]	Pull-Down*	
14	GPIO2	ANEN	Pull-Up	PHY Mode Auto-negotiate: Enabled
21	GPIO3	ISODEF	Pull-Down	RGMII PHY Mode Isolate Selection: Normal Operation
16	GPIO4	SPEED_SEL[0]	Pull-Down*	RGMII PHY Mode Speed Selection: 1000Mbps
23	GPIO11	SPEED_SEL[1]	Pull-Up*	
17	GPIO5	MD_A3	Pull-Up	RGMII PHY Mode Management Address Selection MD_A[4:3]: 0x08
19	GPIO7	MD_A4	Pull-Down	
22	GPIO10	BM_SEL	Pull-Up	Boot and DRAM Configuration Straps [BM_SEL/CFG_SEL]: Load DRAM configuration and boot code from flash
18	GPIO6	CFG_SEL	Pull-Up	
20	GPIO8	MP_SEL	Pull-Down*	RGMII Mode Selection: PHY mode
49	PHY_CLK	DUPLEX	Pull-Up	MII PHY Mode Duplex Selection: Full Duplex

** Powerline module default strapping changed, (configuration forced by 0804-EVALB02)*

Evaluation board layout and connections



Getting Started

The evaluation board is able to accept one of the following Bel Powerline Modules via connector J1:

- 0804-5000-18 (MII; 200Mbps)
- 0804-5000-24 (MII; 200Mbps)
- 0804-5000-25 (MII; 200Mbps)
- 0804-5000A50 (RGMII; 500Mbps)
- 0804-5000E50 (RGMII; 500Mbps)

The board requires a 19-75V DC input (NOT MAINS as on previous evaluation boards).

Communications lines can be connected to either a Dry wire, AC, DC separate line via the connector J8.

The on board coupling transformer (Bel 0557-7700-42) provides isolation suitable for AC mains operation.

CAUTION: TO PREVENT AN ELECTRICAL SHOCK, DO NOT SUPPLY HIGH VOLTAGE TO THE BOARD WITHOUT PROTECTIVE COVER

Led indicators are provided to show the status of the evaluation board, the function of these are:

D5 - Power LED: Operates when the board is powered and the DCDC convertor is functioning correctly

D4 - Powerline Link: Operates when a powerline connection is made between two or more powerline modules

D3 - Ethernet Link: Operates when connectivity to an Ethernet host is detected on any of the Ethernet ports

D2 – Reserved: No used.

An Ethernet PHY solution is implemented using one port of a multiport Gigabit Switch (QCA8337N 7-PORT GIGABIT ETHERNET SWITCH). All of the ports can be utilized.

The Evaluation board will function as an Ethernet to Powerline Bridge with no further configuration.

Expected Performance

Performance of the evaluation board will depend on the powerline module used, the packet size and the communications medium attenuation.

Basic testing should be conducted with a cable no shorter than 2 meters. In some cases, a very short cable can cause performance degradation.

For a short “ideal” cable (~2 meters) the following PHY rates should be achievable:

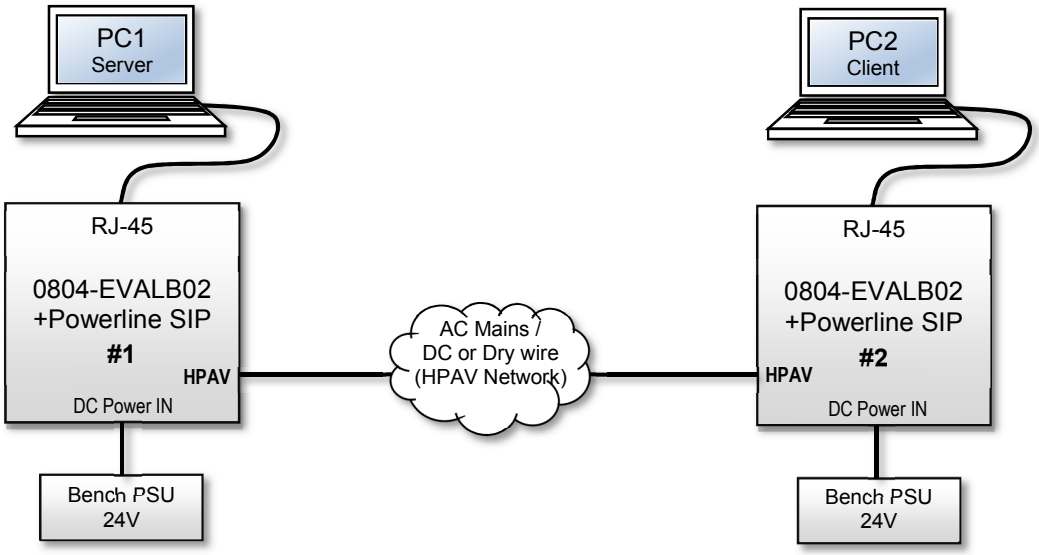
0804-5000-18/-24/-25 (200Mbps technology): PHY rate 130-150Mbps (actual transfer rate ~80Mbps)

0804-5000A50/E50 (500Mbps technology): PHY rate 320-380Mbps (actual transfer rate ~200Mbps)

Open source Qualcomm Atheros Open Powerline Toolkit is freely available on the GitHub web site and can be used to read PHY rate and manage powerline devices.

To test the network performance, you can use commonly used open source network testing tool iPerf, with graphical frontend JPerf.

Before starting the program, please complete the following configuration:



Requirements:

- 2 x PC with network card
- 2 x 0804-EVALB02 Test Fixture
- 2 x 0804-5000-18/-24/-25/A50/E50 Powerline SIP
- 2 x 24V Bench Power Supply
- Cable to create HPAV Network

1. Configure static IP Address:

   PC1:
   - *IP Address:* ***192.168.100.1***
   - *Subnet Mask:* ***255.255.255.0***

   PC2:
   - *IP Address:* ***192.168.100.2***
   - *Subnet Mask:* ***255.255.255.0***

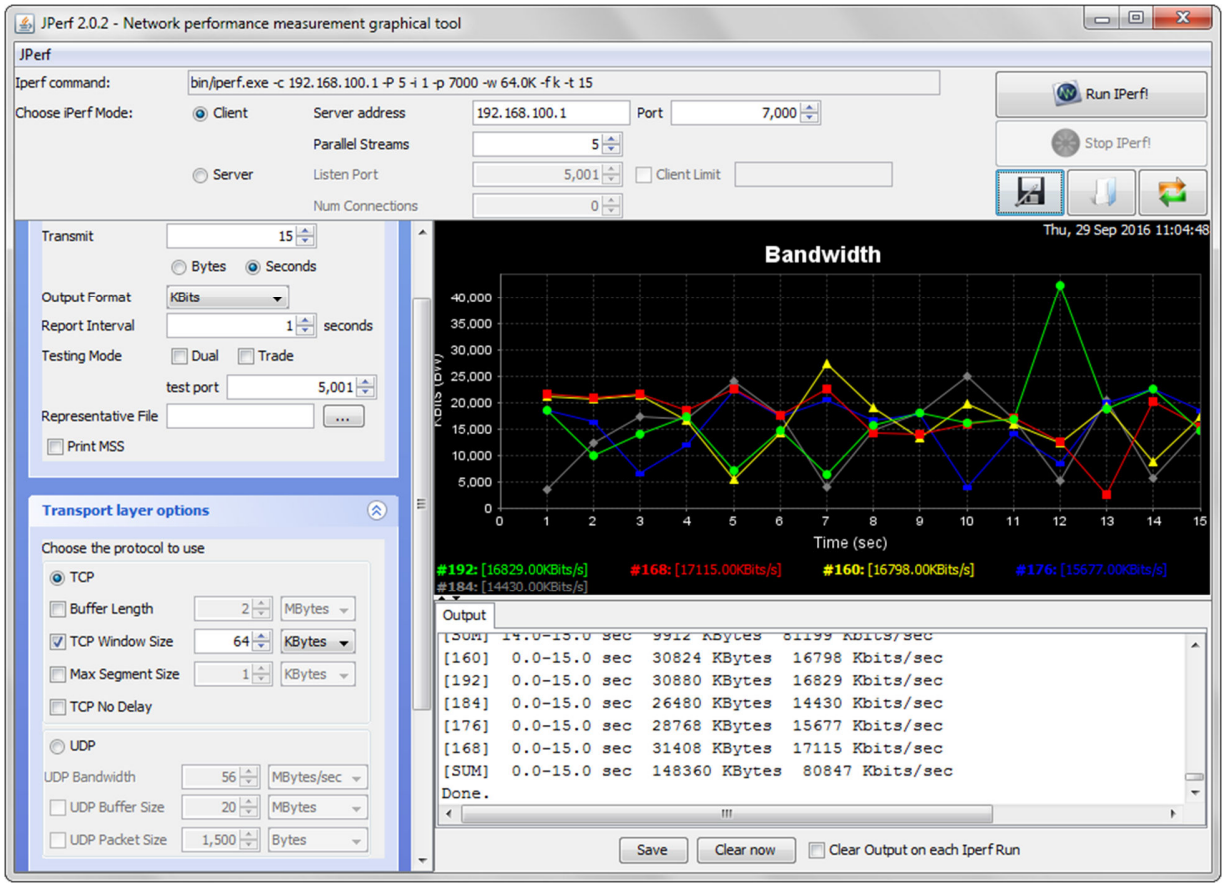
2. Run the "JPerf" and change the program setting:

   PC1:
   - *iPref Mode:* ***Server***
   - *Listen Port:* ***7000***
   - *Num Connections:* ***5***
   - *Protocol:* ***TCP***
   - *TCP Window Size:* ***64 Kbytes***

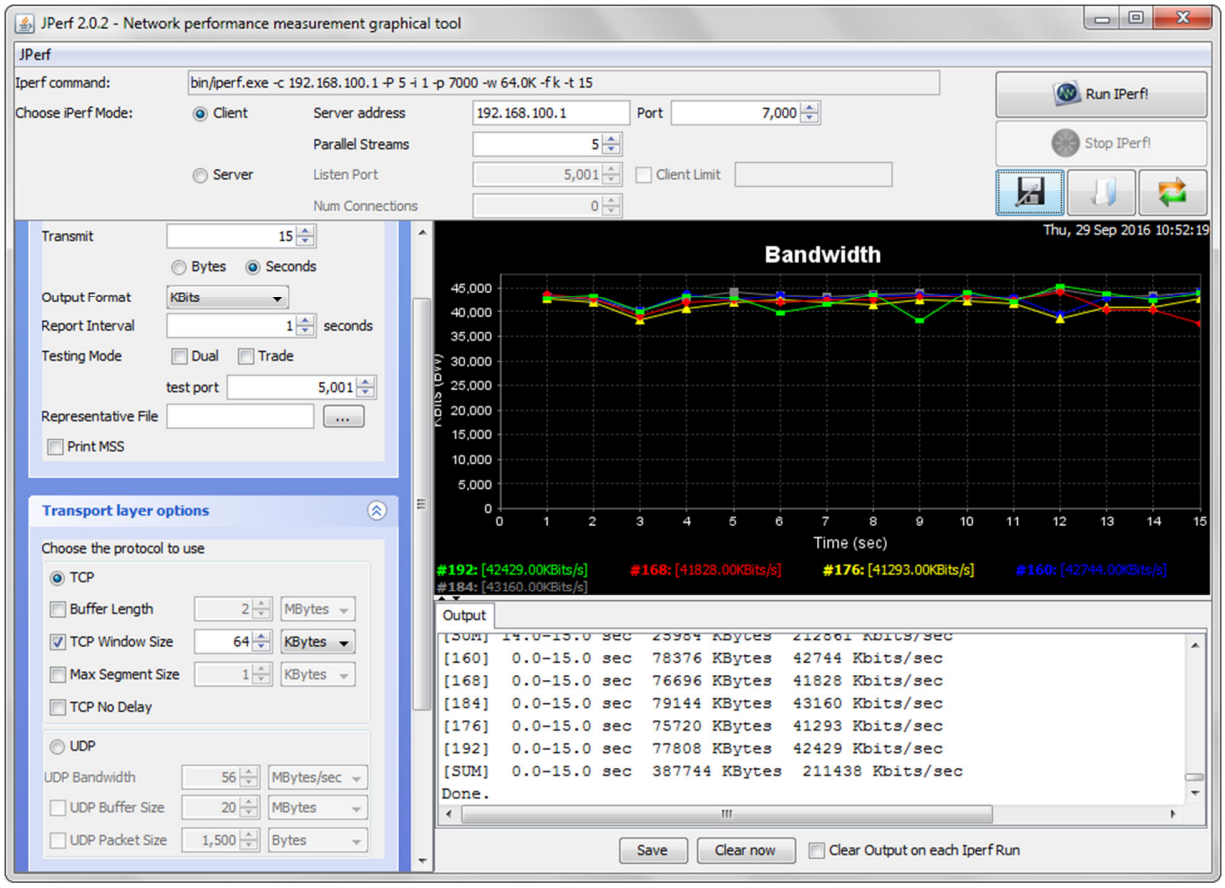
   PC2:
   - *iPref Mode:* ***Client***
   - *Server address:* ***192.168.100.1***

- *Listen Port:* ***7000***
- *Parallel Streams:* ***5***
- *Protocol:* ***TCP***
- *TCP Window Size:* ***64 KBytes***

3. Click "Run IPerf!" button, on PC1 (Server) and PC2 (Client).



Example test results for 0804-5000-24 SIP module



Example test results for 0804-5000E50 SIP module