PFE1300-48-054NA

1300 W, 48 VDC Output

The PFE1300-48-054NA is a 1300 Watt AC to DC power-factor-corrected (PFC) power supply that converts standard AC mains power into a main output of 48 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The PFE1300-48-054NA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

RoHS Compliant

Key Features & Benefits

- Best-in-class, “Platinum” efficiency
- Wide input voltage range: 90-264 VAC
- High Power Density design: 30.25 W/in^3
- Small form factor: 321.5 x 54.5 x 40 mm (12.66 x 2.14 x 1.57 in)
- AC input with power factor correction
- Always-On 16.5 W programmable standby output (3.3/5 V)
- Hot-plug capable
- Parallel operation with active digital current sharing
- I^{2}C communication interface for control, programming and monitoring with Power Management Bus protocol
- Over temperature, output over voltage and over current protection
- 256 Bytes of EEPROM for user information
- 2 Status LEDs: AC OK and DC OK with fault signaling

Applications

- High Performance Servers
- Routers
- Switches

Please read our datasheet & drawing disclaimer here.

1 ORDERING INFORMATION

PFE	1300	-	48	-	054	N	A
Product Family PFE Front-Ends	**Power Level** 1300 W	**Dash**	**V1 Output** 48 V	**Dash**	**Width** 54 mm	**Airflow** N: Normal	**Input** A: AC

*PFE1300-48-054NAS407 has black front panel with white text

2 OVERVIEW

The PFE1300-48-054NA AC/DC power supply is combination of analog and DSP control, highly efficient front-end power supply.

It incorporates resonance-soft-switching technology to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range and minimal linear derating of output power with input voltage and temperature, the PFE1300-48-054NA maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow paths.

The PFC stage guarantee best efficiency and unity power factor over a wide operating range. The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output, with selectable voltage level (3.3/5.0 Volts), provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.
Status information is provided with front-panel LEDs. In addition, the power supply can be controlled and the fan speed set via the I²C bus. The I²C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.

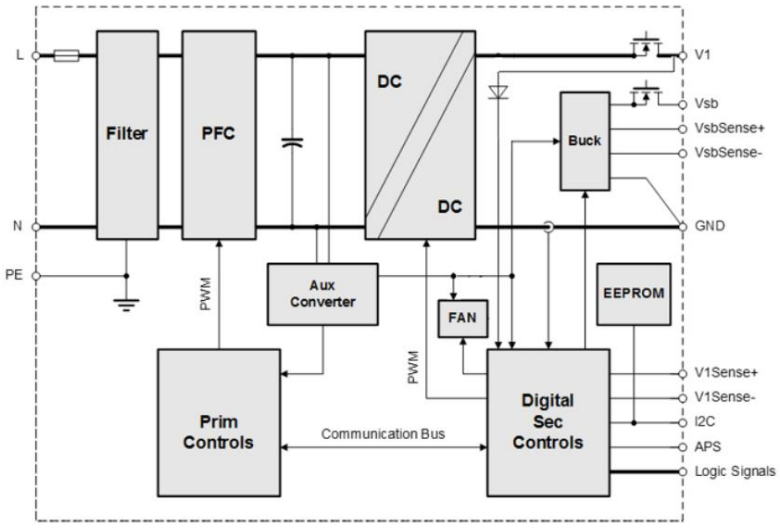

Figure 1. PFE1300-48-054NA Block Diagram

3 ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi max	Maximum Input	Continuous			264	VAC

4 INPUT

General Condition: T_A = 0… 45 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	Nominal Input Voltage		100	230	240	VAC
V_i	Input Voltage Ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	90		264	VAC
$V_{i\,red}$	Derated Input Voltage Range	For North America Application: Derated output (1286 to 1032 W) (see Figure 7A and Figure 26A) For Europe Application Power must be limited to: Power Limit (1286 to 893 W) (see Figure 7B and Figure 26B)	90		145	VAC
$I_{i\,max}$	Max Input Current	Vin =110 VAC / 60 Hz, Full Load			12	A_{rms}
I_{ip}	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, T_{NTC} = 25°C (Figure 4)			50	A_p
F_i	Input Frequency		47	50/60	64	Hz
PF	Power Factor	$V_{i\,nom}$, 50 Hz, > 0.2 $I_{1\,nom}$		0.95		W/VA
$V_{i\,on}$	Turn-on Input Voltage[1)]	Ramping up	85		90	VAC
$V_{i\,off}$	Turn-off Input Voltage[1)]	Ramping down	75		83	VAC
η	Efficiency without Fan	$V_{i\,nom}$, 0.1·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C		87.0		%
		$V_{i\,nom}$, 0.2·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C		92.0		
		$V_{i\,nom}$, 0.5·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C		94.5		
		$V_{i\,nom}$, $I_{x\,nom}$, $V_{x\,nom}$, T_A = 25°C		94.0		
T_{hold}	Hold-up Time	After last AC zero point, V_1 > 42 V, V_{SB} within regulation, V_i = 230 VAC, $P_{x\,nom}$	10			mS

[1)] The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges.

4.1 INPUT FUSE

Quick-acting 16 A input fuses (5 x 20 mm) in series with L line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 3.2 µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current.

NOTE: Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

4.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. An analog controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage.

4.5 EFFICIENCY

High efficiency (see *Figure 2*) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

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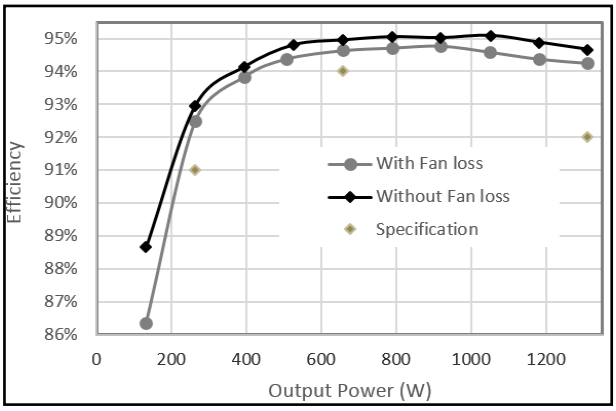

Figure 2. Efficiency vs. Load Current

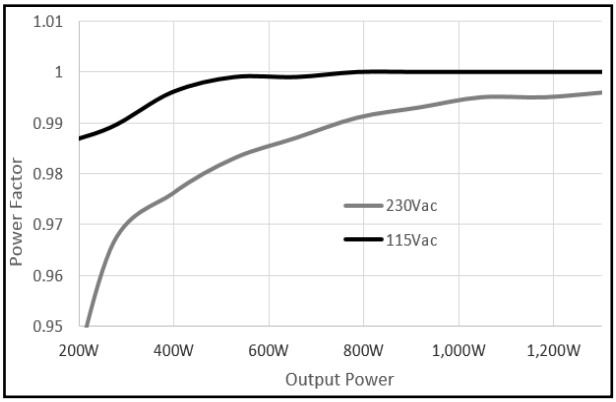

Figure 3. Power Factor vs. Load Current

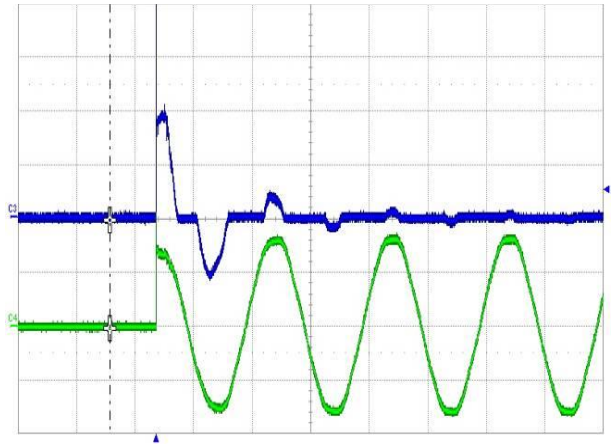

Figure 4. Inrush Current, V_{in} = 230 VAC, 90°
CH4: V_{in} (200 V/div), CH3: I_{in} (20 A/div)

5 OUTPUT

General Condition: T_a = 0 … +45 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
Main Output V_1							
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_{amb} = 25 °C			48.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy			-0.5		+0.5	% $V_{1\ nom}$
$dV_{1\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-1		+1	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	V_i = 48 VDC			1286		W
$I_{1\ nom}$	Nominal Output Current	V_i = 48 VDC			26.8		ADC
$v_{1\ pp}$	Output Ripple Voltage	$V_{1\ nom}$, $I_{1\ nom}$, 20 MHz BW (See Section 5.1)				600	mVpp
$dV_{1\ Load}$	Load Regulation	V_i = $V_{i\ nom}$, 0 - 100 % $I_{1\ nom}$			480		mV
$dV_{1\ Line}$	Line Regulation	V_i = $V_{i\ min}$... $V_{i\ max}$			480		mV
$I_{1\ max}$	Current Limitation PFE1300-48-054NA	V_i > 140 VAC, T_a < 45°C 140 VAC > V_i > 90 VAC, T_a < 45°C For North America Application (see Figure 7A) For Europe Application (see Figure 7B)		28		29.5	ADC
dI_{share}	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%		-3		+3	A
dV_{dyn}	Dynamic Load Regulation	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 - 100% $I_{1\ nom}$, 50 Hz -1 kHz dI_1/dt = 1A/µs, recovery within 1% of $V_{1\ nom\ 1}$		-2.4		2.4	V
T_{rec}	Recovery Time	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 - 100% $I_{1\ nom}$, 50 Hz -1 kHz dI_1/dt = 1A/µs, recovery within 1% of $V_{1\ nom\ 1}$				20	mS
$t_{AC\ V1}$	Start-up Time from AC	V_i = 43.2 VDC				2	sec
$t_{V1\ rise}$	Rise Time	V_i = 10…90% $V_{1\ nom}$			10	200	mS
C_{Load}	Capacitive Loading	T_a = 25°C, CR mode				10000	µF
Standby Output V_{SB}							
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C	VSB_SEL = 1		3.3		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		VSB_SEL = 0		5.0		VDC
			VSB_SEL = 0 / 1	-0.5		+0.5	% V_{1nom}
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-3		+3	% V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power	V_{SB} = 3.3 VDC , normal airflow			16.5		W
		V_{SB} = 5.0 VDC, normal airflow			16.5		W
$I_{SB\ nom}$	Nominal Output Current	V_{SB} = 3.3 VDC, normal airflow			5		ADC
		V_{SB} = 5.0 VDC, normal airflow			3.3		ADC
$V_{SB\ pp}$	Output Ripple Voltage	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW (See Section 5.1)				100	mVpp
dV_{SB}	Droop	0 - 100 % $I_{SB\ nom}$	VSB_SEL = 1		40		mV
			VSB_SEL = 0		26.4		
$I_{SB\ max}$	Current Limitation	VSB_SEL = 1, normal airflow		5.25		6	ADC
		VSB_SEL = 0, normal airflow		3.45		4.3	ADC
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_o/dt = 0.5 A/µs, recovery within 2% of $V_{sb\ nom}$		-5		5	% V_{SBnom}
T_{rec}	Recovery Time					250	µs
$t_{AC\ VSB}$	Start-up Time from AC	V_{SB} = 90% $V_{SB\ nom}$				2	sec
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$ (no capacitive loading)			4	20	mS
C_{Load}	Capacitive Loading	T_{amb} = 25°C, CR mode				10000	µF

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5.1 OUTPUT VOLTAGE RIPPLE

Internal capacitance at the 48 V output (behind the OR-ing circuitry) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors should be added close to the power supply output.

The setup of *Figure 5* has been used to evaluate suitable capacitor types. The capacitor combinations of Table 1 and Table 2 should be used to reduce the output ripple voltage. The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.

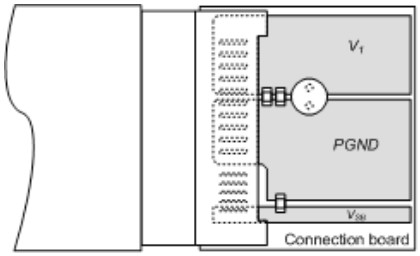


Figure 5. Output Ripple Test Setup

NOTE: Care must be taken when using ceramic capacitors with a total capacitance of 1 µF to 50 µF on output V_1, due to their high quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

External capacitor V1	dV1max	Unit
1 Pc 10 µF / 63 V Electrolytic Capacitor 1 pc 0.1 uF / 100 V ceramic capacitor	550	mVpp
1 Pc 82 µF / 63 V / Conductive Polyer/ø10 x 12.5 mm	400	mVpp

Table 1. Suitable Capacitors for V1

External capacitor VSB	dV1max	Unit
1 Pc 10 µF / 25 V MLCC 1 pc 0.1 uF / 25 V MLCC	80	mVpp
2 Pcs 10 µF / 25 V MLCC 1 pc 0.1 uF / 25 V MLCC	40	mVpp

Table 2. Suitable capacitors for VSB

The output ripple voltage on V_{SB} is influenced by the main output V_1. Evaluating V_{SB} output ripple must be done when maximum load is applied to V_1.

6 PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuses L	Not user accessible, quick-acting (F)		16		A
$V_{1\ OV}$	OV Threshold V_1		57		59.5	VDC
$t_{OV\ V1}$	OV Latch Off Time V_1				1	ms
$V_{SB\ OV}$	OV Threshold V_{SB}		110		120	% V_{SB}
$t_{OV\ VSB}$	OV Latch Off Time V_{SB}				1	ms
$I_{V1\ lim}$	Current Limit V_1 PFE1300-48-054NA	Vi > 145 VAC, Ta < 45°C 145 VAC > Vi > 90 VAC, Ta < 45°C For North America Application (see Figure 7A) For Europe Application (see Figure 7B)	28		29.5	ADC
$I_{V1\ SC}$	Max Short Circuit Current V_1	V_1 < 3 V			50	A
$t_{V1\ SC}$	Short Circuit Regulation Time	V_1 < 3 V, time until I_{V1} is limited to < $I_{V1\ sc}$			2	ms
$t_{V1\ SC\ off}$	Short Circuit Latch Off Time	Time to latch off when in short circuit			200	ms
T_{SD}	Over Temperature On Heat Sinks	Automatic shut-down	100		115	°C

6.1 OVERVOLTAGE PROTECTION

The PFE front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.

6.2 VSB UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_H pin signal status change if the output voltage exceeds ±5% of its nominal voltage. Output undervoltage protection is provided on the standby output only. When V_{SB} falls below 75% of its nominal voltage, the main output V_1 is inhibited.

6.3 CURRENT LIMITATION

6.3.1 MAIN OUTPUT

When main output runs in current limitation mode its output will turn OFF below 2V but will retry to recover every 1s interval. If current limitation mode is still present after the unit retry, output will continuously perform this routine until current is below the current limitation point. The supply will go through soft start every time it retry from current limitation mode.

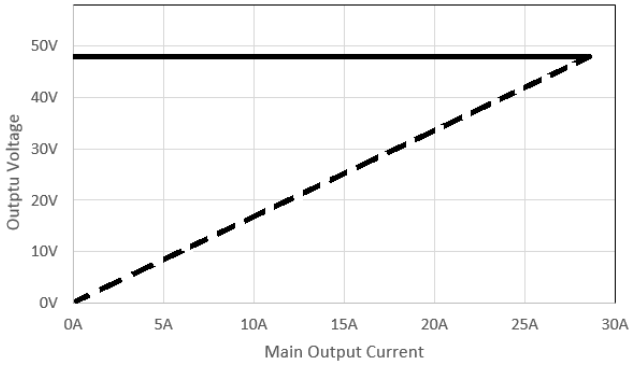
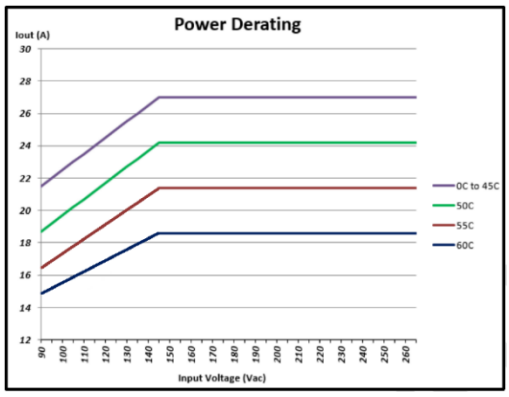
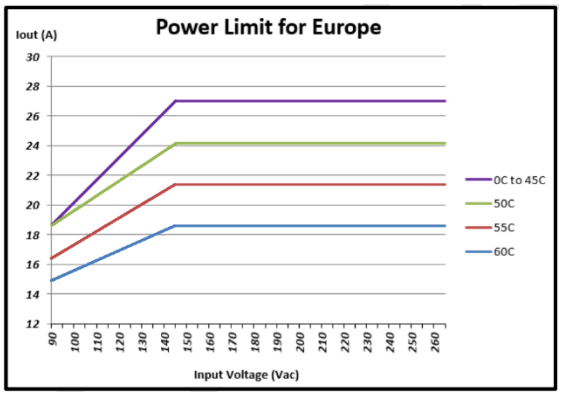


Figure 6. Current Limitation on V_1 (V_i = 230 VAC)

The main output current limitation will decrease if the ambient (inlet) temperature increases above 45°C or if the AC input voltage is too low (see *Figure 7* A or B). Note that the actual current limitation on V_1 will begin at a current level approximately 75 W higher than what is shown in *Figure 7* A or B. (See also Chapter 9 Temperature and Fan Control for additional information.
For European application, derating curve is different from North American application in low line condition as input current limitation for AC input connector is different.)



A. North America



B. Europe

Figure 7.Current on V1 vs. Vin and Ta for PFE1300-48-054NA

(Refer to Safety Installation Instruction for details)

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6.3.2 STANDBY OUTPUT

The standby output exhibits a substantially rectangular output characteristic down to 0 V (no hiccup mode / latch off). If it runs in current limitation and its output voltage drops below the UV threshold, then the main output will be inhibited (standby remains on). The current limitation of the standby output is independent of the AC input voltage.

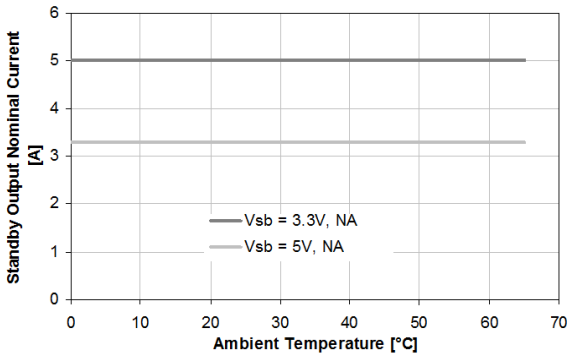

Figure 8. Current Limitation on V_{SB}

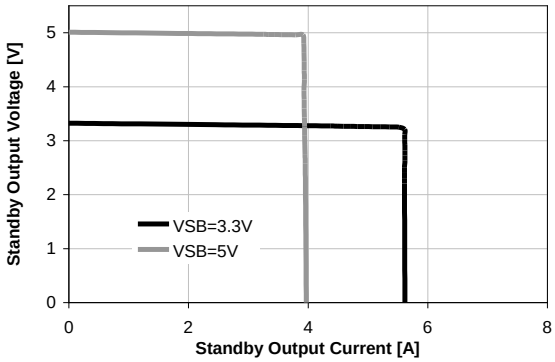

Figure 9. Temperature Derating on V_S

7 MONITORING

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,mon}$	Input RMS Voltage	$V_{i\,min} \le V_i \le V_{i\,max}$	-2.5		+2.5	%
$I_{i\,mon}$	Input RMS Current	$I_i > 4$ A_{rms}	-5		5	%
		$I_i \le 4$ A_{rms}	-0.3		+0.3	A_{rms}
$P_{i\,mon}$	True Input Power	$Po > 260$ W, $V_i = V_{i\,nom}$	-7		+7	%
		$130\ W < Po \le 260$ W, $V_i = V_{i\,nom}$	-25		+25	%
$V_{1\,mon}$	V_1 Voltage		-2		+2	%
$I_{1\,mon}$	V_1 Current	I1 >10 A	-2		+2	%
		I1 ≤ 10 A	-0.3		+0.3	A
$P_{o\,mon}$	Total Output Power	$Po > 260$ W	-5		+5	%
		$Po \le 260$ W	-13		+13	W
$V_{SB\,mon}$	Standby Voltage		-0.1		+0.1	V
$I_{SB\,mon}$	Standby Current	$I_{SB} \le I_{SB\,nom}$	-0.2		+0.2	A

8 SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PSKILL_H / PSON_L / VSB_SEL / HOTSTANDBYEN_H Inputs						
V_{IL}	Input Low Level Voltage		-0.2		0.8	V
V_{IH}	Input High Level Voltage		2.4		3.5	V
$I_{IL, H}$	Maximum Input Sink or Source Current		0		1	mA
$R_{puPSKILL_H}$	Internal Pull Up Resistor on PSKILL_H			10		kΩ
R_{puPSON_L}	Internal Pull Up Resistor on PSON_L			10		kΩ
R_{puVSB_SEL}	Internal Pull Up Resistor on VSB_SEL			10		kΩ
$R_{puHOTSTANDBYEN_H}$	Internal Pull Up Resistor on HOTSTANDBYEN_H			10		kΩ
R_{LOW}	Resistance Pin to SGND for Low Level		0		1	kΩ
R_{HIGH}	Resistance Pin to SGND for High Level		50			kΩ
PWOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 0.5 mA	2.6		3.5	V
R_{puPWOK_H}	Internal Pull Up Resistor on PWOK_H			1		kΩ
ACOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 2 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 50 µA	2.6		3.5	V
R_{puACOK_H}	Internal Pull Up Resistor on ACOK_H			10		kΩ
SMB_ALERT_L Output						
V_{ext}	Maximum External Pull Up Voltage				12	V
V_{OL}	Output Low Level Voltage	I_{source} < 4 mA	0		0.4	V
I_{OH}	Maximum High Level Leakage Current				10	µA
$R_{puSMB_ALERT_L}$	Internal Pull Up Resistor on SMB_ALERT_L			None		kΩ

8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5 V. Therefore all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.

If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in Figure 10 (except for SMB_ALERT_L, ISHARE and I²C pins). This will ensure the pin voltage is not affected by an unpowered power supply.

SMB_ALERT_L pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15 V zener diode as protection device against positive voltage on pins.

ISHARE pins must be interconnected without any additional components. This in-/output is disconnected from internal circuits when the power supply is switched off.

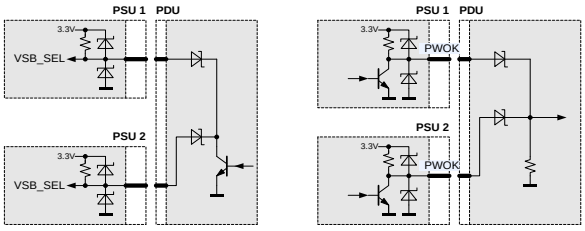

Figure 10. Interconnection of Signal Pins

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8.3 FRONT LEDs

The front-end has 2 front LEDs showing the status of the supply. LED number one is green and indicates AC power is on or off, while LED number two is bi-colored: green and yellow, and indicates DC power presence or fault situations. For the status of the LEDs see *Table 3* lists the different LED status.

OPERATING CONDITION	LED SIGNALING
AC LED	
AC Line within range	Solid Green
AC Line UV condition	Off
DC LED [1)]	
PSON_L High	Blinking Yellow (1:1)
Hot-Standby Mode	Blinking Yellow/Green (1:2)
V_1 or V_{SB} out of regulation	
Over temperature shutdown	
Output over voltage shutdown (V_1 or V_{SB})	Solid Yellow
Output over current shutdown (V_1 or V_{SB})	
Fan error (> 15%)	
Over temperature warning	Blinking Yellow/Green (2:1)
Minor fan regulation error (> 5%, < 15%)	Blinking Yellow/Green (1:1)

1) The order of the criteria in the table corresponds to the testing precedence in the controller.

Table 3. LED Status

8.4 PRESENT_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT_L pin should not exceed 10 mA.

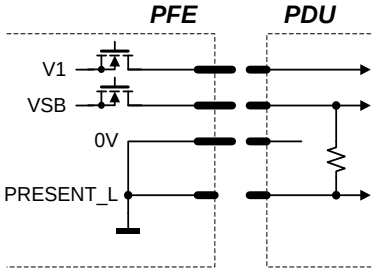

Figure 11. PRESENT_L Signal Pin

8.5 PSKILL_H INPUT

The PSKILL_H input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL_H input state.

8.6 AC TURN-ON / DROP-OUTS / ACOK_H

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON_L signal is pulled low and the AC line is within range. The ACOK_H signal is active-high. The timing diagram is shown in Figure 12 and referenced in *Table 4.*

OPERATING CONDITION		MIN	MAX	UNIT
$t_{AC\ VSB}$	AC Line to 90% V_{VSB}		2	sec
$t_{AC\ V1}$	AC Line to 90% V_1		2	sec
$t_{ACOK_H\ on1}$	ACOK_H signal on delay (start-up)		500	ms
$t_{ACOK_H\ on2}$	ACOK_H signal on delay (dips)		100	ms
$t_{ACOK_H\ off}$	ACOK_H signal off delay		5	ms
$t_{VSB\ V1\ del}$	V_{SB} to V_1 delay	10	500	ms
$t_{V1\ holdup}$	Effective V_1 holdup time	10		ms
$t_{VSB\ holdup}$	Effective V_{SB} holdup time	20		ms
$t_{ACOK_H\ V1}$	ACOK_H to V_1 holdup	7		ms
$t_{ACOK_H\ VSB}$	ACOK_H to V_{SB} holdup	15		ms
$t_{V1\ off}$	Minimum V_1 off time		2000	ms
$t_{VSB\ off}$	Minimum V_{SB} off time		2000	ms

Table 4. AC Turn-on / Dip Timing

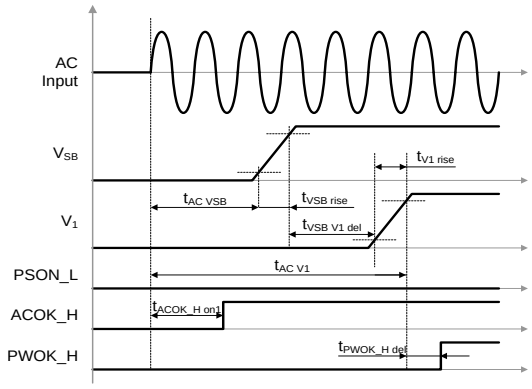

Figure 12. AC Turn-on Timing

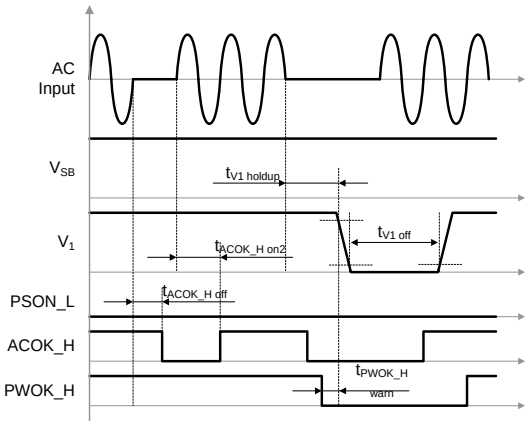

Figure 13. AC Short Dips (below 50 ms)

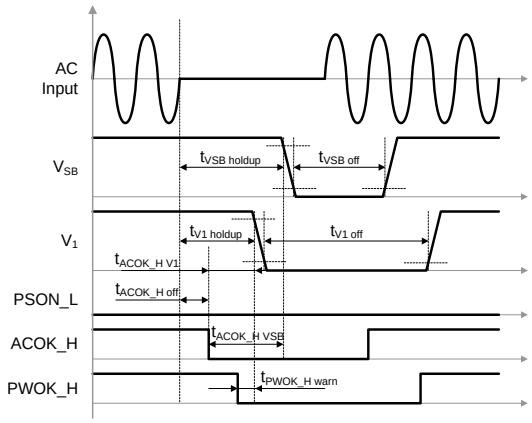

Figure 14. AC Long Dips (above 50 ms)

8.7 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V_1 of the front-end. This active-low pin is also used to clear any latched fault condition. The timing diagram is given in Figure 15 and the parameters in *Table 5*.

OPERATING CONDITION		MIN	MAX	UNIT
$t_{PSON_L\ V1on}$	PSON_L to V_1 delay (on)	10	250	ms
$t_{PSON_L\ V1off}$	PSON_L to V_1 delay (off)	10	250	ms
$t_{PSON_L\ H\ min}$	PSON_L minimum High time	10		ms

Table 5. PSON_L Timing

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8.8 PWOK_H SIGNAL

The PWOK_H is an open drain output with an internal pull-up to 3.3 V indicating whether both V_{SB} is within regulation and V_1 is above 43.2V. The timing diagram is shown in Figure 12 / Figure 15 and referenced in the *Table 6*.

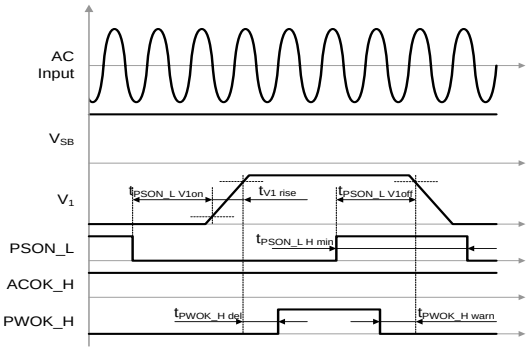

Figure 15. PSON_L turn-on/off Timing

OPERATING CONDITION		MIN	MAX	UNIT
$t_{PWOK_H\ del}$	PWOK_H to V1 delay (on)	100	500	ms
	PWOK_H to V1 delay (off) caused by:			
	PSKILL_H	0	3	ms
	Fan Failure, OT, PSON_L with minimum load	1	100	ms
$t_{PWOK_H\ warn}$*)	ACOK_H	1	30	ms
	UV and OV on VSB	1	30	ms
	OC on V1	1	20	ms
	V1 short	-20	0	
	OV on V1	-50	0	ms

*) A positive value means a warning time, a negative value a delay (after fact).
*) Test must be done with minimum load of 0.5A load on V1 and no capacitive load

Table 6. PWOK_H Timing

8.9 CURRENT SHARE

The PFE front-ends have an active current share scheme implemented for V_1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses a digital bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +1V.

The standby output uses a passive current share method (droop output voltage characteristic).

8.10 SENSE INPUTS

Both main and standby outputs have sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 800 mV and the standby output by 50 mV. Therefore if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.11 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its DC/DC stage. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN_H and the ISHARE pins need to be interconnected. A power supply will only be allowed to enter the hot-standby mode, when the HOTSTANDBYEN_H pin is high, the load current is low (see *Figure 16*) and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I^2C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its active-high HOTSTANDBYEN_H pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

NOTE: The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby model.

Figure 17 shows the achievable power loss savings when using the hot-standby mode operation. A total power loss reduction of 22% is achievable.

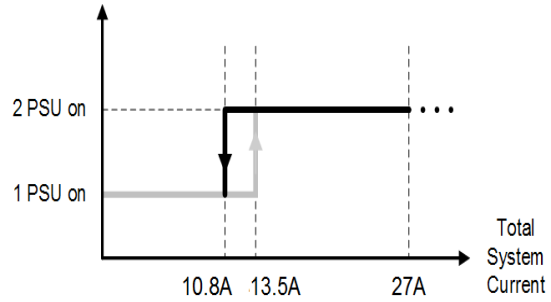

Figure 16. Hot-standby enable/disable current thresholds

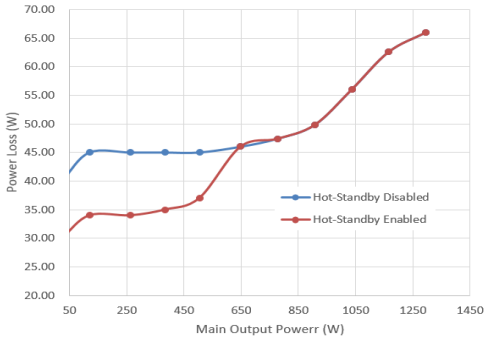

Figure 17. PSU power losses with/without hot-standby mode

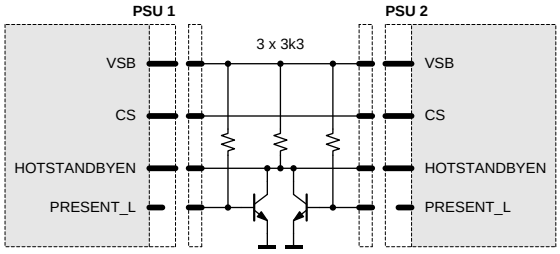

Figure 18. Recommended Hot-standby Configuration

In order to prevent voltage dips when the active power supply is unplugged while the other is in hot-standby mode, it is strongly recommended to add the external circuit as shown in *Figure **18***. If the PRESENT_L pin status needs also to be read by the system controller, it is recommended to exchange the bipolar transistors with small signal MOS transistors or with digital transistors.

8.12 I2C / SMBUS COMMUNICATION

The interface driver in the PFE supply is referenced to the V_1 Return. The PFE supply is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in Table 7 further characterized through:

- There are no internal pull-up resistors
- The SDA/SCL IOs are 3.3 / 5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of > 25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

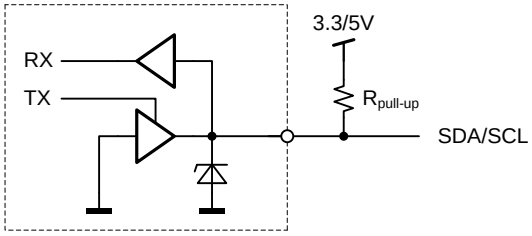

Figure 19. Physical layer of communication interface

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events.

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit). If only VSB is provided, communication is not possible.

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PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	5.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b[1]	300	ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1]	250	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
R_{pu}	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF.

Table 7. I2C / SMBus Specification

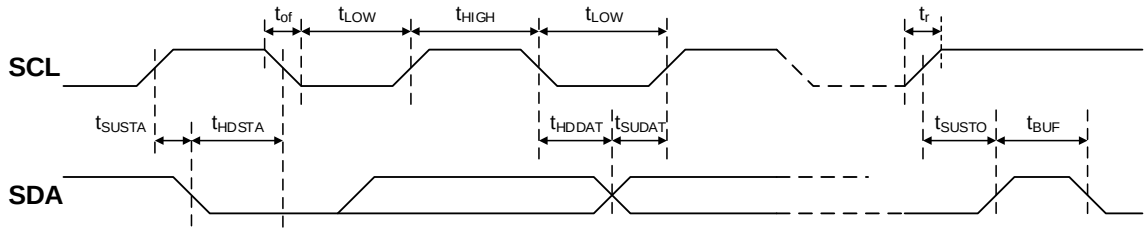


Figure 20. I2C / SMBus Timing

8.13 ADDRESS SELECTION (APS)

The APS pin provides the possibility to select the address by connecting a resistor to V_1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

NOTE:

- If the APS pin is left open, the supply will operate with the Power Management Bus protocol at controller / EEPROM addresses 0xB6 / 0xA6.
- The APS pin is only read at start-up of the power supply. Therefore, it is not possible to change address dynamically

R_{APS} (Ω) [1]	Protocol	I²C Address [2]	
		Controller	EEPROM
820	Power Management Bus	0xB0	0xA0
2700		0xB2	0xA2
5600		0xB4	0xA4
8200		0xB6	0xA6

[1] E12 resistor values, use max 5% resistors, see also Figure 21.
[2] The LSB of the address byte is the R/W bit.

Table 8. Address and Protocol Encoding

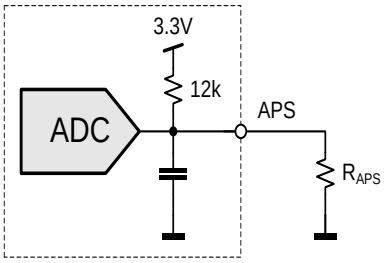


Figure 21. I2C address and Protocol Setting

8.14 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see Figure 22). An I²C driver device assures logic level shifting (3.3 / 5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I²C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

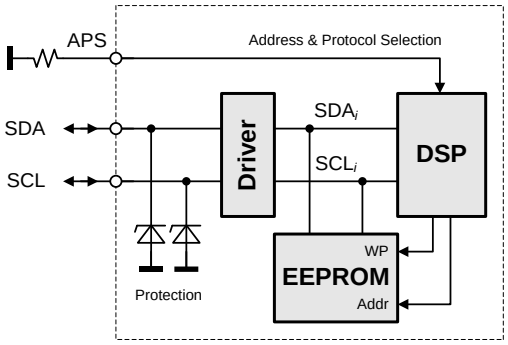


Figure 22. I2C Bus to DSP and EEPROM

8.15 EEPROM PROTOCOL

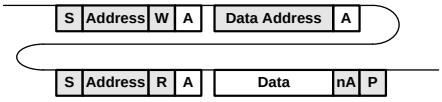
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5 mS of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



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8.16 POWER MANAGEMENT BUS PROTOCOL

The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

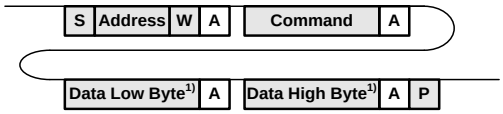
Power Management Bus command codes are not register addresses. They describe a specific command to be executed.

The PFE1300-48-054NA supply supports the following basic command structures:

- Clock stretching limited to 1 mS
- SCL low time-out of > 25 mS with recovery within 10 mS
- Recognized any time Start/Stop bus conditions

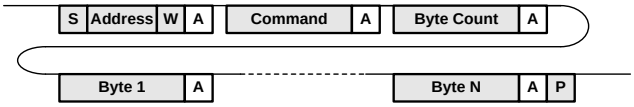
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



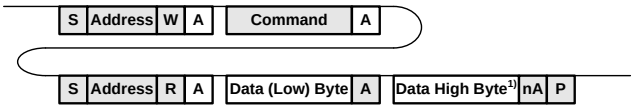
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PFE1300-48-054NA Communication Manual for further information.



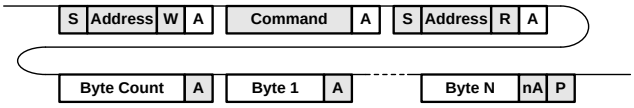
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See PFE1300-48-054NA Communication Manual BCA.00006 for further information.



8.17 GRAPHICAL USER INTERFACE

Bel Power Solutions provides with its “Bel Power Solutions I²C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFE1300-48-054NA Front-End.

The utility can be downloaded on: belfuse.com/power-solutions and supports Power Management Bus protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the PFE1300-48-054NA BOARD Evaluation Kit it is also possible to control the PSON_L pin(s) of the power supply.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

NOTE: The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

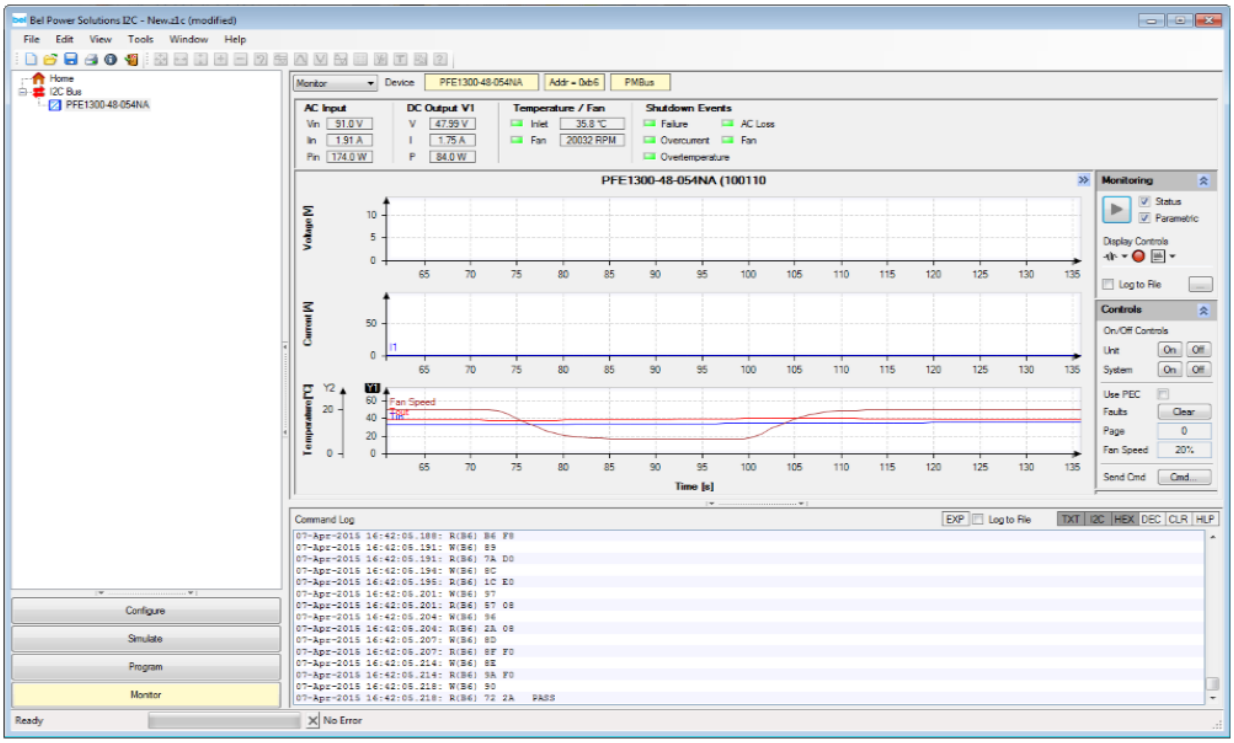


Figure 23. Monitoring Dialog of the I2C Utility

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9 TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFE1300-48-054NA is provided with a normal airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. PFE supplies have been designed for horizontal operation.
The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.
For the normal airflow version additional constraints apply because of the AC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the AC-inlet.
The IEC connector on the unit is rated 120°C. The input power is derated to ensure sufficient thermal margin is allotted to the mating connector. See Figure 26A or 26B.

NOTE: It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

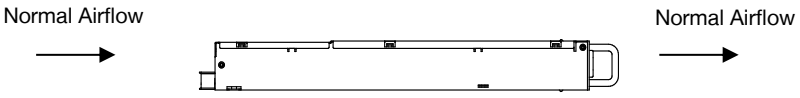


Figure 24. Airflow Direction

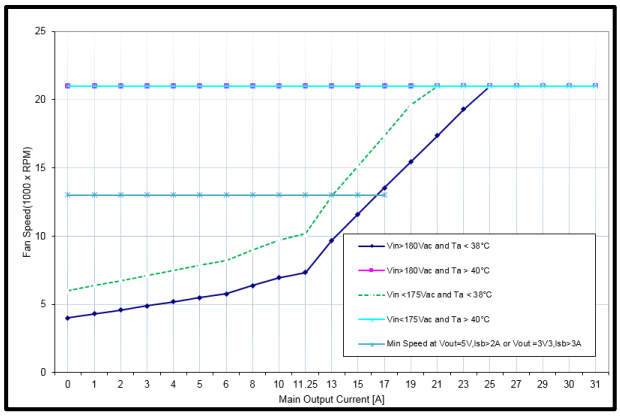
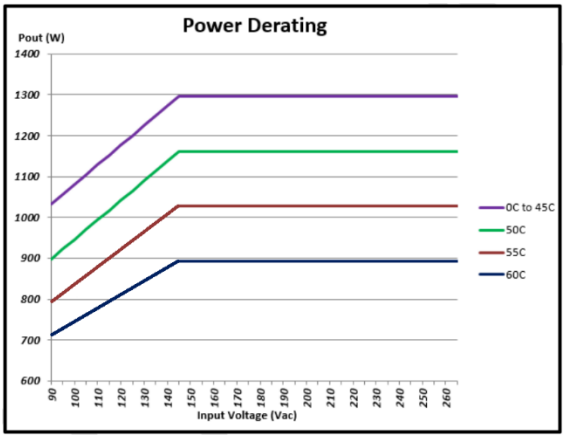
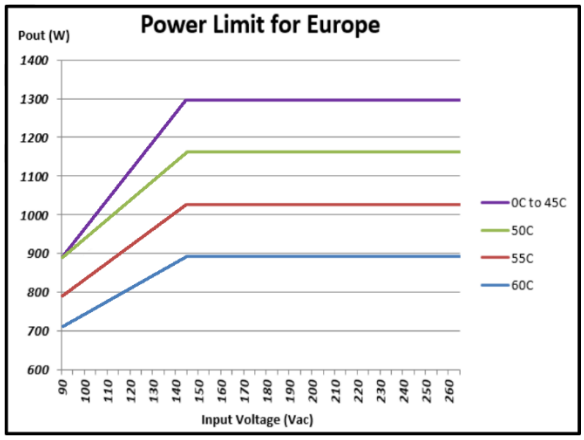


Figure 25. Fan Speed vs Main Output Load for PFE1300-48-054NA



A.



B. Europe

Figure 26. Power Derating for PFE1300-48-054NA
(Refer to Safety Installation Instruction for details)

10 ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	B
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	B
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation, 10 kHz…2 GHz	A
Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute	B
Surge	IEC / EN 61000-4-5 Line to earth: level 3, ±2 kV Line to line: level 2, ±1 kV	V_{SB}: A, V_1: B[1] A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A
Voltage Dips and Interruptions	IEC/EN 61000-4-11 1: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 10 mS 2: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 20 mS 3: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration > 20 mS	A V_{SB}: A, V_1: B V_{SB}, V_1: B

[1] V_1 drops to 90 … 97% $V_{1\ nom}$ for 3 mS.

10.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single unit	Class A 6 dB margin
	EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, 2 units in rack system	Class A 6 dB margin
Radiated Emission	EN55022 / CISPR 22: 30 MHz … 1 GHz, QP, single unit	Class A 6 dB margin
	EN55022 / CISPR 22: 30 MHz … 1 GHz, QP, 2 units in rack system	Class A 6 dB margin
Harmonic Emissions	IEC61000-3-2, Vin = 115 VAC / 60 Hz, & Vin = 230 VAC / 50 Hz, 100% Load	Class A
AC Flicker	IEC61000-3-3, Vin = 230 VAC / 50 Hz, 100% Load	Pass

11 SAFETY / APPROVALS

Maximum electric strength testing is performed according to UL/CSA 62368-1 and EN/IEC 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Agency Approvals	Approved to latest edition of the following standards: UL/CSA 62368-1 and EN/IEC 62368-1		Approved by independent body (see CE Declaration)		
Isolation Strength	Input (L/N) to case (PE)		Basic		
	Input (L/N) to output		Reinforced		
	Output to case (PE)		Functional		
Electrical Strength Test	Input to case	2500			VDC
	Input to output	4000			VDC

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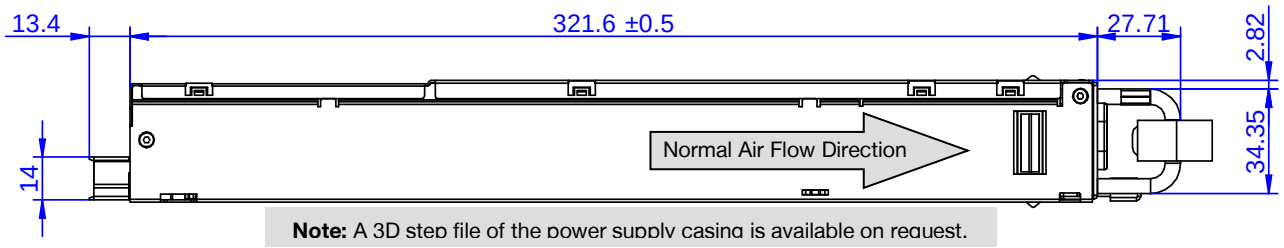
12 ENVIRONMENTAL

PARAMETER		CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNIT
T_A	Ambient temperature	$V_{i\,min}$ to $V_{i\,max}$, $I_{1\,nom}$, $I_{SB\,nom}$	0		+45	°C
T_{Aext}	**Extended temp range**	***North America Application:***				
		Full Power 1286W @ V_i 145-264 VAC	0		+45	°C
		Derated power (1032 to 1286 W) @ V_i 90-145 VAC	0		+45	
		Derated power (893 to 1162 W) @ V_i 90-145 VAC	+45		+50	
		Derated power (792 to 1028 W) @ V_i 90-145 VAC	+50		+55	
		Derated power (716 to 893 W) @ V_i 90-145 VAC	+55		+60	
		(see Figure 7A and Figure 26 A)				
		Europe Application Power must be limited to:				
		Full Power 1286W @ Vi 145-264 VAC	0		+45	°C
		Power Limit (893 to 1286 W) @ V_i 90-145 VAC	0		+45	
		Power Limit (893 to 1162 W) @ V_i 90-145 VAC	+45		+50	
		Power Limit (792 to 1028 W) @ V_i 90-145 VAC	+50		+55	
		Power Limit (716 to 893 W) @ V_i 90-145 VAC	+55		+60	
		(see Figure 7B and Figure 26B)				
T_S	Storage temperature	Non-operational	-20		+70	°C
N_a	Audible noise	$V_{i\,nom}$, 50% $I_{o\,nom}$, T_A = 25 °C		46		dBA
	Altitude	Operational, above Sea Level			10,000	feet
					3048	m

13 MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		54.5		mm
		Height		40.0		
		Depth		321.5		
M	Weight			1.09		kg



Note: A 3D step file of the power supply casing is available on request.

Figure 27. Side View 1

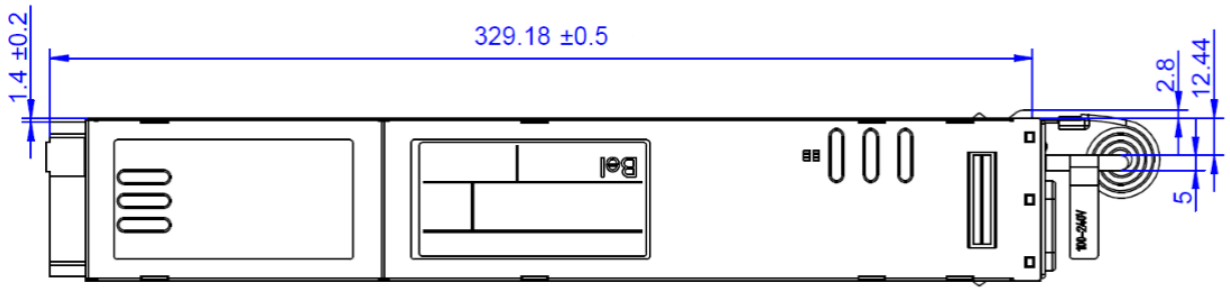


Figure 28. Top View

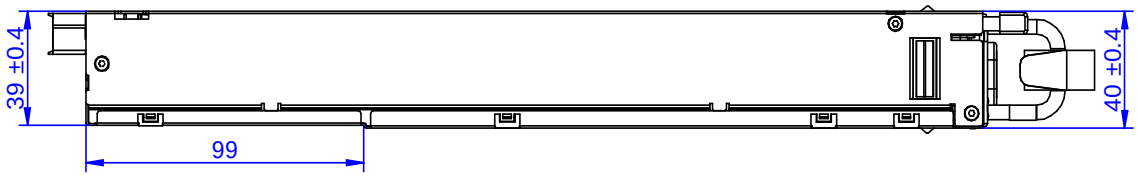


Figure 29. Side View 2

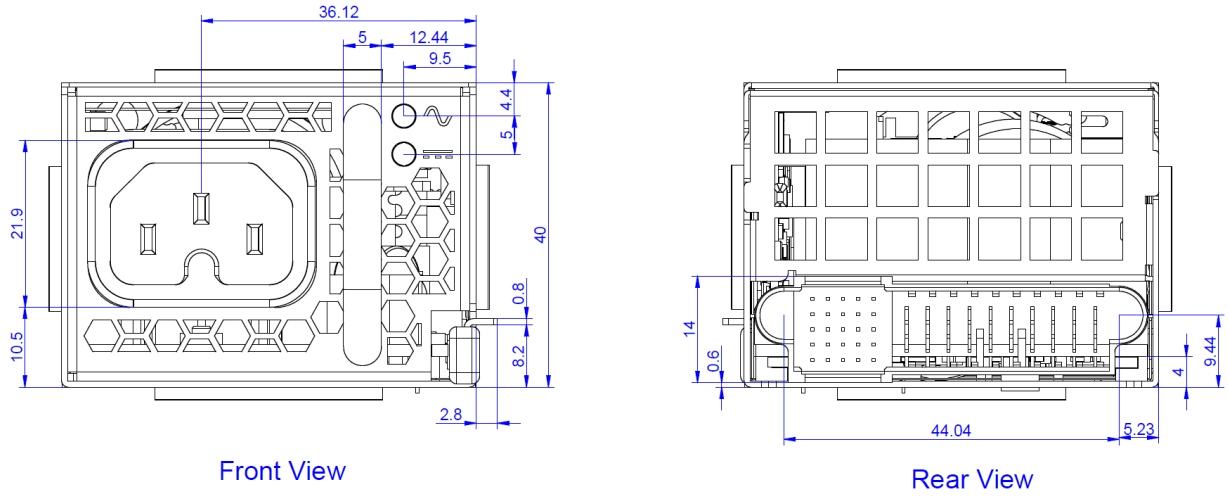


Figure 30. Front and Rear View

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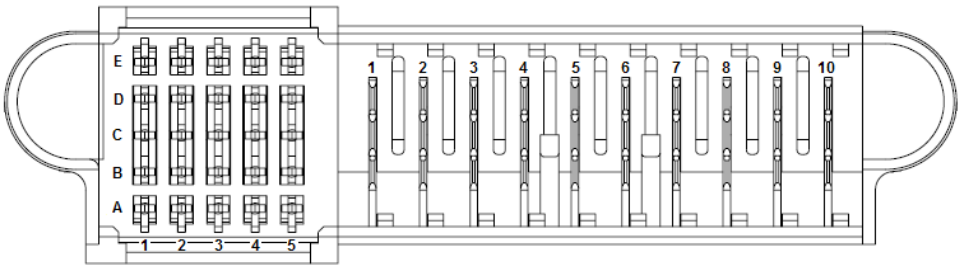
14 CONNECTIONS

AC Input:
Unit: IEC320 Type C16 AC socket.
Counterpart: IEC320 C15 power cord

DC Output:



Power Supply Connector: Tyco Electronics P/N 1926736-3 or FCI connector 10133129-002LF or equivalent
(NOTE: Column 5 is recessed (short pins))
Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

PIN	NAME	DESCRIPTION
Output		
6, 7, 8, 9, 10	V1	+48 VDC main output
1, 2, 3, 4, 5	PGND	Power ground (return)
Control Pins		
A1	VSB	Standby positive output (+3.3/5 V)
B1	VSB	Standby positive output (+3.3/5 V)
C1	VSB	Standby positive output (+3.3/5 V)
D1	VSB	Standby positive output (+3.3/5 V)
E1	VSB	Standby positive output (+3.3/5 V)
A2	SGND	Signal ground (return)
B2	SGND	Signal ground (return)
C2	HOTSTANDBYEN_H	Hot standby enable signal: active-high
D2	VSB_SENSE_R	Standby output negative sense
E2	VSB_SENSE	Standby output positive sense
A3	APS	I²C address and protocol selection (select by a pull down resistor)
B3	N/C	Reserved
C3	SDA	I²C data signal line
D3	V1_SENSE_R	Main output negative sense
E3	V1_SENSE	Main output positive sense
A4	SCL	I²C clock signal line
B4	N/C	Reserved
C4	SMB_ALERT_L	SMB Alert signal output: active-low
D4	PSON_L	Power supply on input (connect to A2/B2 to turn unit on): active-lo
E4	ACOK_H	AC input OK signal: active-high
A5	PSKILL_H	Power supply kill (lagging pin): active-high
B5	ISHARE	Current share bus (lagging pin)
C5	PWOK_H	Power OK signal output (lagging pin): active-high
D5	VSB_SEL	Standby voltage selection (lagging pin)
E5	PRESENT_L	Power supply present (lagging pin): active-low

15 ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	Bel Power Solutions I²C Utility Windows XP/Vista/7 compatible GUI to program, control and monitor PFE Front-Ends (and other I²C units)	N/A	belfuse.com/power-solutions
	Dual Connector Board Connector board to operate 2 PFE units in parallel. Includes an on-board USB to I²C converter (Bel Power Solutions I²C Utility as desktop software)	VRA.00389.0	belfuse.com/power-solutions

For more information on these products consult: tech.support@psbel.com

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TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

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