PET750-12-050xA

AC-DC Front-End Power Supply

The **PET750-12-050** is a 759 Watts, 1U form factor power supply module with Active PFC (Power Factor Correction). It converts standard AC mains power into a main output of 12V for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.
The PET750-12-050 meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- Best-in-Class, 80 PLUS Certified “Platinum” Efficiency
- Wide Input Voltage Range 90-264 VAC
- AC Input with Power Factor Correction
- Always-On 15 W Standby Output (5 V/3 A)
- Hot-Plug Capability
- Parallel Operation with Active Current Sharing
- DC-DC Digital Controls for Improved Performance
- High Density Design 20.5 W/in^3
- Small Form Factor 300 x 50.5 x 40 mm (11.81 x 1.99 x 1.57 in)
- Power Management Bus Communications Protocol for Control, Programming and Monitoring
- Over Temperature, Output Over Voltage and Over Current Protection
- One DC OK Signaling Status LED

Applications

- Networking Switches
- High Performance Servers
- Routers

Please read our datasheet & drawing disclaimer here.

1. ORDERING INFORMATION

PET	750	-	12	-	050	x	A
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PET Front-Ends	750 W		12 V		50 mm	N: Normal R: Reverse	A: AC

MODEL	OUTPUT VOLTAGE	MAX LOAD CONVECTION [1]	MAX LOAD 300 LFM [1,2]	MINIMUM LOAD	RIPPLE & NOISE [3]	CONNECTOR	TOTAL REGULATION
PET750-12-050NA	12 VDC	62 A	62 A	0 A	1%	Card edger	± 2.5%
PET750-12-050RA	12 VDC	62 A	62 A	0 A	1%	Card edger	± 2.5%

2. OVERVIEW

The PET750-12-050 AC-DC power supply is a mainly DSP controlled, highly efficient front-end. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range. PET750-12-050 maximizes power availability in demanding server, network switch, and router applications. The front-end is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is controlled using interleaved Critical mode to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant technology in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output, provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

NOTE: Output GND is connected to chassis in power supply.

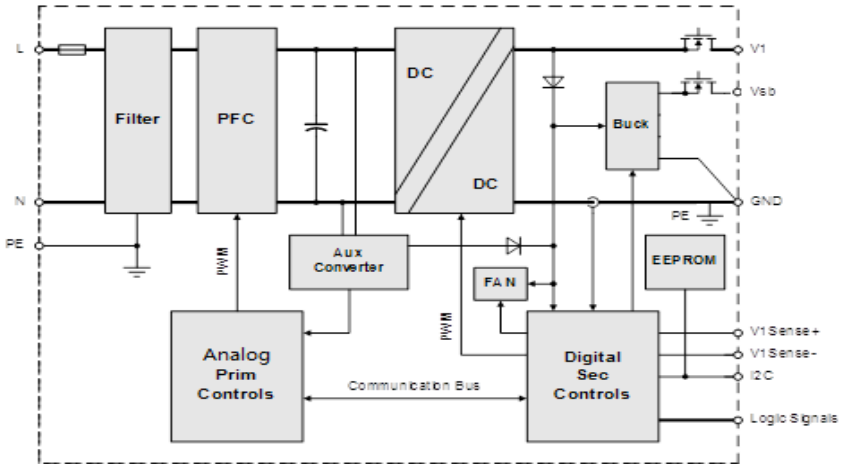

Figure 1. PET750-12-050 Block Diagram

3. INPUT

General Condition: Tamb = -25 to 70°C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ nom}$	Nominal Input Voltage		100		240	VAC
V_i	Input Voltage Ranges	Normal operating ($V_{i\ min}$ to $V_{i\ max}$)	90		264	VAC
$I_{i\ max}$	Max Input Current				10	A_{rms}
$I_{i\ p}$	Inrush Current Limitation[1] (Cold start)	$V_{i\ min}$ to $V_{i\ max}$, 90°(Phase), T_{NTC} = 25°C			50	A_p
F_i	Input Frequency		47	50/60	63	Hz
PF	Power Factor	$V_{i\ nom}$, 50Hz, $I_{1\ nom}$	0.95			W/VA
$V_{i\ on}$	Turn-on Input Voltage	Brown in	80	85	90	VAC
$V_{i\ off}$	Turn-off Input Voltage	Brown out	75	80	85	VAC
η	Efficiency without Fan	$V_{i\ nom}$, 0.2·$I_{x\ nom}$, $V_{x\ nom}$, T_A = 25°C		92		%
		$V_{i\ nom}$, 0.5·$I_{x\ nom}$, $V_{x\ nom}$, T_A = 25°C		94.3		
		$V_{i\ nom}$, $I_{x\ nom}$, $V_{x\ nom}$, T_A = 25°C		93.5		
T_{hold}	Hold-up Time	After last AC zero point, V_1 > 10.8 V, V_{SB} within regulation, V_i = 230 VAC, $P_{x\ nom}$X60%		24		ms

[1] The charging currents for X capacitors are not considered as in-rush current

3.1 EFFICIENCY

The power supply module efficiency should meet at least 80Plus Platinum rating, the efficiency should be measured at 230 VAC and with external fan power according to 80Plus efficiency measurement specifications.

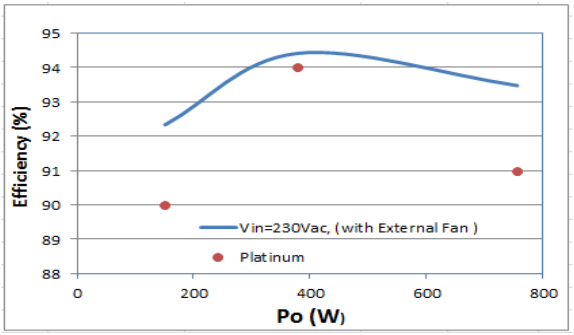

Figure 2. Efficiency vs. Load current (ratio metric loading)

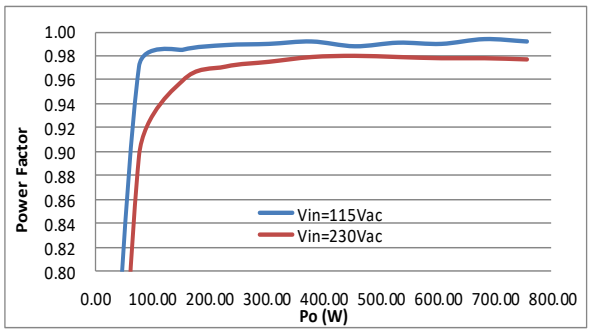

Figure 3. Power factor vs. Load current

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4. OUTPUT

5.1 MAIN OUTPUT V_1

General Condition: Ta = 0 … +50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 ·$I_{1\ nom}$, T_{amb} = 25 °C		12.0		VDC
$V_{1\ set}$			-0.5		+0.5	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	V_1 = 12V		744		W
$I_{1\ nom}$	Nominal Output Current[3]	Input voltage 165-264 VAC		62		ADC
		Input voltage 90-164 VAC		43		
$V_{1\ pp}$	Output Ripple Voltage[2]	$V_{1\ nom}$, $I_{1\ nom}$, 20MHz BW (See Section 4.1)			120	mVpp
$dV_{1\ Load}$	Load Regulation	V_i = $V_{i\ nom}$, 0 - 100 % $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-2		+2	% $V_{1\ nom}$
$dV_{1\ Line}$	Line Regulation	V_i =$V_{i\ min}$...$V_{i\ max}$, $T_{a\ min}$ to $T_{a\ max}$	-1		+1	% $V_{1\ nom}$
dI_{share}	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%	-5		+5	ADC
dV_{dyn}	Dynamic Load Regulation	ΔI1 = 50% $I_{1\ nom}$, I1 = 5 … 100% $I_{1\ nom}$, dI1/dt = 1A/µs, recovery within 1% of V1 nom	-5		+5	% $V_{1\ nom}$
T_{rec}	Recovery Time				2	ms
$C_{V1\ Load}$	Capacitive Loading	T_a = 25°C			11000	µF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 ·$I_{SB\ nom}$, T_{amb} = 25°C		5.0		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-0.5		+0.5	%V_{1nom}
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-1.5		+1.5	%V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power			15		W
$I_{SB\ nom}$	Nominal Output Current			3		ADC
$V_{SB\ pp}$	Output Ripple Voltage[2]	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW			50	mVpp
dV_{SB}	Droop	0 - 100 % $I_{SB\ nom}$		90		mV
dV_{SBdyn}	Dynamic Load Regulation	ΔI$_{SB}$ = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI$_{SB}$/dt = 0.5 A/µS, recovery within 1% of $V_{SB\ nom}$	-3		+3	%V_{SBnom}
T_{rec}	Recovery Time				250	µs
$C_{VSB\ load}$	Capacitive Loading for 5V_{SB}	T_{amb} = 25°C			350	µF

[2] The output noise and ripple measurement was made with 20MHz bandwidth using a 6-inch twisted pair, terminated with a 10 uF tantalum capacitor in parallel with a 0.1uF ceramic capacitor. The output ripple voltage on VSB is influenced by the main output V1. Evaluating VSB output ripple must be done when maximum load is applied to V1.

[3] The output power derating at low line only for PET750-12-050NA, for RA model no derating required.

5. PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuse (Line)	Not user accessible, quick-acting (F)		12.5		A_{rms}
$V_{1\ OV}$	OV Threshold V1	Refer to section 5.1	13.3		14.5	VDC
$V_{1\ UV}$	UV Threshold V1	unlatch unit by disconnecting AC or by toggling the PS_ON signal		10.5		VDC
$I_{V1\ lim}$	Current Limit V1	Refer to section 5.3	68		78	ADC
$I_{V1\ SC}$	Max Short Circuit Current V1	V1 < 3V (unlatch unit by disconnecting AC or by toggling the PS_ON signal)		250		ADC
$V_{SB\ OV}$	OV Threshold V_{SB}	Unlatch unit by disconnecting AC	5.75		6.5	VDC
$I_{SB\ lim}$	Current Limit V_{SB}	Hiccup mode	3.5		4.5	ADC
T_{SD}	Over Temperature on Inlet	Automatic recovery with Hysteresis for NA model		70		°C
	Over Temperature Oring	Automatic recovery with Hysteresis for NA model		100		°C
T_{SD}	Over Temperature on Inlet	Automatic recovery with Hysteresis for RA model		60		°C
	Over Temperature Oring	Automatic recovery with Hysteresis for RA model		110		°C

5.1 OVERVOLTAGE PROTECTION

The PET front-ends provide a fixed threshold over voltage protection implemented with a HW comparator. Once an over voltage condition has been triggered, the power supply will shut down and latch the fault condition. The latch can be unlatched by disconnecting the supply from the AC mains or by toggling the PS_ON input.

5.2 UNDERVOLTAGE DETECTION

The main output will latch off when V1 drop to below the UV threshold. The latch can be unlatched by disconnecting the supply from the AC mains or by toggling the PS_ON input. The main output will shut down if the VSB voltage drop below 4 V and recover when VSB voltage higher than 4.3 V.

5.3 CURRENT LIMITATION

MAIN OUTPUT

The main output exhibits a substantially rectangular output characteristic controlled by a software feedback loop. If it runs in current limitation and its voltage drops below ~10.8 VDC for more than 10 ms, the output will latch off (standby remains on).

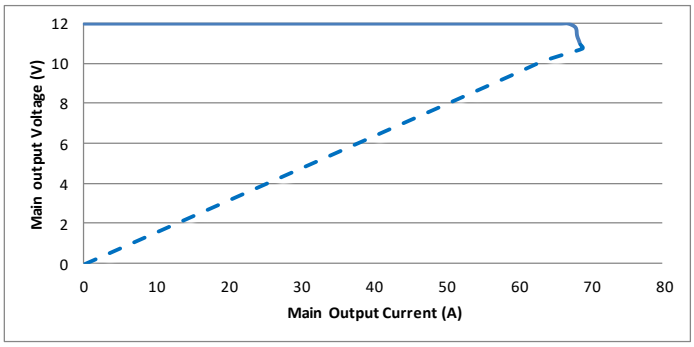

Figure 4. Current Limitation on V1 (Vi = 230 VAC)

A second current limitation circuit on V1 will immediately switch off the main output if the output current increases beyond the peak current trip point. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PS_ON input.

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STANDBY OUTPUT

The standby output exhibits a substantially rectangular output characteristic down to 0V (hiccup mode). If it runs in current Limitation and its output voltage drops to 0 V, then the main output will be inhibited.

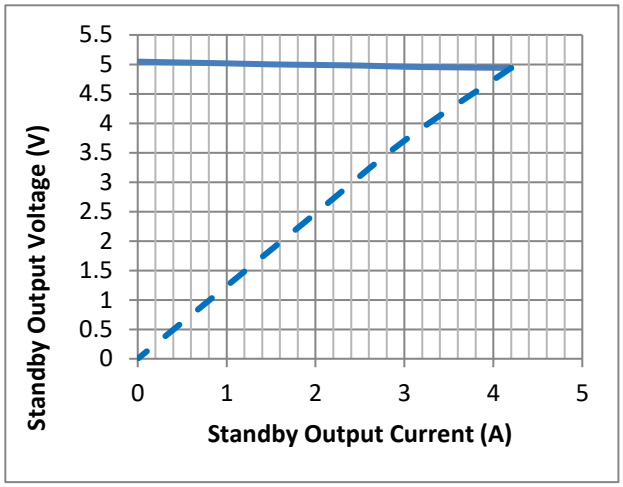

Figure 5. Current limitation on VSB

6. TIMING SPECIFICATION

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Tv1out_rise	Output voltage rise time for main output		20	ms
TV_{SB}out_rise	Output voltage rise time for the 5 V_{SB} output		25	ms
Tsb_on-delay	Delay from AC being applied to 5 V_{SB} voltage being within regulation.		1500	ms
Tac_on-delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all output voltage stays within regulation after loss of AC tested at 60% of maximum load.	17	24	ms
Tpwok_holdup	Delay from loss of AC de-assertion of PW_OK tested at 60% of maximum load.	16		ms
Tpson_on_delay	Delay from PS_ON active to output voltage within regulation limits.	5	400	ms
Tpson_pwok	Delay from PS_ON de-active to PW_OK being de-asserted.		50	ms
Tpwok_on	Delay from output voltage within regulation limits to PW_OK asserted at turn on.	100	500	ms
Tpwok_off	Delay from PW_OK de-asserted to output voltage dropping out of regulation limits, tested at 60% of maximum load.	1		ms
Tpwok_low	Duration of PW_OK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
Tsb_vout	Delay from 5 V_{SB} being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms

Table 1. Output Voltage & Turn On/Off Timing

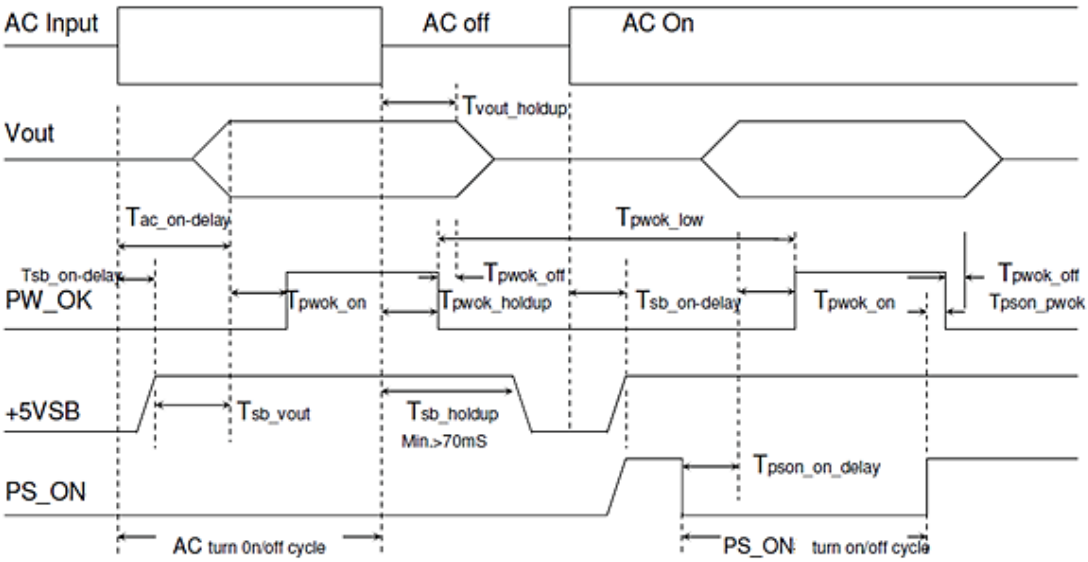

Figure 6. Turn On/Off Timing

7. MONITORING FOR Power MANAGEMENT BUS ACCURACY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input RMS Voltage	$V_{i\ min} \le V_i \le V_{i\ max}$	-3		+3	%
$I_{i\ mon}$	Input RMS Current	$I_i > 4\ A_{rms}$	-10		+10	%
		$I_i \le 4\ A_{rms}$	-0.4		+0.4	A_{rms}
$P_{i\ mon}$	True Input Power	$P_i > 200$ W	-10		+10	%
		$P_i \le 200$ W	-20		+20	W
$V_{1\ mon}$	V_1 Voltage		-2		+2	%
$I_{1\ mon}$	V_1 Current	I1 > 10 A	-3		+3	%
		I1 ≤ 10 A	-0.3		+0.3	A
$P_{o\ nom}$	Total Output Power	Po > 200 W	-5		+5	%
		Po ≤ 200 W	-10		+10	W
$V_{SB\ mon}$	Standby Voltage		-2		+2	%
$I_{SB\ mon}$	Standby Current	$I_{SB} \le I_{SB\ nom}$	-0.2		+0.2	A

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8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER		DESCRIPTION/CONDITION	MIN	NOM	MAX	UNIT
INPUT SIGNALS						
PSKILL, PSON, PDB_ALERT, PDB_FAULT						
V_{IL}	Input Low Level Voltage		0		1.0	V
V_{IH}	Input High Level Voltage		2.0		3.5	V
$I_{IL, H}$	Maximum Input Source Current				4	mA
OUTPUT SIGNALS						
PW_OK						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 0.2 mA	2.4		3.5	V
R_{puPW_OK}	Internal Pull Up Resistor on PW_OK			1.6		kΩ
AC_OK						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{leak}< 50 µA	2.4		3.5	V
R_{puAC_OK}	Internal Pull Up Resistor on AC_OK			1.6		kΩ
SMB_ALERT						
V_{OL}	Output Low Level Voltage		0		0.4	V
V_{OH}	Output High Level Voltage	I_{leak} < 4 mA			3.5	V
R_{puSMB_ALERT}	Internal Pull Up Resistor on SMB_ALERT	I_{leak}< 100 µA		4.7		kΩ

8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5 V. Therefore, all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.

If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in Figure 7 (except for SMB_ALERT, PW_OK pins). This will ensure the pin voltage is not affected by an unpowered power supply.

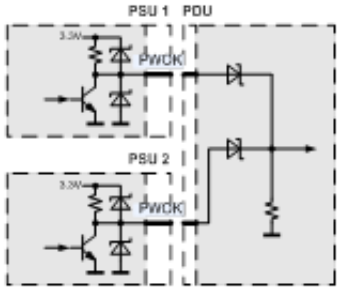

Figure 7. Interconnection of Signal Pins

8.3 FRONT LEDS

Status information is indicated by front-panel LED, LED is bi-colored: green and yellow. See Table 2 for the different LED status.

POWER SUPPLY CONDITION	LED
No AC power to all PSU	OFF
AC present/only standby output ON	1 Hz Flashing Green
Power supply DC output ON and OK	Green
Power supply failure	Yellow
Power supply warning	0.5 Hz Flashing Yellow*/Green*

* Flashing frequency: 1 Hz (0.5 sec Yellow/ 0.5sec Green)

Table 2. LED Status

8.4 PS_KILL

The PS_KILL input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PS_KILL input state.

8.5 AC_OK

The power supply will automatically turn-on when connected to the AC line under the condition that the PS_ON signal is pulled low and the AC line is within range. The AC_OK signal is active-high.

8.6 PS_ON

The PS_ON is an internally pulled-up (3.3 V) input signal to enable/disable the main output V_1 of the front-end. This active-low pin is also used to clear any latched fault condition.

8.7 PDB_ALERT

The PDB_ALERT is received signal from system, if signal is pulled low, the unit internal fan will be forced to run at maximum speed, this signal is inactive at standby mode.

8.8 SMB_ALERT

The SMB_ALERT is an output signal and it is pulled to 3.3V by a 4.7K resistor in power supply. The signal is low that indicates the power supply is experiencing a problem and the user should investigate.

8.9 PW_OK

The PW_OK is an open drain output with an internal pull-up to 3.3 V indicating whether both VSB and V1 outputs are within regulation.

8.10 PDB_FAULT

The PDB_FAULT receive a signal from system, Power will be shut down if this signal is high.

8.11 CURRENT SHARE

The PET front-ends have an active current share scheme implemented for V1. Eight of supplies in parallel are allowed. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.
For V1 output the Ishare (load sharing) voltage shall be a linear function Ishare [V] = 8 x Iout/62 (with 8 V at 62 A) for a single power supply (~129 mV/A).

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At light load, the load share becomes difficult because of low feedback signal. Refer to output parameters table for current sharing accuracy.
The current balance accuracy is calculated as: 2*|I1-I2|/ (I1+I2), where the I1 is the PSU1 load current and I2 is the PSU2 load current. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.
The standby output uses a passive current share method (droop output voltage characteristic).

8.12 REMOTE SENSE

Main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 200 mV on the output return rail.

8.13 I2C / POWER MANAGEMENT BUS COMMUNICATION

The interface driver in the PET supply is referenced to the V1 Return. The PET supply is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and further characterized referenced in Figure 8:

- There are 10K internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms

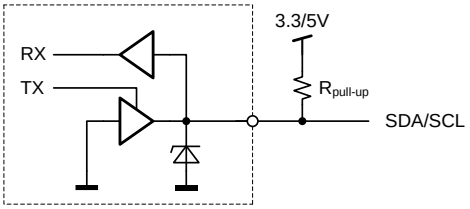

Figure 8. Physical layer of communication interface

The SMB_ALERT signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events.
Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life VSB output (provided e.g. by the redundant unit).

PARAMETER		DESCRIPTION /CONDITION	MIN	MAX	UNIT
t_r	Rise time for SDA and SCL			1000	Ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF		300	Ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
R_{pu}	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 3. I2C / SMBus Specification

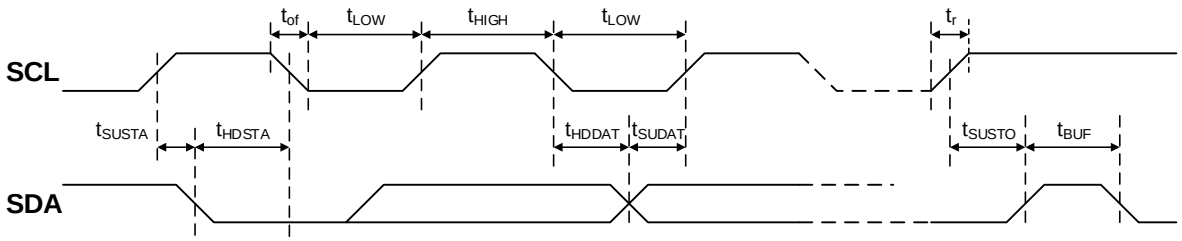

Figure 9. I2C / SMBus Timing

8.14 ADDRESS SELECTION

A2	A1	A0	EEPROM Address	Unit Address
0	0	0	0xA0	0xB0
0	0	1	0xA2	0xB2
0	1	0	0xA4	0xB4
0	1	1	0xA6	0xB6
1	0	0	0xA8	0xB8
1	0	1	0xAA	0xBA
1	1	0	0xAC	0xBC
1	1	1	0xAE	0xBE

8.15 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see figure 10). An I2C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.
The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default, the write protection is on.
The EEPROM provides 32K bytes of user memory. None of the bytes are used for the operation of the power supply.

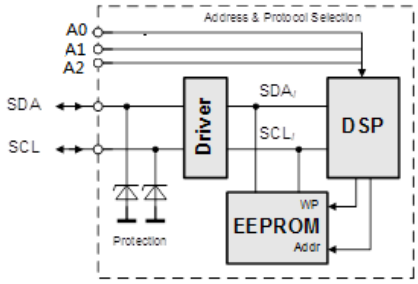

Figure 10. I2C Bus to DSP and EEPROM

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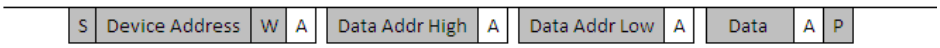
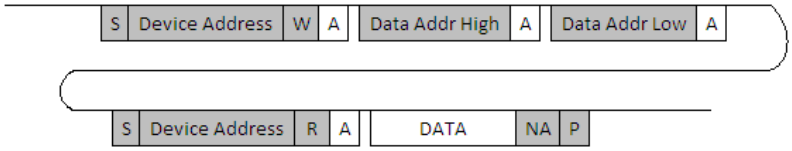
8.16 EEPROM PROTOCOL

The EEPROM behaviour the same as the 24C32 series 16 bit address protocol, High order address byte followed by low order address byte. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

Byte Write:

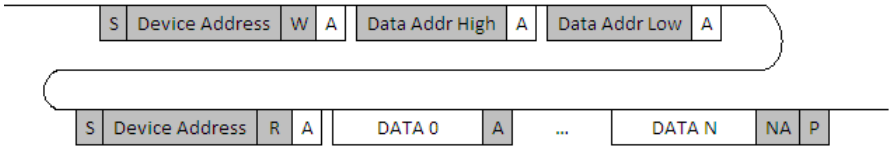


Byte Read:



Page Write:

Page Read:



The page size is 32 bytes.

8.17 POWER MANAGEMENT BUS PROTOCOL

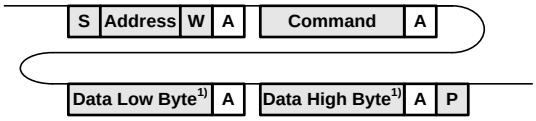
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PET750-12-050 supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

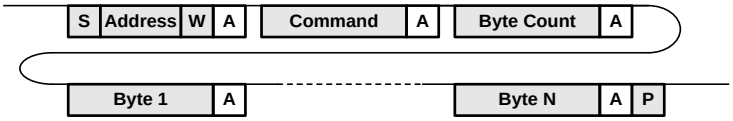
Write

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



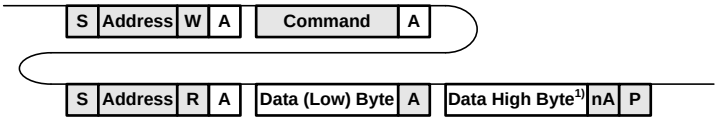
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PET750-12-050 Programming Manual for further information.



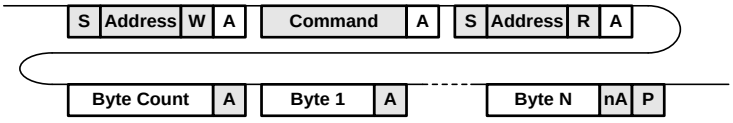
Read

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See PET750-12-050 Programming Manual for further information.



8.18 POWER MANAGEMENT BUS PROTOCOL

Bel Power Solutions provide with its “Bel power solutions I2C” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PET750-12-050 Front-End. The utility can be downloaded on: belfuse.com/power-solutions and supports both the PSMI and Power Management Bus protocols.
The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.
If the GUI is used in conjunction with the PET750-12-050 Evaluation Kit it is also possible to control the PS_ON pin(s) of the power supply.

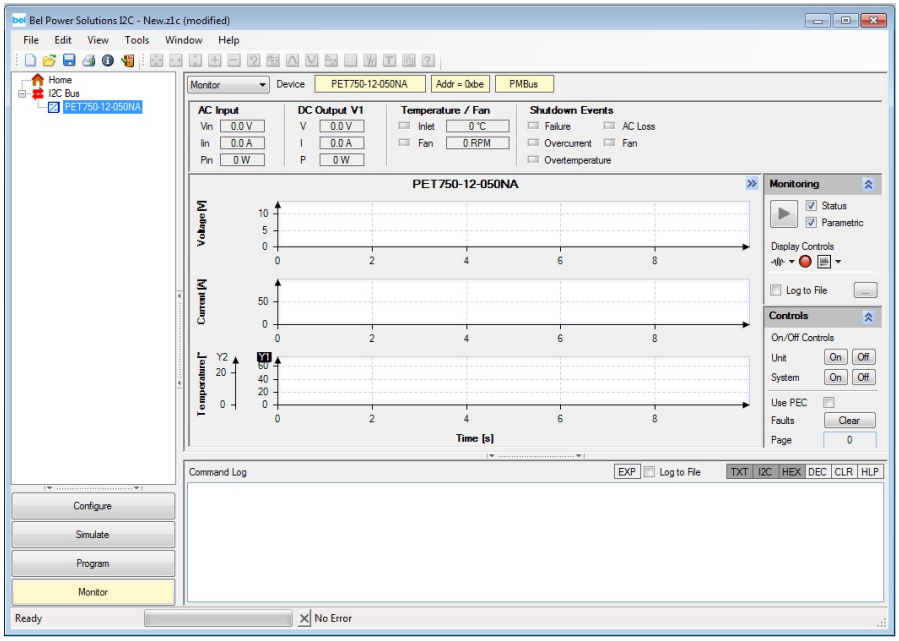


Figure 11. Monitoring dialog of the I²C Utility

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9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PET750-12-050 is provided with a normal airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the AC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the AC-inlet.

The IEC connector on the unit is rated 100°C. If 70°C mating connector is used then end user must derate the input power to meet a maximum 70°C temperature at the front for PET750-12-050NA. the rated output power should be 516W if input voltage less than 164VAC for PET750-12-050NA, don't need derate for PET750-12-050RA.

NOTE: It is the responsibility of the user to check the front temperature in such case. The unit will not limit its power automatically to meet such a temperature limitation.

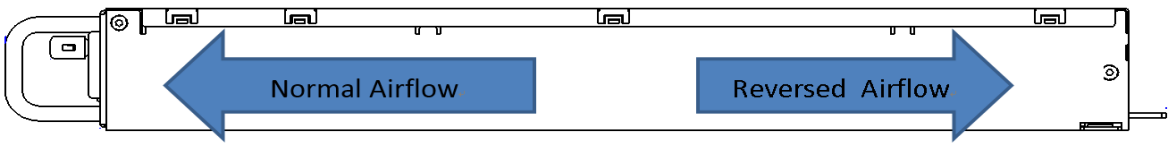

Figure 12. Airflow direction

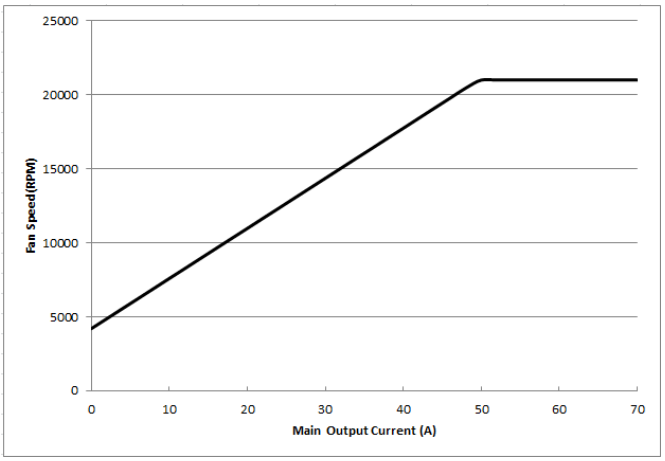

Figure 13. Fan speed vs. main output load

10. ELECTROMAGNETIC COMPATIBILITY

PARAMETER	DESCRIPTION / CONDITION		CRITERION
Electromagnetic Interference	FCC CFR Title 47 Part 15, Sub Part B, EN55022/EN55024		Class B
Harmonics	IEC61000-3-2		A
Flicker	IEC61000-3-3		
ESD Susceptibility	EN-61000-4-2, ±8 kV by Air, ±4 kV by Contact		A
Radiated Susceptibility	80MHz~1000MHz(3V/m(rms) Amplitude 80% AM 1KHz		A
EFT/Burst	EN61000-4-4, 5 kHz, AC: 1 kV,		A
Surge Voltage	EN61000-4-5, Line-to-Line: 1 kV, Line-to-Ground: 2 kV		A
Conducted Susceptibility	EN61000-4-6, 0.15MHz~80MHz 3Vrms amplitude 80% AM 1KHz		A
Power Frequency Magnetic Field Immunity	EN61000-4-8, 30 A/m		A
Voltage Dips and Interruptions	EN61000-4-11	30% (Voltage Dips), 10 ms	A
		60% (Voltage Dips), 100 ms	C
		>95% (Voltage Dips), 500 ms	C
Leakage Current	EN60950-1, 3.5 mA @ 264 VAC/60 Hz		

11. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 62368-1, and UL/CSA 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Agency Approvals	Approved to latest edition of the following standards: UL/CSA62368-1, IEC62368-1 and EN62368-1. GB4943.1, GB9254.1; GB17625.1 CNS15598-1, CNS15936		Approved		
	CMTBF	>300,000 hour @ Full rated load; 120V AC input; Ground Benign; 25°C(MIL-HDBK-217F-2)				
	Isolation	Input to case (PE)		Basic		
		Input (L/N) to output		Reinforced		
d_C	Creepage / Clearance	Primary to protective earth (PE)		3.0 minimum		mm
		Primary to secondary		6.0 minimum		
	Electrical Strength Test	Input to case	2500			VDC
		Input to output	4000			

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12. ENVIRONMENTAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Temperature	Operating ambient temperature, normal mode (inlet air): $T_{a\,min}$ to $T_{a\,max}$	0		+50	°C
	Non-operating Ambient	-40		70	°C
Humidity	Operating (Non-condensing)	20		90	%
	Non-operating (Non-condensing)	5		95	%
Altitude	Operating, above Sea Level			5000	m
	Non-operating, above Sea Level			40,000	Feet
Mechanical Shock	Non-Operating: 50 G Trapezoidal Wave, 11mS half sin wave. The shock is to be applied in each of the orthogonal axes.				
Vibration	Subjected to a vibration test consisting of a 10 to 300 Hz sweep at a constant acceleration of 2.0g for duration of one (1) hour for each of the perpendicular axes X, Y and Z (0.1 octave/minute). The output voltages shall remain within specification.				
Acoustic Noise	1 meter, 25°C, 50% load		46		dBA

13. MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		50.5		mm
		Heigth		40		mm
		Depth		300		mm
m	Weight			870		g

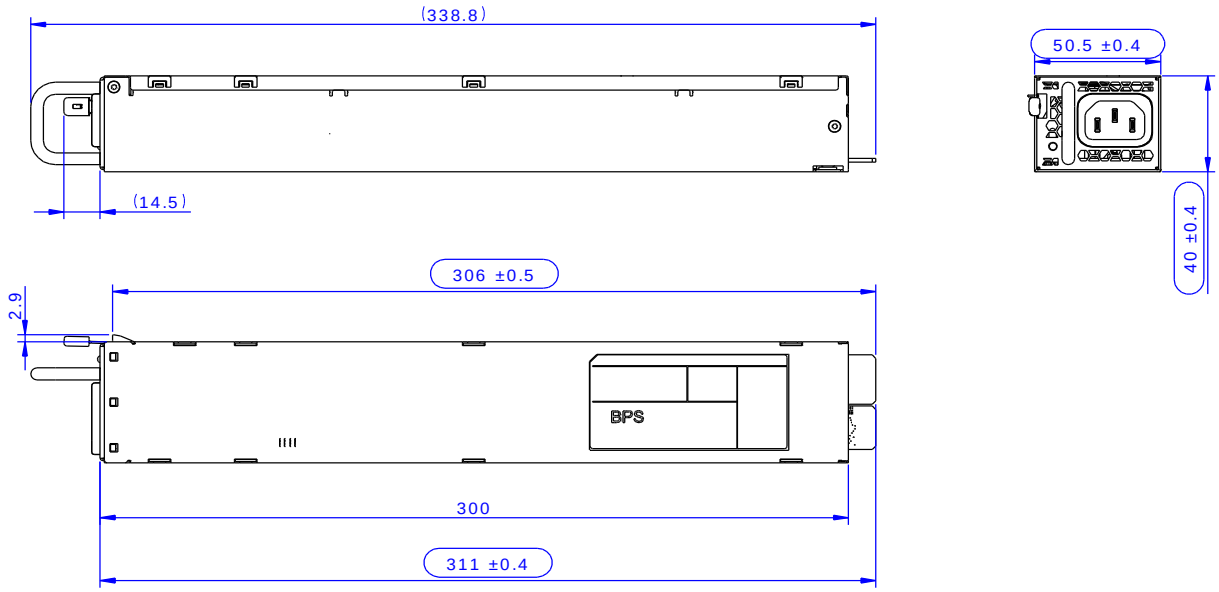

Figure 14. Mechanical Drawing-Side/Top View

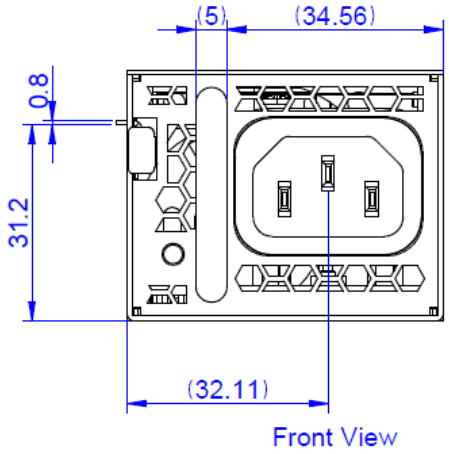

Figure 15. Front View

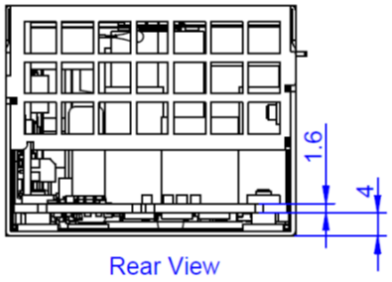

Figure 16. Rear View

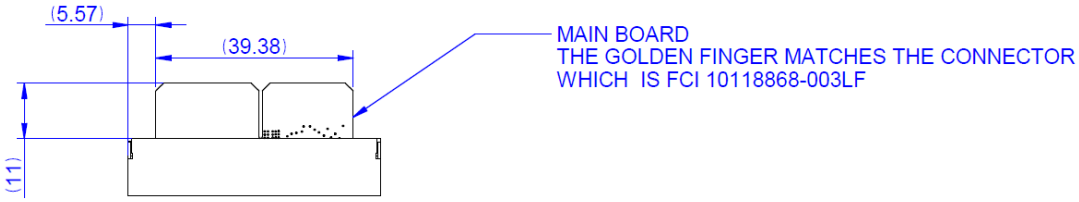

Figure 17. Mating Connector FCI 10118868-003LF

14. CONNECTIONS

The AC input receptacle is a 3 pins IEC320 C14 inlet.
For the pin assignment of DC connector, please refer to Figure 18 and Table 4.

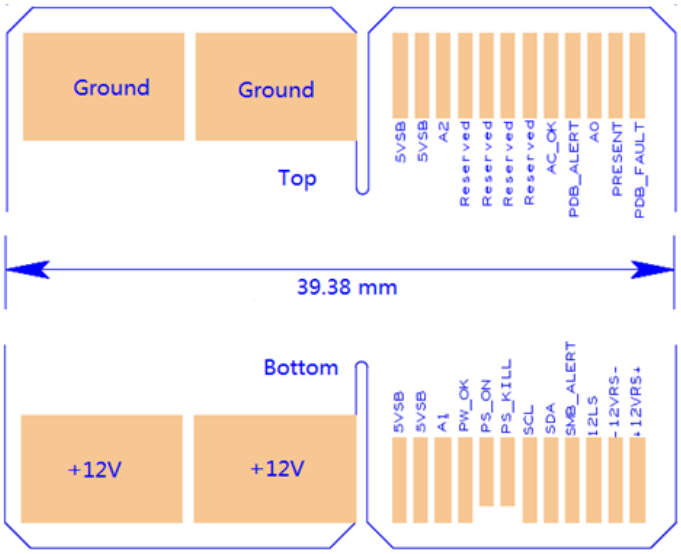

Figure 18. Pin Assignment of DC Connector

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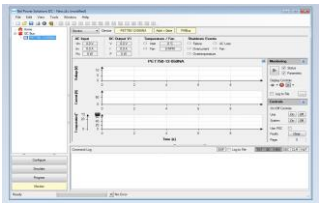
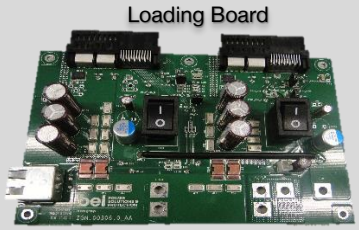
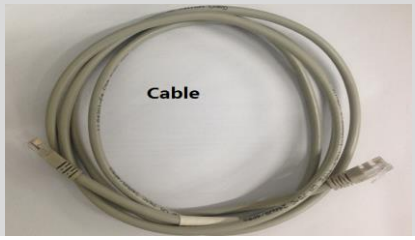
PIN	Description
+12V	12 V power output
GND	Grounding
5 V_{SB}	5 V standby power
A0	I^2C Address
A1	I^2C Address
A2	I^2C Address
PW_OK	Power Good Output. Signal is pulled HIGH to indicate all outputs ok.
PS_ON	Module PS_ON Remote control power On/Off (Pulled LOW = POWER ON)
PS_KILL	Activate PSU by hot-plug activity
SCL	I^2C CLOCK
SDA	I^2C DATA
PDB_ALERT	To receive ALERT signal from system, If signal is pulled LOW, the unit internal fan will be forced to run at maximum speed, This signal is inactive at standby mode.
SMB_ALERT	SMB Alert signal output: active-low
12LS	12 V Load Share
PRESENT	This pin is grounded with a 47R resistor, to indicate a power has been plugged in.
12VRS+	12 V Remote sense
12VRS-	12 V Remote sense return
PDB_FAULT	To receive a FAULT signal. Power shall be shut down if this pin is pulled HIGH.
AC_OK	AC input OK signal: active-high

Table 4. Output Pin Assignment

15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**BPS I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PET Front-Ends (and other I²C units)	Download	belfuse.com/power-solutions
   	**Dual Connector Board** Connector board to operate 2 PET units in parallel. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).	VRA.00335.0	Bel Power Solutions

For more information on these products consult: tech.support@psbel.com

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