

TEC3201-12-074xD Series

DC-DC Front-End Power Supply

The TEC3201-12-074xD series is a 3200 Watt DC to DC power supply that converts -40 to -72 VDC voltage into an isolated main output of 12.2 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The TEC3201-12-074xD series utilizes full digital control architecture for greater efficiency, control, and functionality.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



Key Features & Benefits

- High Efficiency, typ. 95% efficiency at half load
- Wide input voltage range: -40 to -72 VDC
- 3200 W continuous output power capability
- Always-on standby 12V / 3.5A output
- **CRPS Form Factor**
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- High power density design: 100 W/in³
- Small form factor (W x H x L): 73.5 x 40.0 x 185 mm (2.89 x 1.54 x 7.28 in)
- Power Management Bus communication interface for control, programming and monitoring
- Over temperature, output over voltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- Front LED with fault signaling
- Black Box Recorder, Bootloader

Applications

- Networking Switches
- Servers & Routers
- Telecommunications



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1. ORDERING INFORMATION

TEC	3200	-	12	-	074	x	D	x
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow	Input	Specific code ²
TEC Front-Ends	3200 W		12 V		74.0 mm	N: Normal ¹ R: Reverse ¹	DC	x = Blank x = S+3 digits

¹ "N" Normal Airflow from Output connector to Input DC connector, "R" Reverse Airflow from Input DC connector to Output connector.

² Contact factory for availability of Specific code.

2. OVERVIEW

The TEC3201-12-074xD DC/DC power supply is a DSP controlled, highly efficient front-end power supply. It incorporates state of the art technology and uses an interleaved forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency.

With a wide input DC voltage range the TEC3201-12-074xD maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

An active ORing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always on standby output provides power to external power distribution and management controllers. It is protected with an active ORing device for maximum reliability.

Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

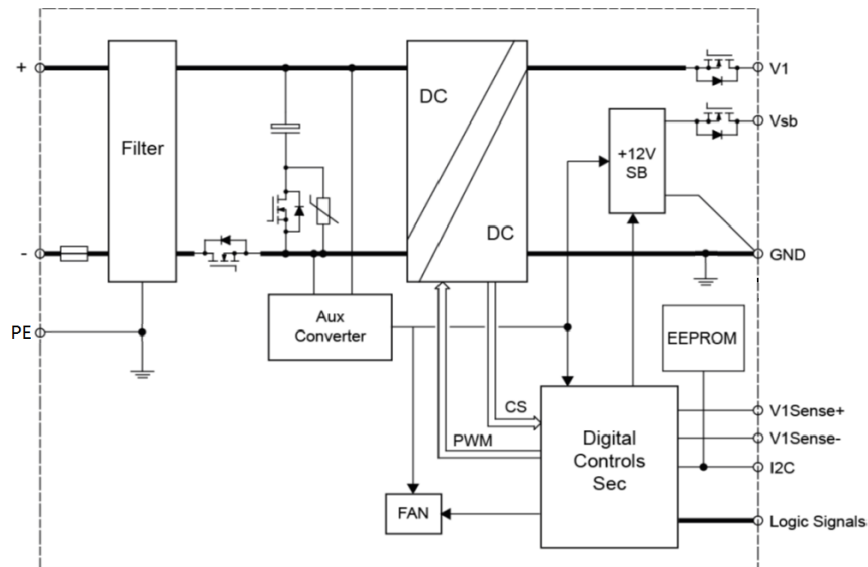


Figure 1. TEC3201-12-074xD Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
V_i maxc	Maximum Input	Continuous	-75	VDC



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4. INPUT

General Condition: $T_{amb} = -5...+50\text{ }^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_i\text{ nom}$	Nominal input voltage	-48		-60	VDC
V_i	Input voltage	Normal operation (from $V_i\text{ min}$ to $V_i\text{ max}$)		-72	VDC
I_i	Input current	$V_i > V_i\text{ min}$		92	A
$I_i\text{ pk}$	Inrush current limitation	From $V_i\text{ min}$ to $V_i\text{ max}$, $T_A = 25^{\circ}\text{C}$, cold start		120	A
$V_i\text{ VSB}_{on}$	Turn-on standby input voltage	Ramping up		-32	VDC
$V_i\text{ VSB}_{off}$	Turn-off standby input voltage	Ramping down		-30	VDC
$V_i\text{ V1}_{on}$	Turn-on V1 input voltage	Ramping up		-40	VDC
$V_i\text{ V1}_{off}$	Turn-off V1 input voltage	Ramping down		-39	VDC
η	Efficiency ¹	$V_i = -48\text{ VDC}$; -60 VDC; 20% load		94	%
		$V_i = -48\text{ VDC}$; -60 VDC; 50% load		95	%
		$V_i = -48\text{ VDC}$; -60 VDC; 100% load		92	%
T_{V1_holdup}	Hold-up Time V1	$V_1 > 10.8\text{ V}$, $V_i = -48\text{ VDC}$, $P_{0\text{ nom}}$ (from DC input lost to V1 lost to 10.8 V)		1.0	ms
T_{VSB_holdup}	Hold-up time Vsb	V , $V_i = -48\text{ VDC}$, $P_{0\text{ nom}}$		2.5	ms

4.1 INPUT FUSE

120 A (or equivalent) input fuse in the negative voltage path inside the power supply protects against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

4.3 INPUT UNDER-VOLTAGE

If the input voltage stays below the input under voltage lockout threshold $V_i\text{ on}$, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 EFFICIENCY

High efficiency (see [Figure 2](#)) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

¹ Efficiency measured without fan power per EPA server guidelines.



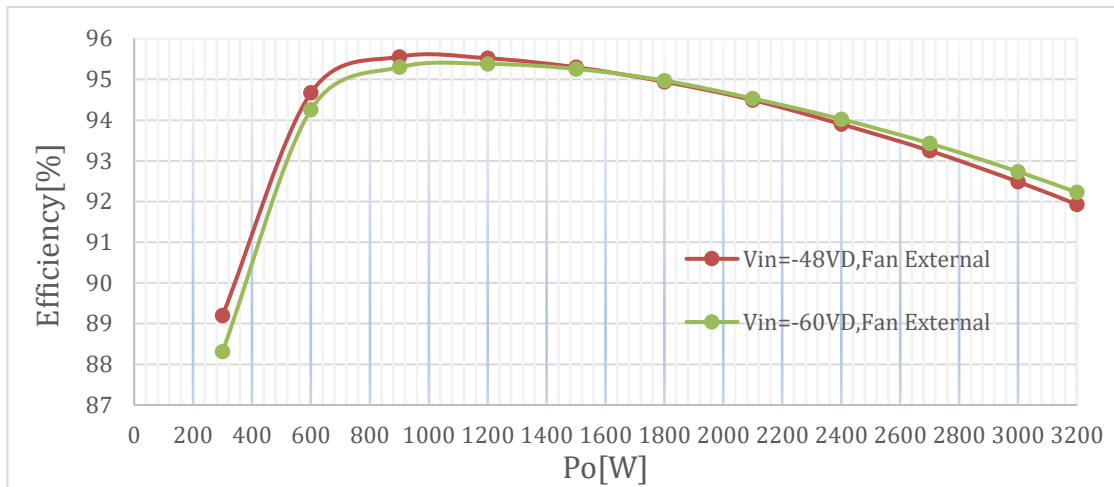


Figure 2. Efficiency vs. Output power

4.5 DC LINE TRANSIENT TEST

MINUS 72 VDC LINE TRANSIENT TEST

A standard line voltage momentary transient test is shown below. This test simulates a momentary voltage overshoot. This should not affect the operation of the PSU; the output voltage should remain in regulation. This test shall be conducted every 10 seconds for 30 min (180 times total).

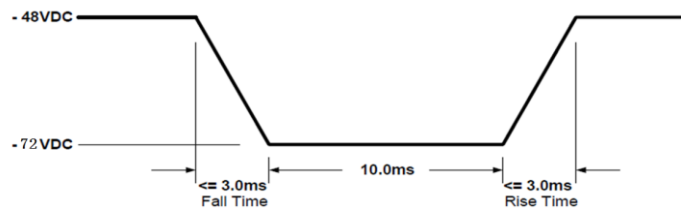


Figure 3. Minus 72 VDC Line Transient Test

0 V LINE TRANSIENT TEST

A standard line voltage momentary blackout test is shown below. This test simulates a momentary switch throw off-on, see graph below. The power supply should restart, not latch. This test shall be conducted 3 times in 10 min intervals.

Practically a blackout of any duration should not damage the power supply in any way and not cause a latch off condition.

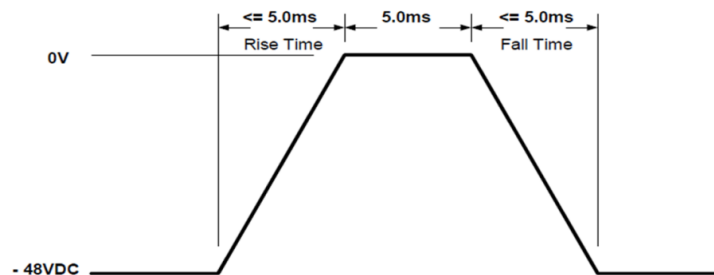


Figure 4. 0 V Line Transient Test



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5. OUTPUT

General condition: $T_{amb} = -5 \dots +50 \text{ }^{\circ}\text{C}$, $V_i = -48 \text{ VDC}$ unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1					
$V_{1\text{ nom}}$	Nominal Output Voltage		12.2		VDC
$V_{1\text{ set}}$	Output Set Point Accuracy	-0.5		+0.5	% $V_{1\text{ nom}}$
$dV_{1\text{ tot}}$	Total Regulation	-5		+5	% $V_{1\text{ nom}}$
$P_{1\text{ nom}}$	Nominal Output Power		3200		W
$I_{1\text{ nom}}$	Output Current		262.3		ADC
$V_{1\text{ pp}}$	Output Ripple Voltage ¹			120 ²	mVpp
$dV_{1\text{ load}}$	Load Regulation			480	mV
$dV_{1\text{ line}}$	Line Regulation			120	mV
$dI_{1\text{ share}}$	Current Sharing	-5		+5	A
$V_{1\text{ SHARE}}$	Current Share Bus Voltage		8		VDC
$dV_{1\text{ dyn}}$	Dynamic Load Regulation ³	-5		+5	% $V_{1\text{ nom}}$
t_{rec}	Recovery Time			2	ms
$t_{\text{VIN } V_1}$	Start-up Time from DC			3	sec
$t_{V_1\text{ rise}}$	Output Voltage Rise Time			30	ms
$t_{V_1\text{ ovr sh}}$	Output Turn-on Overshoot			0.6	V
$C_{V_1\text{ load}}$	Capacitive Loading			30	mF
V_{SB} Standby Output					
$V_{SB\text{ nom}}$	Nominal Output Voltage		12.0 12.2		VDC
$V_{SB\text{ set}}$	Output Set point Accuracy	-1		+1	% $V_{SB\text{ nom}}$
$dV_{SB\text{ tot}}$	Total Regulation	-5		+5	% $V_{SB\text{ nom}}$
$P_{SB\text{ nom}}$	Nominal Output Power		42		W
$I_{SB\text{ nom}}$	Output Current		3.5		ADC
$V_{SB\text{ pp}}$	Output Ripple Voltage ¹			120	mVpp
$dV_{SB\text{ load}}$	Load Regulation		250		mV
$dV_{SB\text{ line}}$	Line Regulation		20		mV
$dV_{SB\text{ dyn}}$	Dynamic Load Regulation	-0.6		0.6	V
t_{rec}	Recovery Time			2	ms
$t_{V_{SB}\text{ rise}}$	Output Voltage Rise Time			30	ms
$t_{\text{VIN } V_{SB}}$	Start-up Time from DC			2.7	sec
$t_{V_{SB}\text{ ovr sh}}$	Output Turn-on Overshoot			0.6	V
$C_{V_{SB}\text{ load}}$	Capacitive Loading			3.1	mF

¹ Ripple noise & dynamic load measured with a 10 μ F low ESR capacitor in parallel with a 0.1 μ F ceramic capacitor at the point of measurement.

² Ripple noise is 150mV when $V_{in} = -72\text{Vdc}$ with 262.3A full load.

³ Dynamic load testing the input voltage needs to be above 40.5V.



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5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referred to in these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 5*. Alternatively, separated ground signals can be used as shown in *Figure 6*. In this case the two ground planes should be connected at the power supplies ground pins.

NOTE: Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal. Therefore, it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

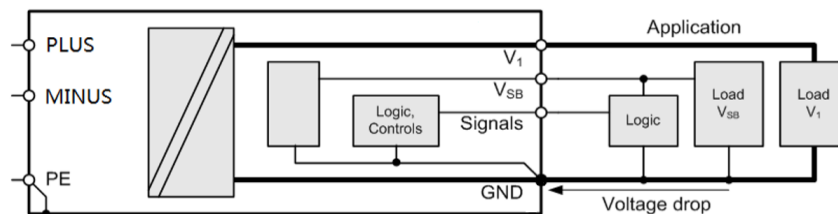


Figure 5. Common Low Impedance Ground Plane

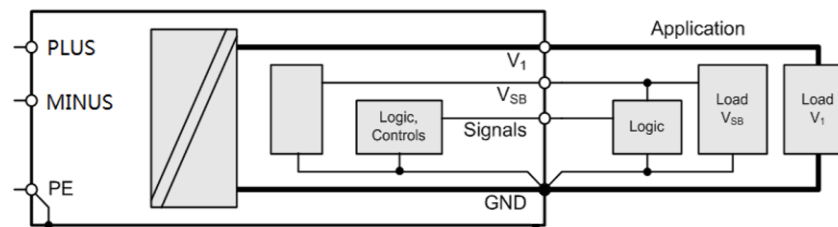


Figure 6. Separated Power and Signal Ground

5.2 RIPPLE / NOISE

Internal capacitance at the 12V output (behind the ORing circuitry) is minimized to prevent disturbances during hot plug. To provide low output ripple voltage in the application, external capacitors (a parallel combination of a low ESR capacitor in parallel with a 0.1μF and 10μF ceramic capacitor) should be added close to the power supply output. The ripple voltage is measured with 20 MHz BWL, close to the external capacitors. The test setup shall follow *Figure 7*.

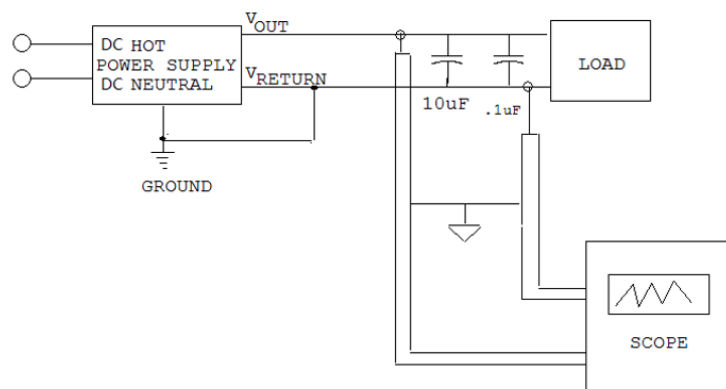


Figure 7. Output ripple Test Setup

NOTES: When performing this test, the probe clips should be close to capacitors.

6. PROTECTION SPECIFICATIONS

General Condition: $T_{amb} = -5... +50\text{ }^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)	Not user accessible, fast acting			A
$V_{1\text{ OV}}$	OV Threshold V_I	13.3		14.5	VDC
$t_{\text{OV } V1}$	OV Latch Off Time V_I			1	ms
$V_{\text{VSB OV}}$	OV Threshold V_{SB}			14.5	VDC
$t_{\text{OV VSB}}$	OV Latch Off Time V_{SB}			1	ms
$I_{V1\text{ OC}}$	OC Limit V_I	Refer to section 6.3.1			A
$I_{\text{VSB OC}}$	OC Limit V_{SB}				A
T_{SD}	Over Temperature on Critical Points	Automatic shut-down			$^{\circ}\text{C}$
		Refer to table 7			

6.1 OVER VOLTAGE PROTECTION

The TEC3201-12-074xD front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input.

6.2 UNDER VOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_H pin signal if the output voltage exceeds the regulation limit. Output under voltage protection is provided on both outputs. When either V_I or V_{SB} fall below 11V, the output is inhibited.

6.3 CURRENT LIMITATION

6.3.1 MAIN OUTPUT

The power supply shall have current limit to prevent the outputs from exceeding the values shown in Table 1. If the current limits are exceeded the power supply shall shut down and latch off. The latch will be cleared only by a DC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto recovered after removing OCP limit.

NORM	DESCRIPTION	CURRENT THRESHOLD (A)		TRIP TIMING		COMMENTS
		MIN	MAX	MIN	MAX	
OCP1	Fast over current protection (shutdown, latch)	344.3A	354.3A	100μs		
OCP2	Slow over current protection (shutdown, latch)	282.3A	292.3A	20ms	100ms	
OCW1	Fast over current warning (SMB_ALERT_L)	324.3A	344.3A	100μs	600μs	SMB_ALERT_L Latch and hold for 50-150ms
OCW2	Slow over current warning	272.3A	282.3A	10ms	15ms	
OCPstby	Standby over current protection (shutdown, hiccup mode)	3.6	5			

Table 1. Current Limitation on V_I and standby



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6.3.1 STANDBY OUTPUT

A hiccup-mode overcurrent protection is implemented on the standby output. This protection will shut down the standby output immediately when standby current reaches or exceeds $I_{VSB\ OC\ lim}$. After an off time of 1 s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly try to restart with 1s intervals. A failure on the Standby output will shut down both Main and Standby outputs.

6.4 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature.

In an OTP condition the PSU main output will shut down, when the power supply temperature drops to within specified limits, the power supply shall restore power automatically, the OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition, the OTP trip temperature level shall be at least 5°C higher than over temperature warning threshold level.

7. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to TEC3201-12-074xD Power Management Bus Communication Manual.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input Voltage	$V_{i\ min} \leq V_i \leq V_{i\ max}$	-1		+1	VDC
$I_{i\ mon}$	Input Current	$I_i \leq 20A$	-1		+1	ADC
		$I_i > 20A$	-3		+3	%
$P_{i\ mon}$	Input Power	$P_i \leq 1000\ W$	-35		+35	W
		$P_i > 1000\ W$	-5		+5	%
$V_1\ mon$	V_1 Voltage		-1		+1	%
$I_1\ mon$	V_1 Current	$I_1 \leq 50A$	-2		+2	A
		$I_1 > 50A$	-2		+2	%
P_{nom}	V_1 Output Power	$120\ W \leq P_o \leq 700\ W$	-20		+20	W
		$P_o > 700\ W$	-2		+2	%
$V_{SB\ mon}$	Standby Voltage		-2		+2	%
$I_{SB\ mon}$	Standby Current	$I_{SB} \leq I_{SB\ nom}$	-0.2		+0.2	A
T_{ambmon}	Ambient Temperature		-3		+3	°C
$Fan\ Speed$	Fan speed		-500		+500	RPM

Table 2 PMBus Sensors Accuracy



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8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
PSON_L / HOTSTANDBYEN_H Inputs						
V _{IL}	Input Low Level Voltage		-0.2		0.8	V
V _{IH}	Input High Level Voltage		2.4		3.5	V
I _{IL, H}	Maximum Input Sink or Source Current		0		1	mA
R _{pu_intPSON_L}	Internal Pull Up Resistor on PSON_L			100		kΩ
R _{pu_intAx}	Internal Pull Up Resistor on A0, A1			10		kΩ
R _{pu_intHOTSTANDBYEN_H}	Internal Pull Up Resistor on HOTSTANDBYEN_H			2		kΩ
PWOK_H Output						
V _{OL}	Output Low Level Voltage	V _i < V _{i min LL} , I _{sink} =400μA	0		0.4	V
V _{OH}	Output High Level Voltage	V _i > V _{i min LL} , I _{source} =200μA	2.4		3.46	V
I _S	Maximum Sink Current	PWOK_H = low			400	μA
	Maximum Source Current	PWOK_H = high			2	mA
INPUT_OK_H Output						
V _{ext}	Maximum External Pull up Voltage				3.46	V
V _{OL}	Output Low Level Voltage	Failure or Warning condition, I _{sink} < 4mA	0		0.4	V
R _{pull up}	Pull-up to 3.3V Located in Power Supply			1		kΩ
I _S	Sink Current	VIN_OK_H = low			4	mA
SMB_ALERT_L Output						
V _{ext}	Maximum External Pull up Voltage				3.46	V
V _{OL}	Output Low Level Voltage	Failure or Warning condition, I _{sink} < 4mA	0		0.4	V
R _{pull up}	Pull-up to 3.3V Located in Power Supply			1		kΩ
I _S	Sink Current	SMB_ALERT_L = low			4	mA
		SMB_ALERT_L = high			50	μA

8.2 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative paths. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.3 CURRENT SHARE

The TEC3201-12-074xD front ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The bus voltage changes linearly with the current delivered by the PSU (0V corresponds to 0 A and 8V corresponds to 262.3A). The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The 12 VSB output is not required to actively share current between power supplies (passive sharing).



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8.4 PRESENT_L OUTPUT

This signaling pin PRESENT_L is wired through a 100 Ohms resistor to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor must be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low-level voltage if power supply is seated.

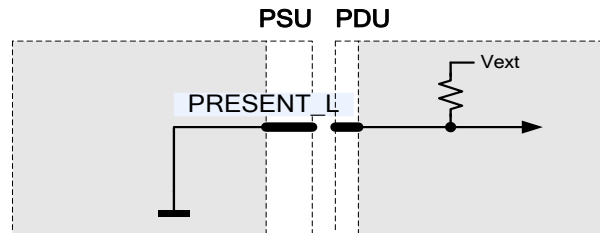


Figure 8. PRESENT_L Connection

8.5 PSON_L INPUT

The PSON_L is an internally pulled up (3.3V) signal to enable/disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. Figure 9 shows PSON_L circuit used in PSU and proposed connections.

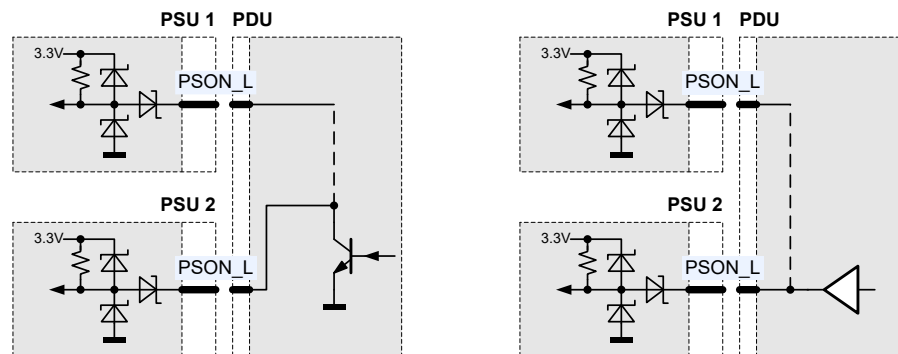


Figure 9. PSON_L connection

8.6 PWOK_H OUTPUT

The PWOK_H is an open drain output (without an internal pullup) indicating whether both VSB and V1 outputs are within regulation. This pin is active-high. When any output voltage falls below regulation limits or when DC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK_H will be de-asserted to a LOW state.

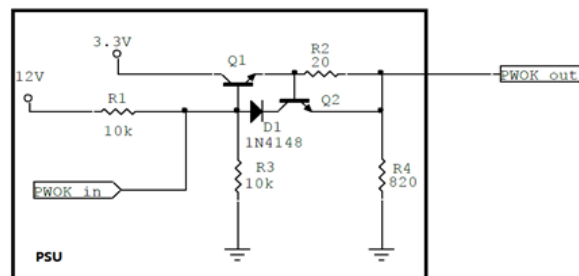


Figure 10. PWOK_H connection

8.7 SMB_ALERT_L OUTPUT



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The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, over-current, under voltage. This signal may also indicate the power supply is operating in an environment exceeding the specified limits.

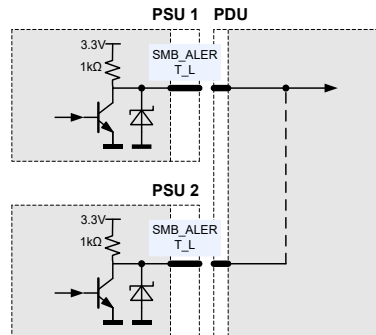


Figure 11. SMB_ALERT_L connection

8.8 INPUT_OK_H OUTPUT

This signal will be asserted, driven high, by the power supply to indicate that the input voltage meets the minimum requirements of the parametric PSU specification.

The PSU shall de-assert (drive low) under input over-voltage condition or input under-voltage condition.

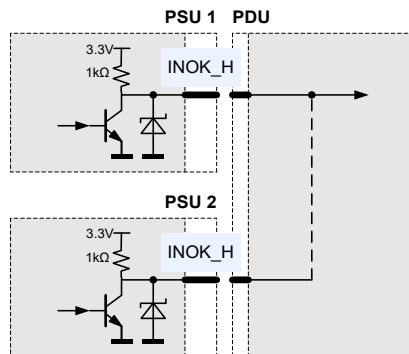


Figure 12. INPUT_OK_H connection

8.9 TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. All outputs must rise monotonically.



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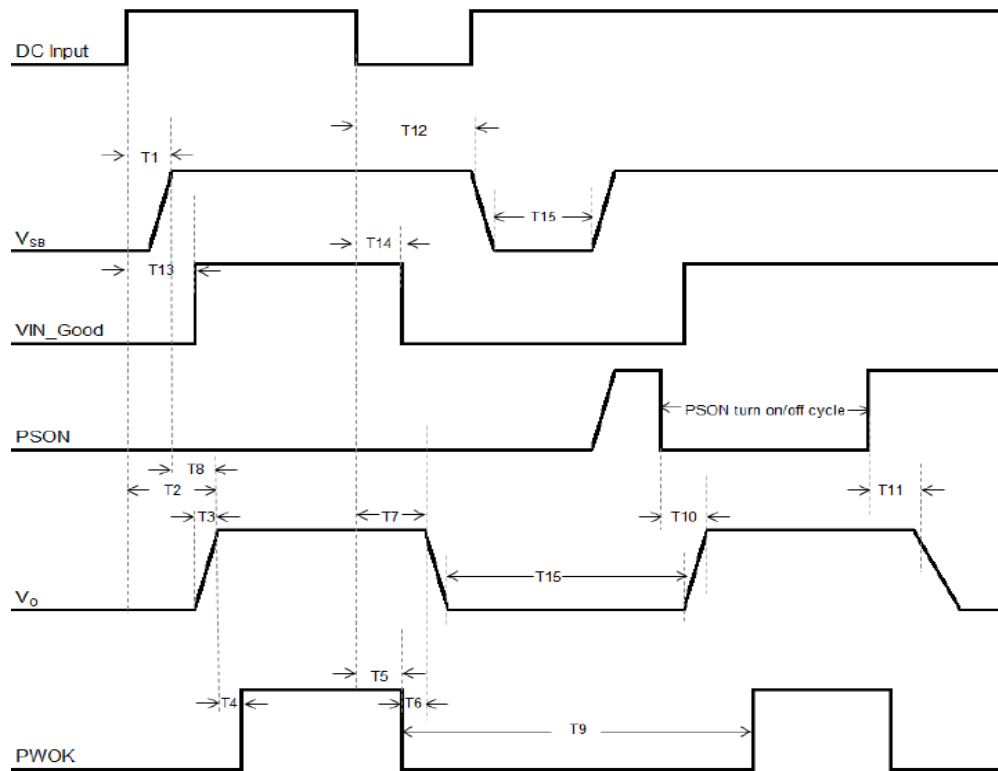


Figure 13. Timing Diagram

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vsb Power-on-delay(T1)	From application of Vin nom. to Vsb reaching 90% Vsb, nom.			2700	ms
V1 Power-on-delay(T2)	From application of Vin to V1 reaching 90% of Vout nom.			3000	ms
V1 Rise time(T3)	V1 rising from 10% to 90% V1 nom.			30	ms
V1 PW_OK delay(T4)	Delay from output voltages within regulation limits to PWOK asserted high at turn on	100		500	ms
PW_OK Hold Up(T5)	Delay from loss of DC to de-assertion of PW_OK	0.0			ms
PW_OK Warning(T6)	Delay from PWOK de-asserted to 90% Vout nom (due to loss of input power)	0.8			ms
V1 holdup(T7)	From loss of Vin to V1 falling to 90% Vout nom.	1.0			ms
Vsb to V1 delay(T8)	Delay from standby voltage in regulation to output voltage in regulation at DC turn on.	50		1000	ms
PW_OK Hold low(T9)	Duration of PWOK being in the de-asserted state during an off/on cycle using DC or the PSON signal.	100			ms
V1 PS_ON delay(T10)	Delay from PSON active to output voltages within regulation limits	5		400	ms
V1 PS_OFF delay(T11)	Delay from PSON deasserted to power supply turning off.			5	ms
Vsb holdup(T12)	From loss of Vin to Vsb falling to 90% Vsb nom	2.5			ms
Input_OK delay(T13)	From application of Vin to assertion of Input_OK Signal edge.			1800	ms
Input fail detect(T14)	From loss of Vin to falling edge of Input_OK signal.			2	ms

Table 3. Timing Requirements



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8.10 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable Oring gate, to make sure into hot standby mode. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having better efficiency.

8.11 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored green and yellow and indicates DC and DC power presence and warning or fault conditions. *Table 4* lists the different LED status.

POWER SUPPLY CONDITION	LED STATUS
Output ON and OK	Solid GREEN
No DC power to all power supplies	OFF
DC present / Only 12VSB on (PS off) or PS in Hot standby state	1Hz Blink GREEN
DC cord unplugged; with a second power supply in parallel still with DC input power.	Solid YELLOW
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink YELLOW
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	Solid YELLOW
Power supply in FW upload mode	2Hz Blink GREEN

Table 4. LED Characteristics

8.12 I2C BUS

The interface driver in the TEC3201-12-074xD supply is referenced to the SGND. The TEC3201-12-074xD supply is a communication Slave device only, it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing are defined in *Table 4* further characterized through:

- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

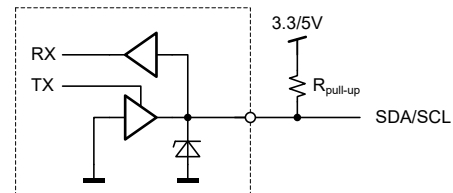


Figure 14. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible if the input DC voltage is provided. If no DC is present, communication to the unit is possible if it is connected to a live V_{SB} output or V_I output (provided by the redundant unit).

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
V_{IL}	Input low voltage	-0.5		1.0	V
V_{IH}	Input high voltage	2.3		5.5	V
V_{hys}	Input hysteresis	0.15			V
V_{OL}	Output low voltage	0		0.4	V
t_r	Rise time for SDA and SCL	20+0.1Cb ¹		300	Ns
t_{of}	Output fall time $V_{IHmin} \rightarrow V_{ILmax}$	10 pF < Cb ³ < 400 pF	20+0.1Cb ²	250	Ns
I_i	Input current SCL/SDA	0.1 VDD < V_i < 0.9 VDD	-10	10	μA
C_i	Internal Capacitance for each SCL/SDA			0	pF

¹ Cb = Capacitance of bus line in pF, typically in the range of 10...400 pF



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f_{SCL}	SCL clock frequency	0	100	kHz
R_{pu}	External pull-up resistor	$f_{SCL} \leq 100$ kHz	1000 ns / Cb	Ω
R_{pu_int}	Internal pull-up resistor	None		Ω
t_{HDSTA}	Hold time (repeated) START	$f_{SCL} \leq 100$ kHz	4.0	μ s
t_{LOW}	Low period of the SCL clock	$f_{SCL} \leq 100$ kHz	4.7	μ s
t_{HIGH}	High period of the SCL clock	$f_{SCL} \leq 100$ kHz	4.0	μ s
t_{SUSTA}	Setup time for a repeated START	$f_{SCL} \leq 100$ kHz	4.7	μ s
t_{HDDAT}	Data hold time	$f_{SCL} \leq 100$ kHz	0	3.45 μ s
t_{SUDAT}	Data setup time	$f_{SCL} \leq 100$ kHz	250	ns
t_{SUSTO}	Setup time for STOP condition	$f_{SCL} \leq 100$ kHz	4.0	μ s
t_{BUF}	Bus free time between STOP and START	$f_{SCL} \leq 100$ kHz	5	ms

Table 5. I²C / SMBus Specification

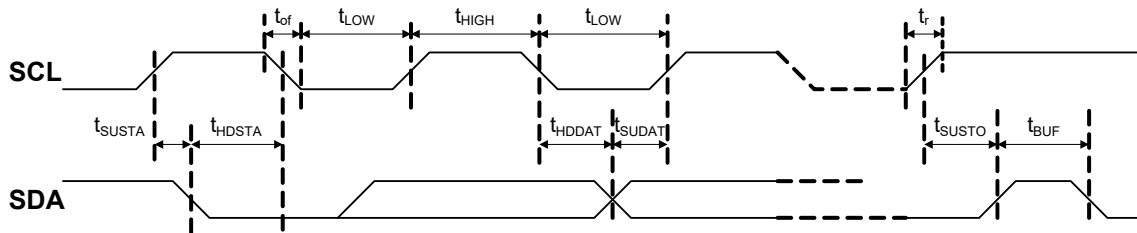


Figure 15. I²C / SMBus Timing

8.13 ADDRESS SELECTION (A0, A1)

The address for I2C communication can be configured by pulling address input pins A0 and A1 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A0 and A1 pin to be at a High Level if left open.

A fixed addressing offset exists between the Controller and the EEPROM.

NOTE: The address pins are only read at start-up of the power supply. Therefore, it is not possible to change address dynamically.

A1	A0	I2C Address ¹	
		Controller	EEPROM
0	0	0xB0	0xA0
0	1	0xB2	0xA2
1	0	0xB4	0xA4
1	1	0xB6	0xA6

Table 6. I2C Address combination

¹ The LSB of the address byte is the R/W bit

8.14 DSP CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 16).

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set.

To write to the EEPROM, firstly the write protection needs to be disabled by sending the appropriate command to the DSP. By default, the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

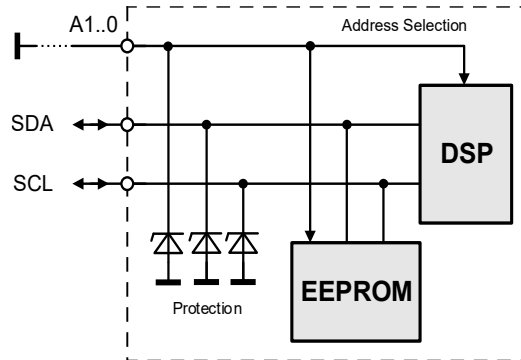


Figure 16. I2C Bus to DSP and EEPROM

8.15 EEPROM PROTOCOL

The EEPROM device used is the AT24C02C or compatible alternative.

8.16 DSP CONTROLLER PROTOCOL

Monitoring data is reported by the DSP Controller.

Refer to URP.00744 for the supported commands.



9. TEMPERATURE AND FAN CONTROL

FAN CONTROL

To achieve the best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. TEC3201-12-074ND is provided with normal airflow, which means the air enters through the DC output connector of the supply and leaves at the DC input connector. The TEC3201-12-074xD supply has been designed for horizontal operation. In a normal airflow unit, the hot air is exiting the power supply unit at the DC input connector.

The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

The TEC3201-12-074xD provides access via I2C to the measured temperatures of in total 4 sensors within the power supply, see Table 7. The microprocessor monitors these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V1 (or VSB if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signaled accordingly through LED, PWOK_H and SMB_ALERT_L.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	PMBUS® REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet air temperature	Sensor located on control board close to DC end of power supply	8Dh	78	83
Syn rectifier Mosfet1	Sensor located close to Syn rectifier Mosfet1	8Eh	125	130
Syn rectifier Mosfet2	Sensor located close to Syn rectifier Mosfet2	EAh	125	130
Outlet air temperature	Sensor located on main board close to DC input front of power supply	8Fh	ND:100 RD:95	ND:105 RD:100

Table 7. Temperature Sensor Location and Thresholds

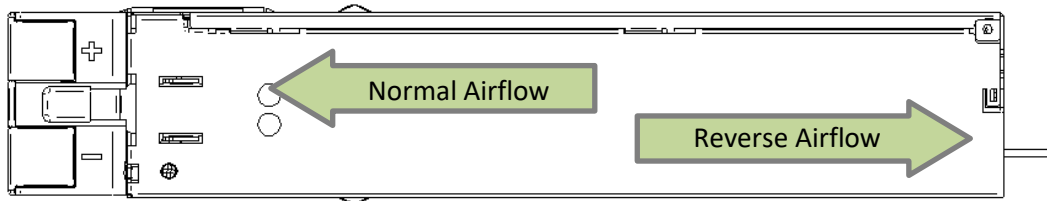


Figure 17. Airflow Direction

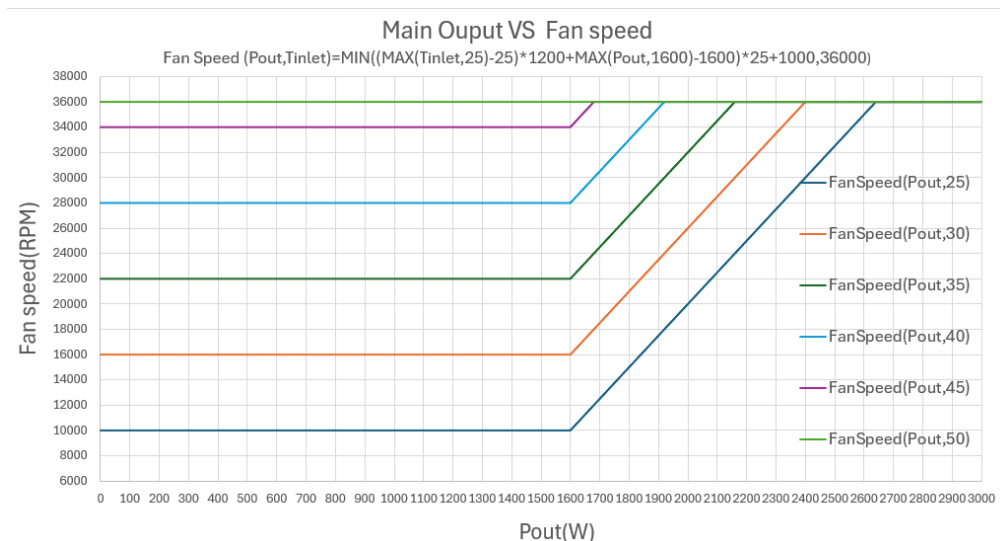


Figure 18. Fan Speed vs. Main Output Load



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10. ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ± 8 kV, 25+25 discharges per test point (metallic case, LED, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ± 15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetics Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 μ s Pulse Modulation	A
Burst	IEC / EN 61000-4-4, ± 2 kV, 1 minute	A
Surge	IEC / EN 61000-4-5, Line to earth: ± 1.5 kV Line to line: ± 1.5 kV	A
RF Conducted Immunity	IEC / EN 61000-4-6, Level 2, 10 Vrms	A

10.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55032:2015 / CISPR 32:2015: 0.15 ... 30 MHz, QP and AVG	Class A
Radiated Emission	EN 55032:2015 / CISPR 32:2015: 30 MHz ... 1 GHz, QP	Class A

11. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to UL/CSA 62368-1, IEC/EN 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to the latest edition of the following standards: UL/CSA 62368-1, IEC 62368-1	Approved
Isolation Strength	Input (L/N) to chassis (PE)	Basic
	Input (L/N) to output	Basic
	Output to chassis (PE)	Functional
Electrical Strength Test	Input to output	1500 VDC
	Input to chassis	1500 VDC
	Output and Signals to case	NA



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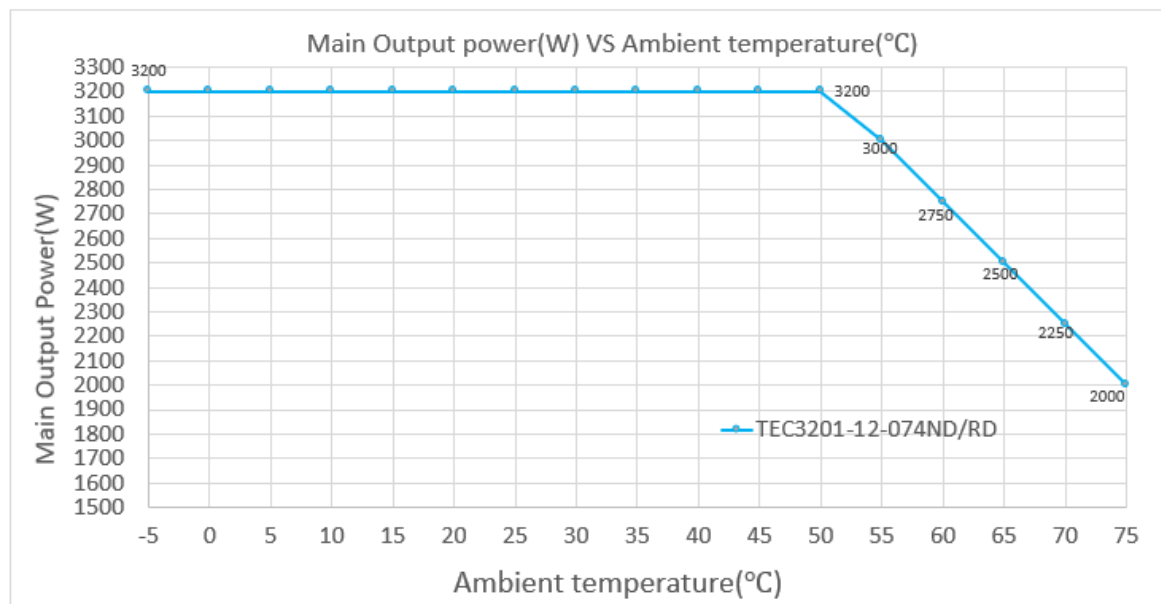
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12. ENVIRONMENTAL SPECIFICATION

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	$V_{I \min}$ to $V_{I \max}$, $I_{I \text{ nom}}$, $I_{SB \text{ nom}}$ below 1800 meters Altitude		+50	°C
$T_{A \text{ ext}}$	Extended Temp. Range	Derated output		+75	°C
T_s	Storage Temperature	Non-operational		+75	°C
	Altitude	Operational, above Sea Level, refer derating to T_A		4000	m
	Humidity	(Operating) non-condensing		90	%
N_a	Audible Noise	Sound power @ $V_{I \text{ nom}}$, 50% $I_{O \text{ nom}}$, $T_{\text{amb}} = 25^\circ\text{C}$		50.06	dBA

Output power derating curve:



13. MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		73.5		mm
	Height		40.0		mm
	Depth		185		mm
Weight			1.1		kg



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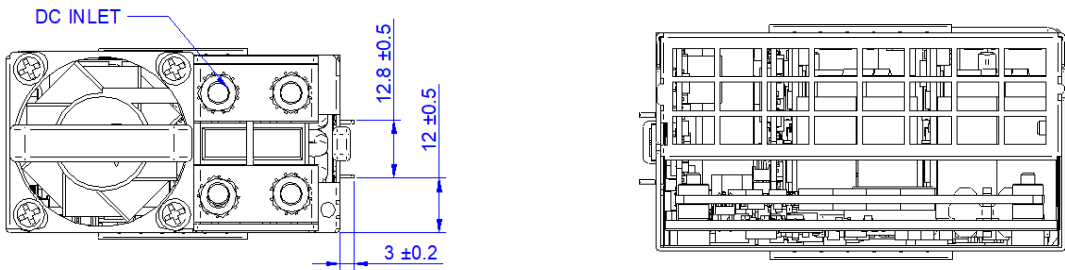


Figure 19. Front and back view

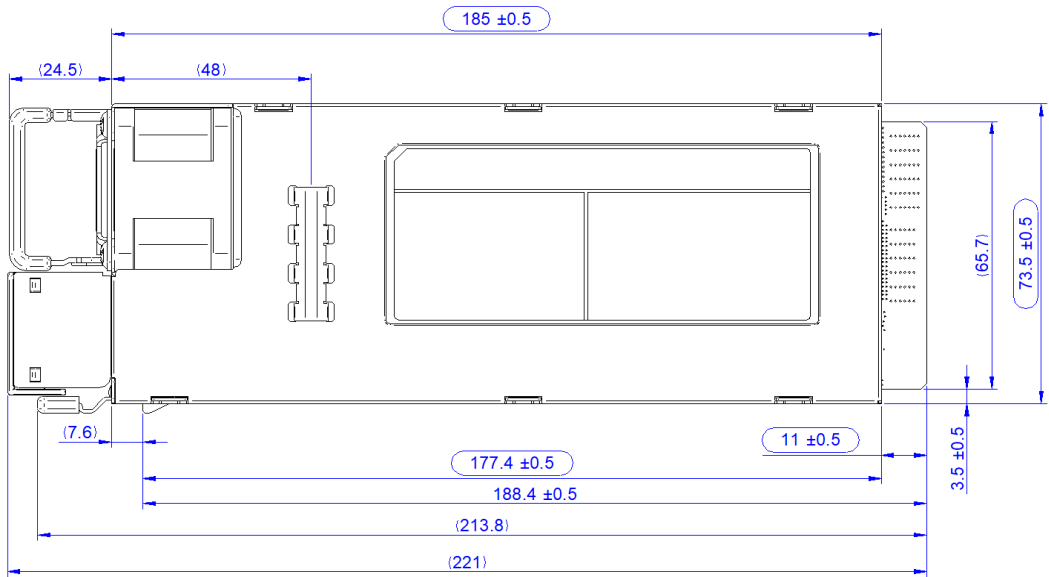


Figure 20. Top view

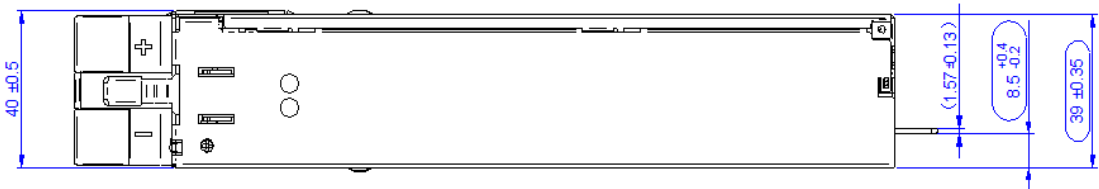


Figure 21. Side view 1

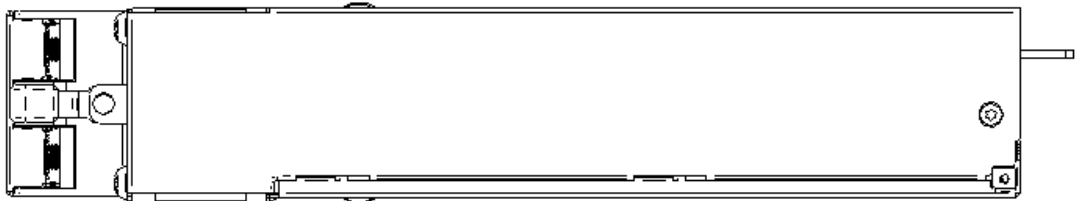


Figure 22. Side view 2



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14. CONNECTORS

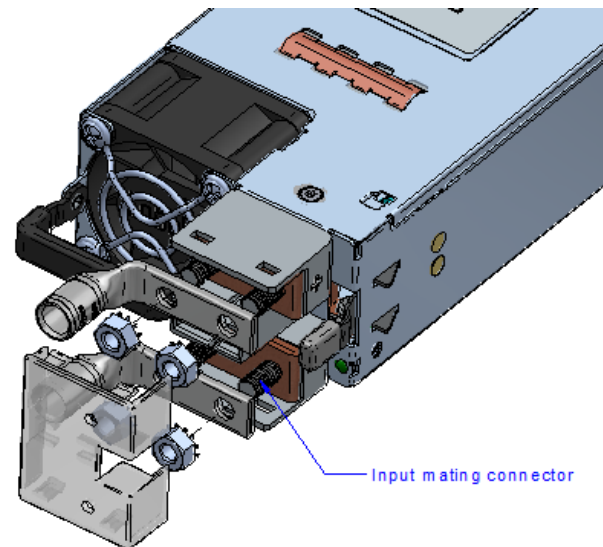


Figure 23. Input mating connector

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Input connector	Copper busbar with #10-32 bolt				
Mating Input connector screw	#10-32 nut (contains the washer) Recommended torque force for the #10 nut is 10-12kgf-cm				
Input DC cord requirement	Wire size		4		AWG
Mating input connector	Manufacturer : BURNDY Manufacturer P/N : YAV4CL2NT10FX(straight) Or YAV4CL2NT10FX90(right angle) Or Equivalent				
Output connector	PCB card edge				
Mating output connector	Manufacturer : AMPHENOL Manufacturer P/N: HPG12P14SRT153T or equivalent.				

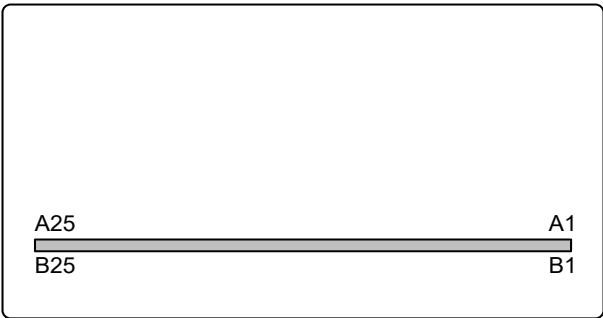


Figure 24. Power supply connector pinout



Output Pin Assignment

PIN	SIGNAL NAME	DESCRIPTION
A1 ~ A9	GND	Power and signal ground (return)
B1 ~ B9	GND	
A10 ~ A18	V1	+12 VDC main output
B10 ~ B18	V1	
A19	SDA	I ² C data signal line
A20	SCL	I ² C clock signal line
A21	PSON_L	Power supply on input, active-low
A22	SMB_ALERT_L	SMB Alert signal output, active-low
A23	V1_SENSE_R	Main output negative sense
A24	V1_SENSE	Main output positive sense
A25	PWOK_H	Power OK signal output, active-high
B19	A0	I ² C address selection input
B20	A1	
B21	VSB	+12 V Standby positive output
B22	HOTSTANDBYEN_L	Hot standby enable signal, active-high
B23	ISHARE	Analog current share bus
B24	PRESENT_L	Power supply seated, active-low
B25	INPUT_OK_H	Input OK signal output, active-high

Table 6 Output connector pin assignment



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15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	Evaluation Board Connector board to operate TEC3201-12-074xD. Includes an onboard USB to I2C converter (use I2C Utility as desktop software)	YTM. G6901.0	Bel Power Solutions

It is recommended to add each a width 18 mm x thickness 3 mm x length 40 mm busbar for Main output +/- on loading board as such high output current density.

16. REVISION HISTORY

DATE	REVISION	CHANGES / UPDATES	ECO/MCO REFERENCE NO.
2025/04/16	001	Preliminary release	
2025/07/16	002	1. Section15 Recommend adding two busbars for Main output +/- on loading board.	
2026/06/30	A	1. Update OCW1 trip timing and current range. 2. Update OCP1 trip current range. 3. Update OTW and OTP setpoints.	CO149509

For more information on these products consult: powersupport@belf.com

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TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.



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