TQPX8M12B

Isolated DC-DC Converter

The TQPX8M12B series are isolated DC/DC converters that provide up to 1800 W of output power from a nominal 54 VDC input.

These converters are intended to provide isolation and step down to generate a regulated intermediate bus for the purpose of powering non-isolated Point-of-Load (POL) converters.

These converters are provided in 1/4th brick package.

RoHS Compliant

Key Features & Benefits

- 48 – 60 VDC Input
- 12 VDC Output
- Thermal Design Power up to 1800 W
- Peak Power up to 2500 W (≤ 1 second)
- High Efficiency
- Remote On/Off
- Power Good Function
- Power Management Bus
- Black-Box Functionality
- Approved to EN/IEC 62368-1
- Approved to CSA/UL 62368-1
- Class II, Category 2, Isolated DC/DC Converter (refer to IPC-9592B)

Applications

- Networking
- Computers and Peripherals
- Telecommunications

1. MODEL SELECTION

MODEL NUMBER	OUTPUT VOLTAGE	INPUT VOLTAGE	MAX. OUTPUT CURRENT	MAX. OUTPUT POWER	TYPICAL EFFICIENCY
TQPX8M12B Series	12 VDC	48 – 60 VDC	150 A	1800 W	97%

PART NUMBER EXPLANATION

T	QP *	X8	M	12	B	-	L	N	x	T
Mounting Type	Series Name	Output Power	Input Range	Output Voltage	Thermal Solution		Active Logic	Sense/Trim	Pin configuration	Package Type
Through Hole Mount	1/4th Brick	1800 W	48 – 60 V	12 V	Baseplate		Active Low	None	A – Pin length 0.18", with PG, 7-pin Power Management Bus B – Pin length 0.145", with PG, 7-pin Power Management Bus C – Pin length 0.110", with PG, 7-pin Power Management Bus D – Pin length 0.18", no PG, 4-pin Power Management Bus	Tray Package

* Power Management Bus

2. ABSOLUTE MAXIMUM RATINGS

	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_I	Input Voltage Continuous		-0.3	–	60	V
V_{tr}	Input Voltage Transient (t ≤ 100 ms)		-	–	80	V
V_{RM}	Remote On/Off pin Voltage		-0.3	-	16	V
V_{DAT}	Data pin Voltage		-0.3	-	3.3	V
V_{CLK}	CLK pin Voltage		-0.3	-	3.3	V
V_{Alert}	Alert pin Voltage		-0.3	-	3.3	V
V_{Addr0}	Addr0 pin Voltage		-0.3	-	3.3	V
V_{Addr1}	Addr1 pin Voltage		-0.3	-	3.3	V
V_{C2}	C2 pin Voltage		-0.3	-	15	V
V_{PG}	PG pin Voltage		-0.3	-	15	V
Ta	Ambient Temperature Long-Term	See Note 1	-20	-	85	°C
Tas	Ambient Temperature Short-Term	See Note 2	-20	-	90	°C
T_S	Storage Temperature		-40	-	100	°C
AT	Altitude		-500	-	16404	feet
RH	Humidity		10	85	90	%

Note 1: All components on the Unit meet IPC-9592 (latest revision) derating guidelines.

Note 2: (96 hours/year). Unit's component temperatures exceed IPC-9592 (latest revision) derating guidelines but not exceed component temperature ratings.

Note: Ratings used beyond the maximum ratings may cause a reliability degradation of the converter or may permanently damage the device.

3. INPUT SPECIFICATIONS

All specifications are typical at 25°C unless otherwise stated.

	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{IN}	Operating Input Voltage		48	54	60	V
I_{IMAX}	Input Current (full load)	P_O = 100% of P_{OTDP}	-	-	43	A
I_{Iid}	Input Current (no load)	Input idling current, P_O = 0 W	-	170	200	mA
I_{Ioff}	Remote Off Input Current		-	20	35	mA
I_S	Input Reflected Ripple Current (rms)	See Note 1	-	30	50	mA
I_S	Input Reflected Ripple Current (pk-pk)	See Note 1	-	240	300	mA
I_C	Input Terminal Ripple Current (rms)	See Note 1	-	1900	2300	mA
	Input Terminal Ripple Current over Temperature (rms)	Ta = -20 to 85°C	-	3	15	mA
C_{II}	Internal Input Capacitance		-	33.6	-	µF
C_{IN}	Recommended Input Capacitor		220	430	660	µF
V_{IoffL}	Input Turn off Voltage Threshold		42.5	44	45	V
V_{IonL}	Input Turn on Voltage Threshold		45	47	48	V
$V_{UV(hys)}$	Hysteresis Voltage		2	-	-	V
V_{IoffH}	Over-Voltage Shutdown Threshold	See Note 2	63	65	67	V
	Recommended input fast-acting fuse on system board	See Note 3	60	-	-	A

Note 1: Refer to section 8 for detail input capacitance and waveforms.

Note 2: Shutdown after 100 ms if V_{IoffH} < Vin < 80 V; Shutdown immediately if Vin > 80 V, hiccup mode.

Note 3: This converter is not internally fused. An input line fuse must be used in application.

4. OUTPUT SPECIFICATIONS

All specifications are typical at nominal input, full load at 25°C unless otherwise stated.

	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_O	Output Voltage Set Point	Vin = 54 V, P_O = 50% of P_{OTDP}	11.88	12	12.12	V
	Output Voltage Total Range	Vin = 48~60 V, Pout = 0~P_{OTDP}	11.2	-	12.12	V
	Load Regulation	Vin = 54 V, P_O = 0~100% of P_{OTDP}	-	0.01	0.02	V
	Line Regulation	Vin = 52~60 V, P_O = 100% of P_{OTDP}	-	10	30	mV
	Regulation Over Temperature	Vin = 54 V, P_O = 100% of P_{OTDP}, Ta = -20 to 85°C	-	100	-	mV
V_{OAC}	Ripple and Noise (pk-pk)	P_O = 100% of P_{OTDP}, See Note 1	-	30	50	mV
V_{ORMS}	Ripple and Noise (rms)	P_O = 100% of P_{OTDP}, See Note 1	-	10	30	mV
V_{OAC}	Output Ripple and Noise (pk-pk) under worst case	All operating input voltage, load and ambient temperature condition.	-	-	80	mV
I_O	Output Current Range		0	-	150	A
I_{OMAX}	Output DC Current Limit	See Note 2	160	180	210	A
P_{OTDP}	Output Power (TDP)	See Note 2	-	-	1800	W
P_{OMAX}	Output Power Peak (t ≤ 1 s)	See Note 2	-	-	2500	W
t_r	Rise Time	See Note 3	-	-	20	ms
t_{s1}	Turn on Time from Vin	See Note 4	-	45	60	ms
t_{s2}	Turn on Time from RM	See Note 5	-	10	30	ms
V_{Pre}	Pre-bias Voltage		-	-	12	V
V_{OS}	Overshoot at Turn on		-	-	3	%
V_{US}	Undershoot at Turn off		-	-	3	%
C_{out}	Output Capacitance	50% ceramic, 50% POSCAP.	270	1800	10000	µF
V_{tr}	Load Transient Voltage Deviation	Load step 50~75~50% P_{OTDP}, di/dt = 1 A/µs. Cout setup please See Note 1	-	±350	-	mV
t_{tr}	Load Transient Recovery Time		-	500	-	µs

Note 1: Cout = 4x 270 µF POSCAP capacitor + 33 x 22 µF ceramic capacitor + 1 µF ceramic capacitor.

Note 2: The maximum output current is rated to 210 A. The maximum power is ≤ 2500 W (t ≤ 1 s) and the continuous power (TDP, Thermal Design Power) is ≤ 1800 W, depending on thermal conditions.

Note 3: Defined as time between V_O at 0% of final value and V_O at 90% of final value.

Note 4: Defined as time between Vin reaching Turn-On voltage and V_O reaching 90% of final value.

Note 5: Defined as time between Remote on and V_O reaching 90% of final value.

5. GENERAL SPECIFICATIONS

	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
η	Efficiency		-	97.3	-	%
f_{SW}	Switching Frequency	Primary FETs	-	150	-	kHz
	MTBF	Vin= 54 V, P_O = 80% of P_{OTDP}, 25°C	-	6.8	-	Mhrs
		Vin = 54 V, P_O = 80% of P_{OTDP}, 40°C	-	4.6	-	Mhrs
		Vin = 54 V, P_O = 80% of P_{OTDP}, 85°C	-	1.1	-	Mhrs
T_P	Over Temperature Protection	Auto-recovery.	-	130	-	°C
V_{OV}	Output Over Voltage Protection		-	-	15	V
G	Weight		-	87	-	g
	Dimensions (L × W × H)			2.30 x 1.45 x 0.57		inch
				58.42 x 36.83 x 14.50		mm
	Isolation Characteristics					
V_{IIO}	Input to Output		-	-	500	VDC
V_{IIC}	Input to Case		-	-	500	VDC
V_{IOC}	Output to Case		-	-	500	VDC
R_{ISO}	Isolation Resistance		10M	-	-	Ohm
C_{IC}	Isolation Capacitance		-	2700	-	pF

6. TYPICAL CHARACTERISTICS

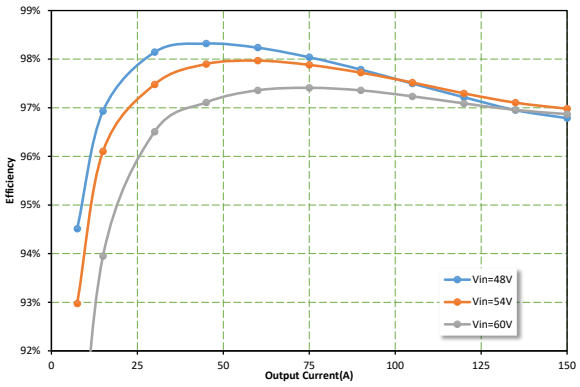


Figure 1. Efficiency

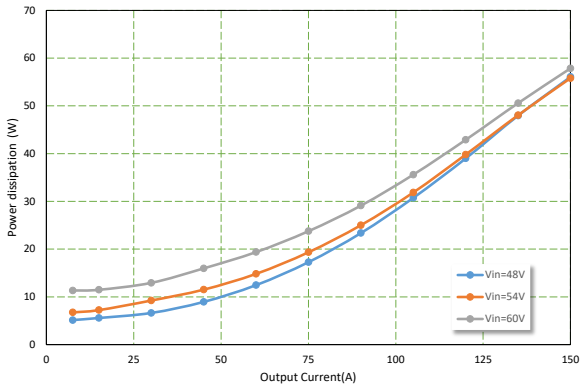


Figure 2. Power Dissipation

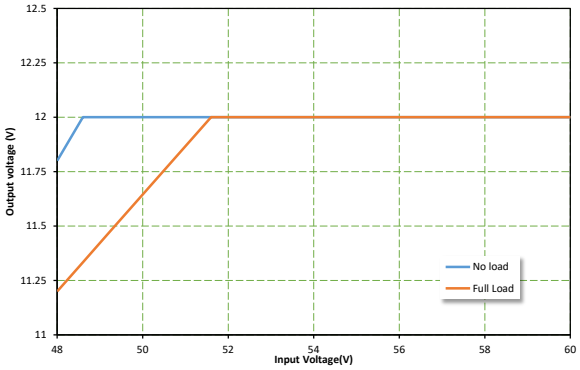


Figure 3. Line Characteristics

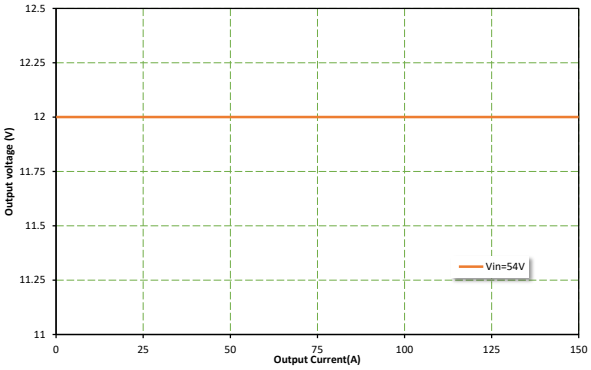


Figure 4. Load Characteristics

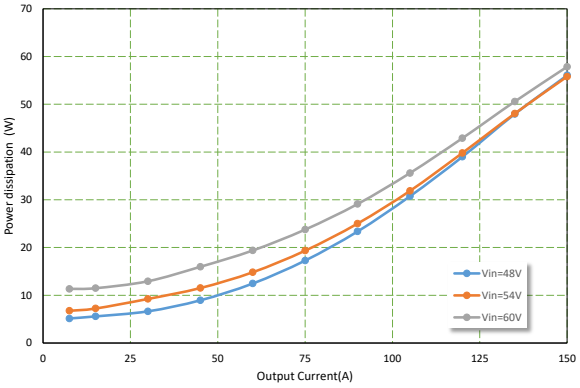


Figure 5. Power Loss @ max temperature

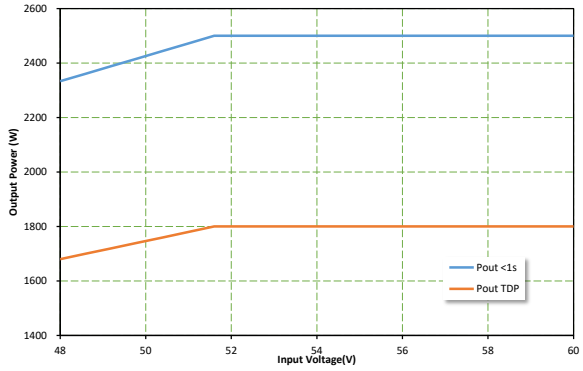


Figure 6. Available Power

7. FUNDAMENTAL CIRCUIT DIAGRAM

The product is a typical full bridge circuit design, the turn ratio of transformer is 4:1, so in theory, when the input voltage is lower than 48 V, it will not be able to continue to output 12 V. The relationship between input and output refer to Line Characteristics curve.

The primary side and the secondary side all use bridge rectifier design, it can effectively reduce the stress of MOSFET. In addition, C_2 can effectively prevent the failure due to transformer (T_1) magnetic bias.

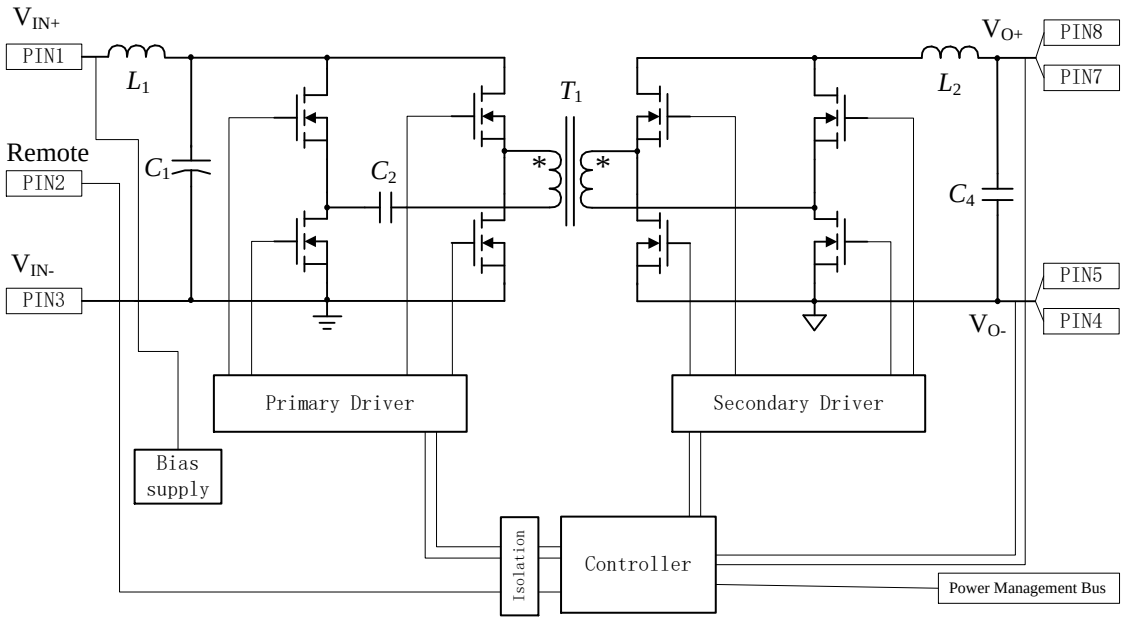


Figure 7. Block Diagram

8. TYPICAL WAVEFORM

Typical Electrical Characteristics measured according to figure below.

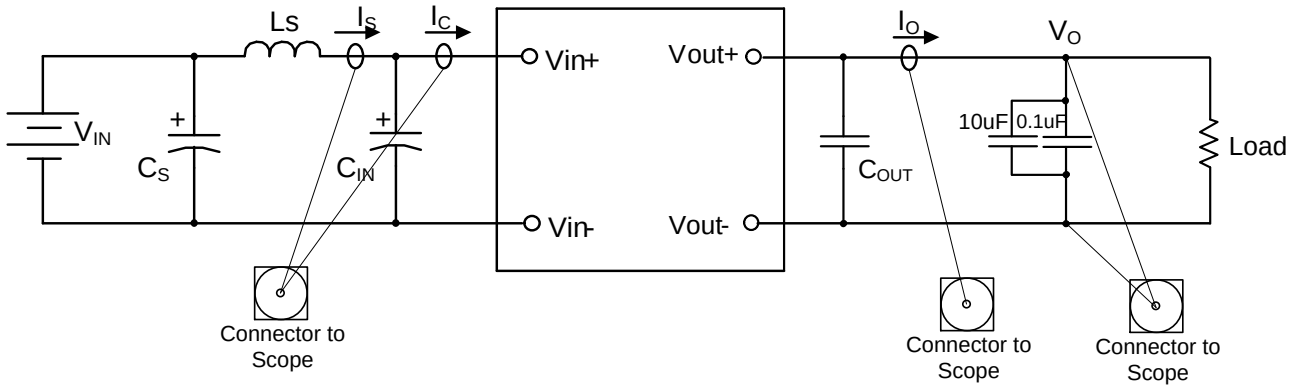


Figure 8. Test Setup

Notes and values in testing:

I_S: Input Reflected Ripple Current, measure by current probe.
I_C: Input Terminal Ripple Current, measure by current probe.
I_O: Output Current, measure by current probe.
V_O: Output Voltage. Measure by voltage probe.
Ls: Simulated Source Impedance (10 µH).
C_S: Offset possible source Impendence (100 µF, ESR < 0.2 Ω @ 100 kHz).
C_{IN}: Electrolytic capacitor, should be as close as possible to the power module to damp IC ripple current and enhance stability. Refer to the input specifications chapter TYP value of C_{IN}.
C_{OUT}: Refer to the output specifications chapter TYP value of C_{OUT}.
V_{IN}: Typical input 54 V.

To improve the accuracy of measurement, a short ground loop is used for measurement, and place 10 µF and 0.1 µF capacitors near the measuring point, use 20 MHz bandwidth for measurement. The correct probe technique is shown in figure below.

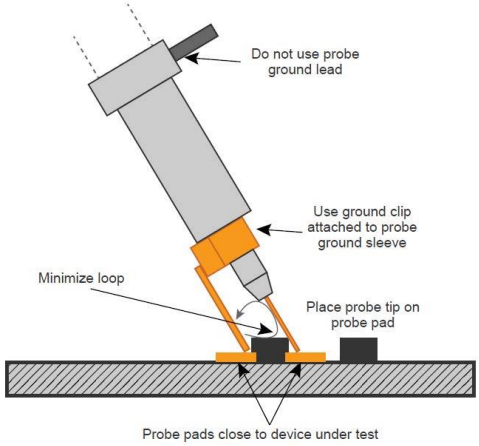


Figure 9. Input Reflected Ripple Current

Input Noise

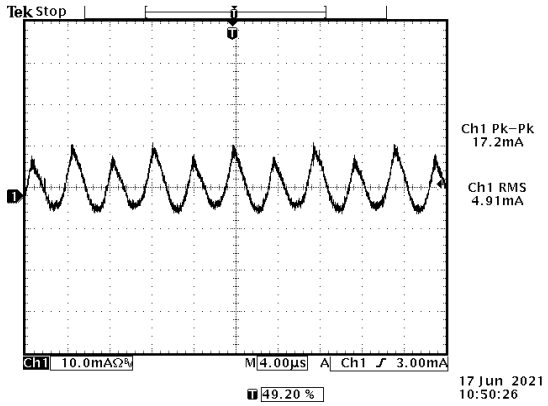


Figure 10. I_S, P_O = 100% of P_{OTDP}

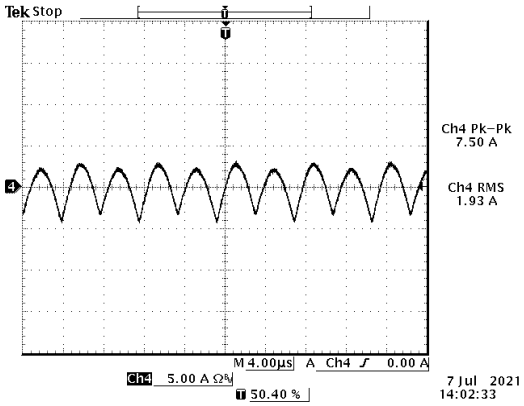


Figure 11. I_C, P_O = 100% of P_{OTDP}

Output Noise

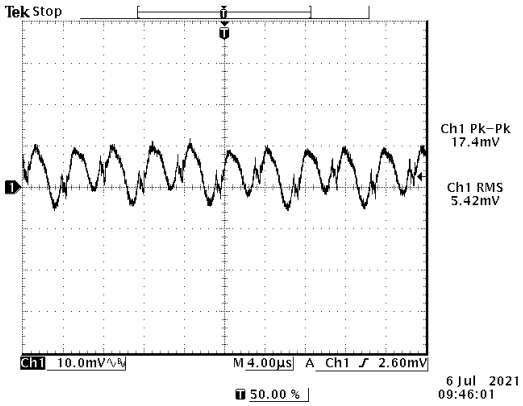


Figure 12. V_{OAC}, P_O = 0% of P_{OTDP}

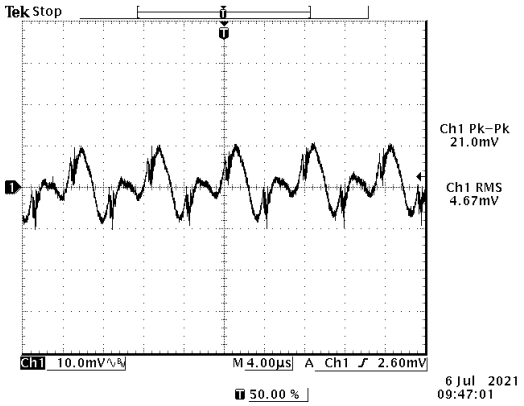


Figure 13. V_{OAC}, PO = 100% of P_{OTDP}

Load Transient

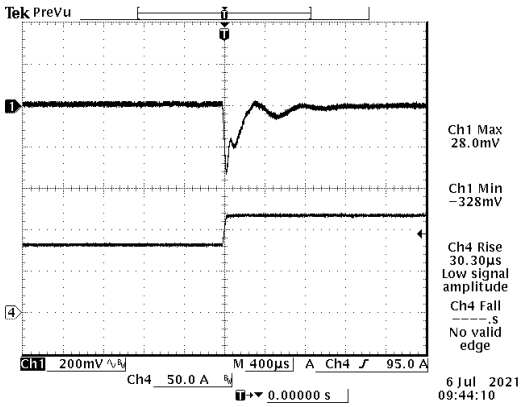


Figure 14. V_{tr}, 50%-75% Load Transients

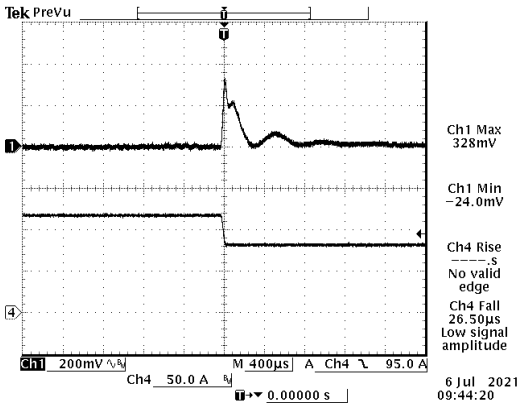


Figure 15. V_{tr}, 75%-50% Load Transients

Startup and Shutdown

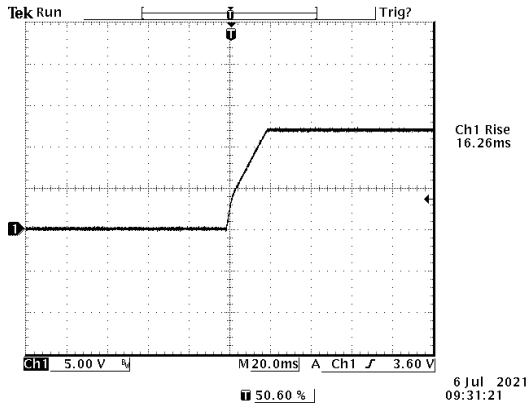


Figure 16. Startup, P_O = 100% of P_{OTDP}

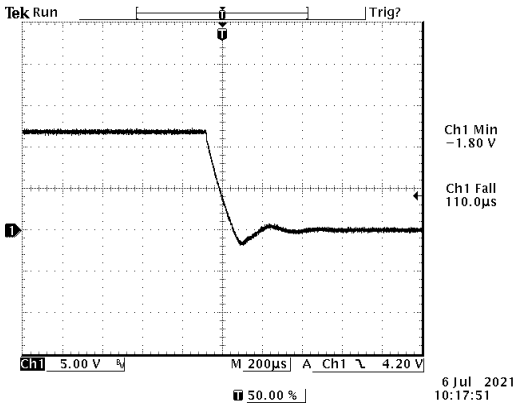


Figure 17. Shutdown, P_O = 100% of P_{OTDP}

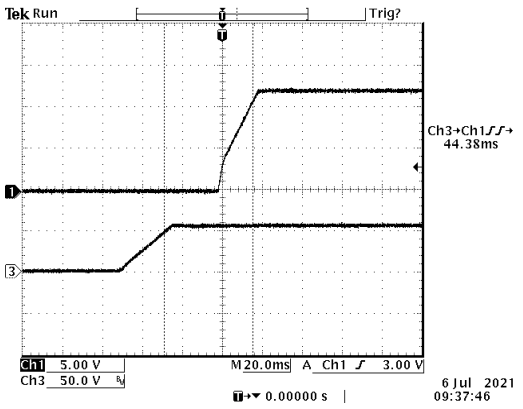


Figure 18. Startup from Vin, P_O = 100% of P_{OTDP}

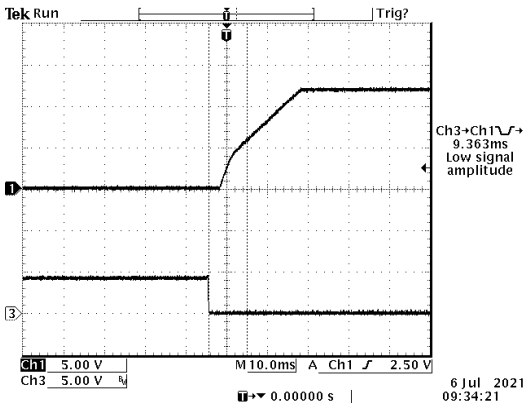


Figure 19. Startup from on/off, P_O = 100% of P_{OTDP}

Input voltage transient 80V (t ≤ 100 ms)

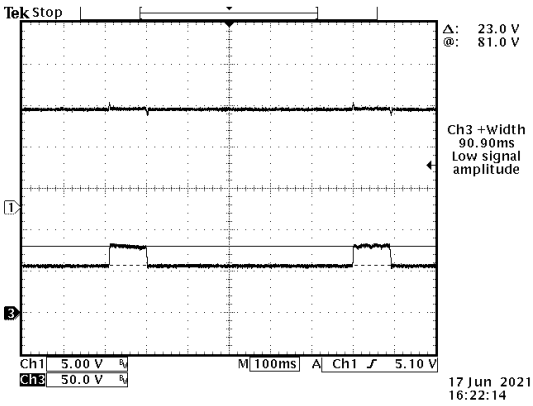


Figure 20. Input and Output Voltage Waveform, P_O = 100% of P_{OTDP}

Output power Peak (t ≤ 1 s)

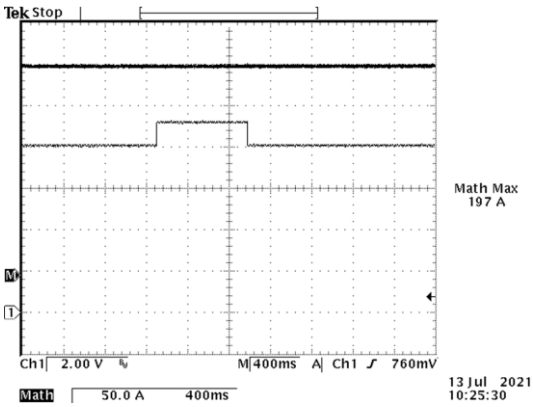


Figure 21. Output Voltage and Current Waveform, P_O = 100% of P_{OTDP} ~P_{OMAX}~ 100% of P_{OTDP}

9. REMOTE ON/OFF

	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{RML}	Signal Low	Remote On/Off pin is open, the module is off.	-0.3	-	0.8	V
V_{RMH}	Signal High		2.4	-	16	V
I_{RML}	Source Current	V_{REMOTE} = 0 V	-	100	150	µA
I_{RML}	Source Current	V_{REMOTE} = 2.4 V	-	60	100	µA
I_{RMH}	Sink Current	V_{REMOTE} = 10 V	-	-250	-300	uA
I_{RMH}	Sink Current	V_{REMOTE} = 16 V	-	-350	-500	µA
V_{RMF}	Open Circuit Voltage		-	12	16	V

Products has a remote-control function referenced to the primary negative input connection (V_{IN}-), with negative and positive logic options available. Remote on/off function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. Remote on/off pin has an internal pull up resistor to internal 10~12 V. External device must provide a minimum required sink current > 0.15 mA to guarantee a voltage not higher than maximum voltage of Signal low (V_{RML})on the Remote on/off pin.

Recommended remote on/off circuit for active low:

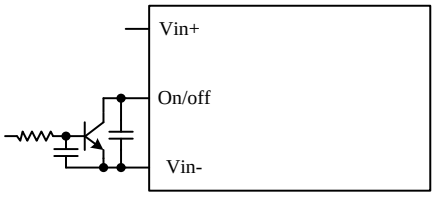


Figure 22. Control with open collector/drain circuit

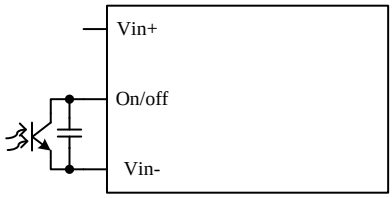


Figure 23. Control with photocoupler circuit

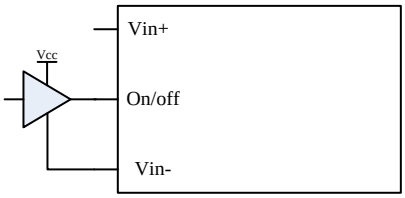


Figure 24. Control with logic circuit

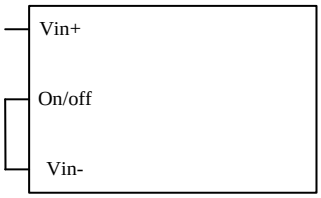


Figure 25. Permanently on

10. POWER GOOD

1. The Power Good signal (PG) is a non-latching open-drain output, that means need to add an external pull-up resistor. PG is pulled to Low during normal operation and is pulled to High when any of the following conditions occur:
   - Over-Temperature.
   - Over-Current.
   - Vout is outside of the DC Output Band while Vin is within the Vin Operating Range.
2. The Power Good signal is referenced to Vout (-).
3. The PG pin is internal connect to C2 pin.

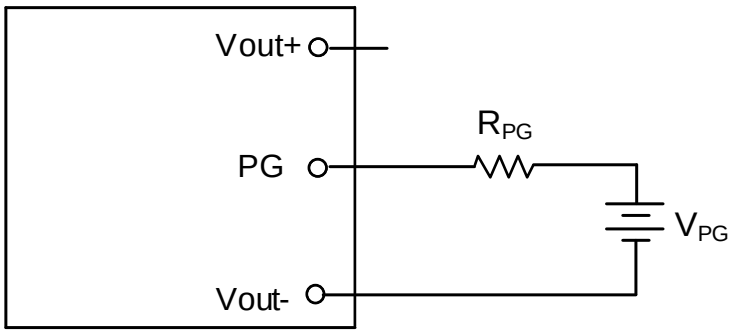


Figure 26. Power Good external pull-up circuit

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{PG}		5	-	15	V
Output Voltage Low (trigger limits)		9	-	10	V
Output Voltage High (trigger limits)		14	-	15	V
Over-Temperature (trigger limits)		128	-	132	°C
Over-Current (trigger limits)	See Note 1	175	-	185	A
Hysteresis		-	1	-	V
High State Voltage		0	-	V_{PG}	V
High State Leakage Current (into Pin)		0	-	10	µA
Low State Voltage		0	-	0.8	V
Low State Current (into Pin)		0	-	5	mA

Note 1: PG signal can only be triggered when the output current reaches the alarm point of over current and exceeds 1.2 s.

11. ALERT

1. The ALERT signal is a non-latching open-drain output, that means need to add an external pull-up resistor. ALERT is pulled to High during normal operation and is pulled to Low when any of the following conditions occur:
   - Over-Temperature warning.
   - Over-Current warning.
   - Vout is outside of the DC Output Band while Vin is within the Vin Operating Range.
   - Vin is outside of the Vin Operating Range.
2. The ALERT signal is referenced to Vout (-).
3. After the Alert level signal is triggered and flipped, it will remain in this state. When the module returns to normal, the alert level can be restored to normal by restarting the module or by inputting the command II2C to clear the signal.

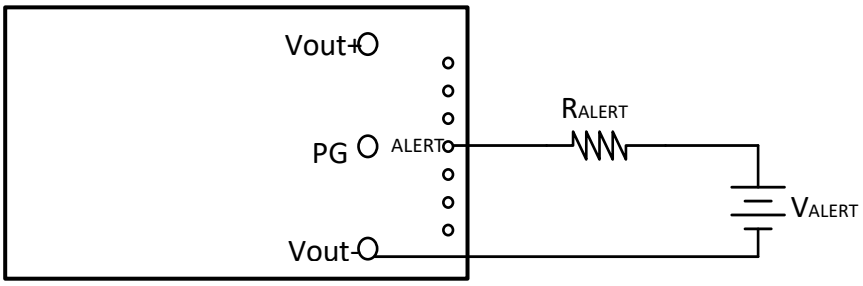


Figure 27. ALERT external pull-up circuit

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Output Voltage Low (trigger limits)		10	-	11	V
Output Voltage High (trigger limits)		13	-	14	V
Over Temperature (trigger limits)		123	-	127	°C
Over Current (trigger limits)	See Note 1	165	-	175	A
Input Voltage Low (trigger limits) Rising		44	-	48	V
Input Voltage High (trigger limits) Rising	See Note 2	62	-	66	V
Hysteresis		-	1	-	V
High State Voltage		0	-	3.3	V
High State Leakage Current (into Pin)		0	-	10	µA
Low State Voltage		0	-	0.8	V
Low State Current (into Pin)		0	-	5	mA

Note 1: ALERT signal is triggered when the output current reaches the alarm point of over current and exceeds 1.3 s.

Note 2: ALERT signal is triggered when the input voltage reaches the alarm point of over voltage and exceeds 0.1 s.

12. INPUT UNDER-VOLTAGE LOCKOUT

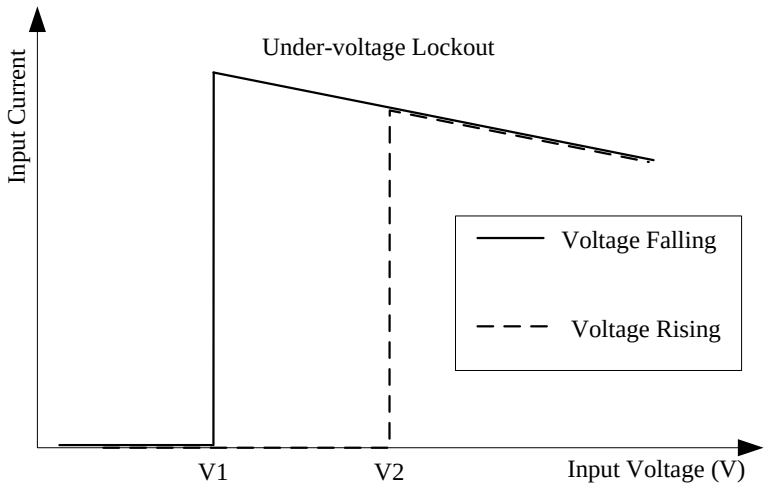


Figure 28. Input under-voltage lockout

V1 = 44 V; V2 = 47 V

13. OVER CURRENT PROTECTION

To provide protection in a fault output overload condition, the module is equipped with internal over current protection circuitry. If the over current condition occurs, the module will shut down into hiccup mode and restart once every 250 ms. The module operates normally when the output current goes into specified range.

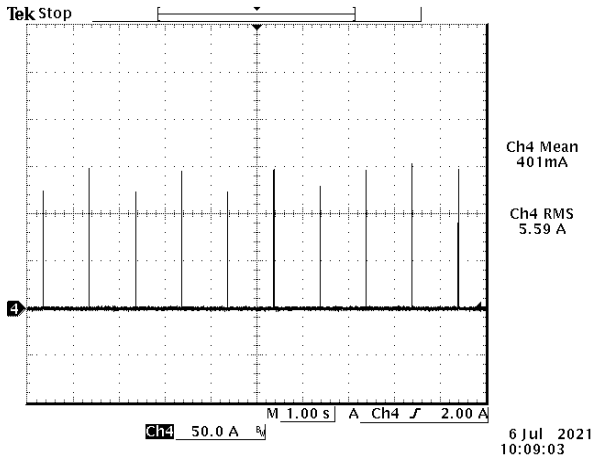


Figure 29. Over current protection
Vin = 54 V @ Ta = 25°C

14. LAYOUT RECOMMENDATIONS

The heat dissipation performance of the product depends not only on the heatsink of the product, but also on the layout of the motherboard in application. The motherboard is often large and can act as a good heatsink, power product can transfer heat to the motherboard through the pin. Therefore, good thermal conductivity should be ensured between the power product and the motherboard. Therefore, it is recommended to use multi-layer PCB for motherboard, expand the area of input and output as much as possible, and place many through holes around input and output pins. At the same time, it is an isolation product, so the layout of the motherboard must fully consider the isolation area. Here is a recommendation of motherboard layout.

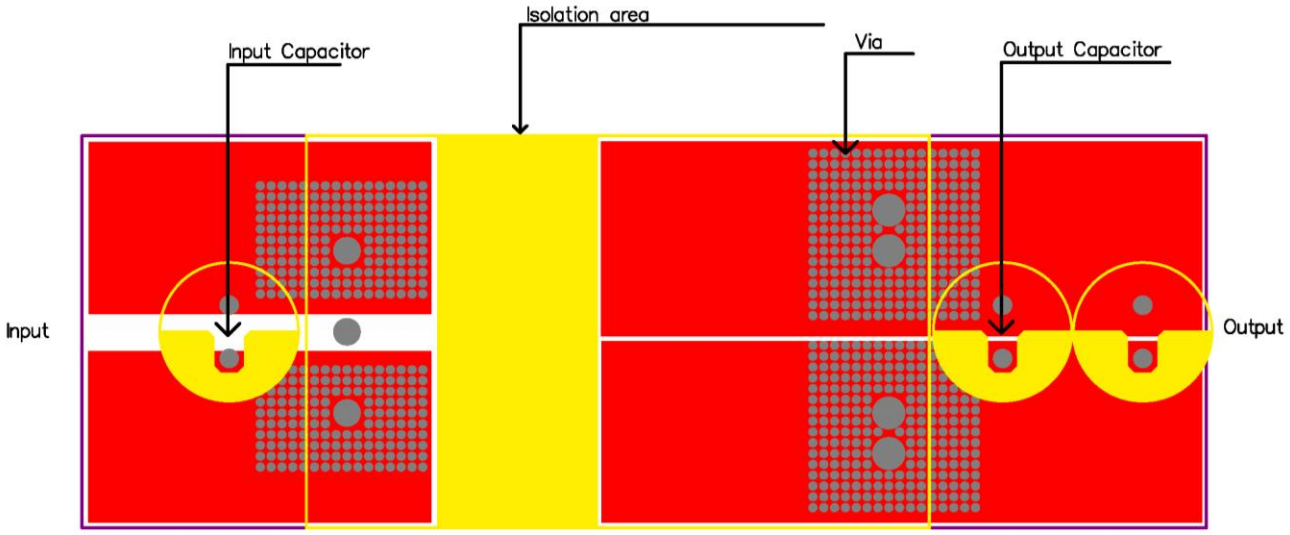


Figure 30. Recommendation of motherboard layout

15. THERMAL DERATING CURVES

The product is designed for different thermal environments, and sufficient cooling environment must be provided to ensure reliable operation. High power output requires external cooling, such as heatsink or cold wall.

If an additional heatsink is used, the teeth and slots at the top of the heatsink should not collide with the wind, that is, the direction of teeth and slots at the top of the heatsink should parallel to the direction of the wind blowing. If the design of the product is changed, for example, the direction of the wind is rotated by 90 degrees, the teeth and slots at the top of the heatsink should be redesigned to ensure the same thermal performance. Typical thermal measured according to figure below.

THERMAL TEST SETUP

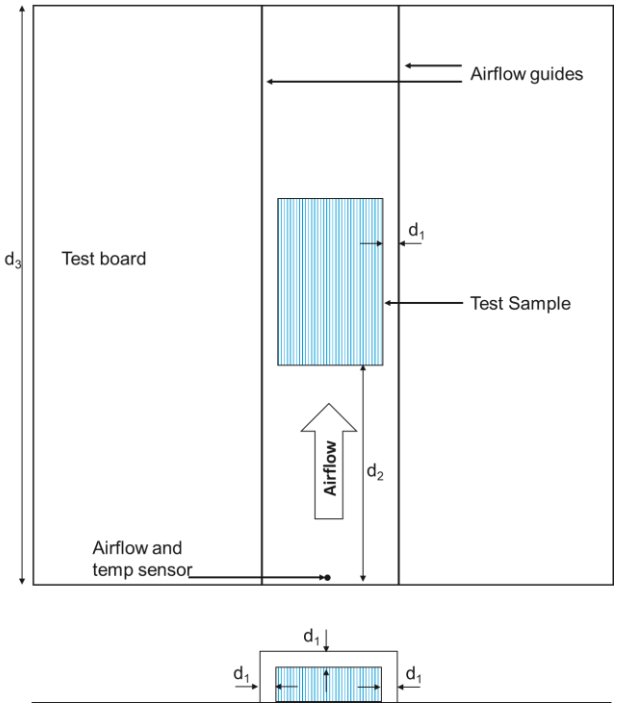


Figure 31. Thermal test setup, Airflow from V_O to V_{IN}

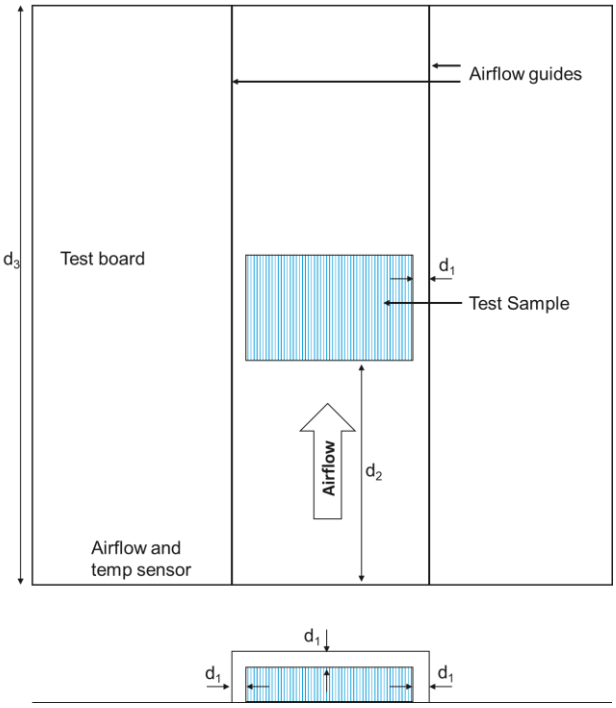


Figure 32. Thermal test setup, Airflow from Vo_- to Vo_+

d_1: The distance is 6.35 mm (0.25 inch) from the top of the module and 6.35 mm (0.25 inch) on the left and right side of the module.

d_2: Ambient temperature and airflow are measured in front of the module at the distance of 76.2 mm (3 inch).

d_3: Product is tested on an 8”×8”, Internal 105 um (3 oz), outside 70 um (2 oz), 6-layer test board mounted in a wind tunnel.

V_{IN}: 54 V.

Airflow: test at 200 LFM, 400 LFM and 600 LFM.

Test without heatsink (baseplate only) or use external heatsink which size is 2.30”×1.45”×0.7”, and the teeth and slots at the top of the heatsink has two different kinds, long teeth and short teeth show as follow.

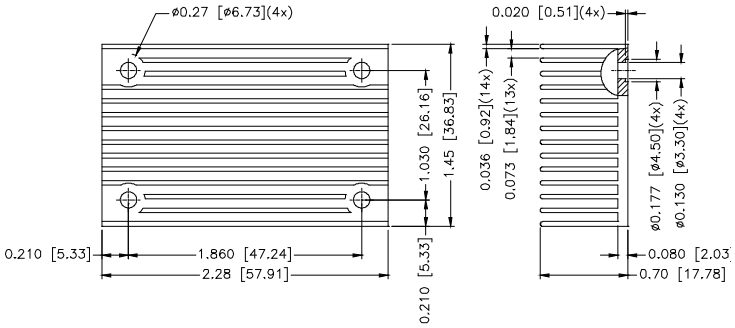


Figure 33. Heatsink with long slot for Airflow from V_O to V_{IN}

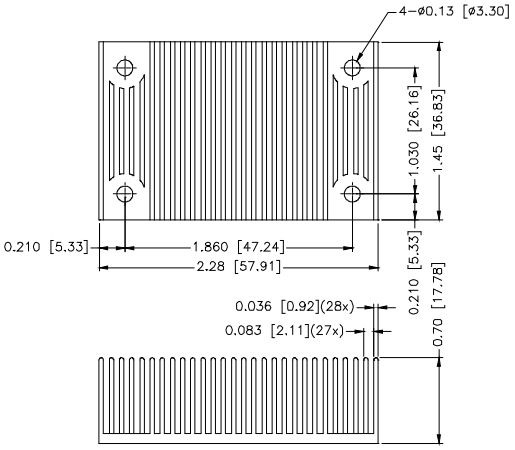


Figure 34. Heatsink with short slot for Airflow from V_{O-} to V_{O+}

Hot spot location and allowed maximum temperature:

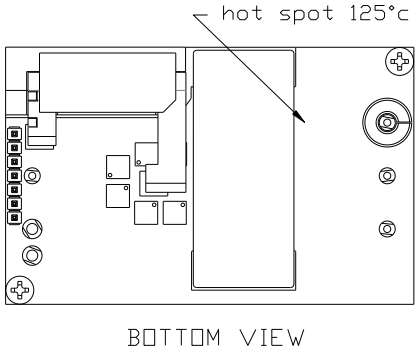


Figure 35. Module bottom view hot spot

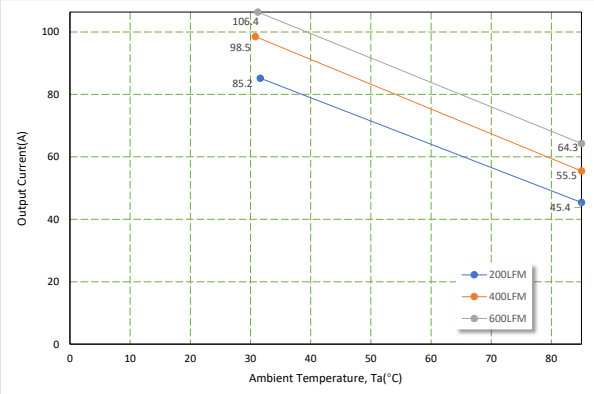


Figure 36. Thermal derating curve – Baseplate, Airflow from V_O to V_{IN}

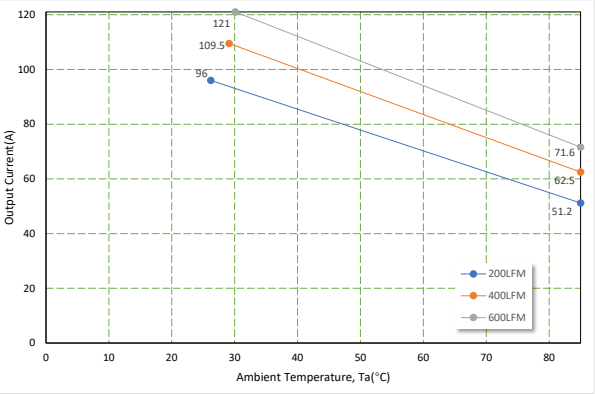


Figure 37. Thermal derating curve – Baseplate, Airflow from V_{O-} to V_{O+}

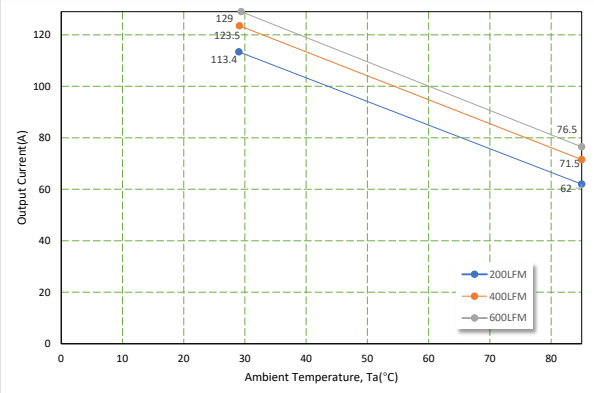


Figure 38. Thermal derating curve – Heatsink, Airflow from V_O to V_{IN}

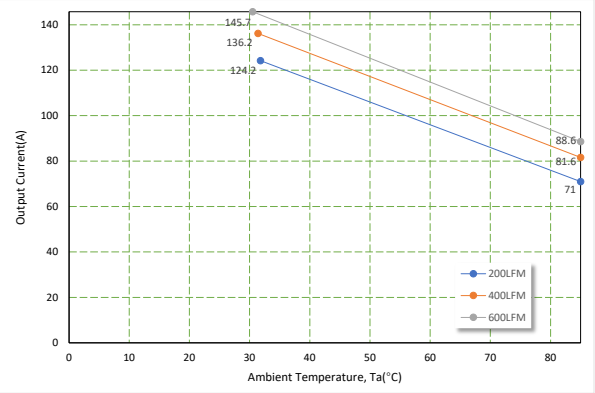


Figure 39. Thermal derating curve – Heatsink, Airflow from V_{O-} to V_{O+}

16. POWER MANAGEMENT BUS

POWER MANAGEMENT BUS DIGITAL FEATURE DESCRIPTION

The module supports Power Management Bus to allow to be monitored, controlled and configured by the system. More detailed Power Management Bus information can be found in the Power Management Bus Power Management Protocol Specification, Part I and part II, revision 1.2, which is shown in the System Management Interface Forum Web site: www.powerSIG.org. The supported Power Management Bus commands of the module are listed below in the supported Power Management Bus commands section. The module supports four Power Management Bus signal lines: Data (Data pin), Clock (CLK pin), SMBALERT (Alert pin, optional), Control (C2 pin, optional), and two Address lines: Addr1 and Addr0 (optional). Connection for the Power Management Bus interface should follow the High-Power DC specifications given in section 3.1.3 in the SMBus specification V2.0 or the Low Power DC specifications in section 3.1.2. The complete SMBus specification is shown in http://smbus.org.100 kHz communication bus speed is preferred.

SMBALERT protocol is also supported by the module. SMBALERT line is also a wired-AND signal, by which the module can alert the Power Management Bus master via pulling the SMBALERT pin to an active low. There is only one way that the master and the module response to the alert of SMBALERT line. The master will communicate with the slave module using the programmed address, and using the various READ_STATUS commands to find the cause for the SMBALERT. The CLEAR_FAULTS command will clear the SMBALERT.

The module also supports the Packet Error Checking (PEC) protocol. It can check the PEC byte provided by the Power Management Bus master, and include a PEC byte in all message transmitted back to the master.

Power Management Bus Addressing

The Module has flexible power management bus addressing capability. When connect different resistor from Addr0 and Addr1 pin to DGND pin, 64 possible addresses can be acquired. The address is in the form of octal digits; Each pin offers one octal digit, and then combine together to form the decimal address as shown in below.

Address = 8 * ADDR1 + ADDR0.

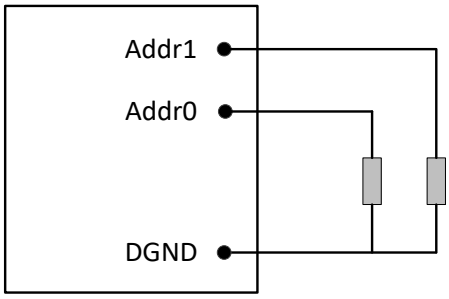


Figure 40.

Octal digit	Resistor (kohm)
0	10
1	15.4
2	23.7
3	36.5
4	54.9
5	84.5
6	130
7	200

Corresponded to each octal digit, the requested resistor values are shown in below, and +/-1% resistors accuracy can be accepted. If there are any resistances exceeding the requested range, address 64 will be return. 0-12 and 40, 44, 45, and 55 in decimal address cannot be used, since they are reserved according to the SMBus specifications, and which will also return address 64.

Power Management Bus Addressing (for TQPX8M12B-LNDT)

The Module has configurable Power Management Bus addressing capability. By connecting different resistors from Addr1 pin to Vout(-) pin, 14 possible addresses can be acquired. The 7 bit Power Management Bus address is defined by the value of the resistor as shown in the table below, and +/-1% resistor accuracy is acceptable. If there is any resistance exceeding the requested range, address 127 will be returned.

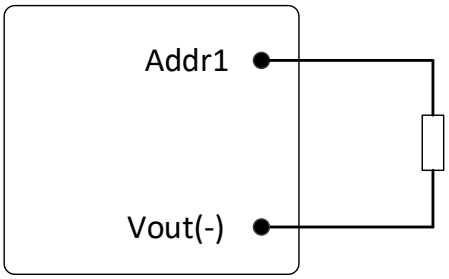


Figure 41.

Power Management Bus Address	Resistor (Kohm)
96	10
97	15
98	21
99	28
100	35.7
101	45.3
102	56.2
103	69.8
104	88.7
105	107
106	130
107	158
108	191
109	232

NOTE:

1. If boot load function is needed, there cannot be an I2C slave address of 0x58 on I2C bus.

POWER MANAGEMENT BUS APPLICATION CIRCUIT

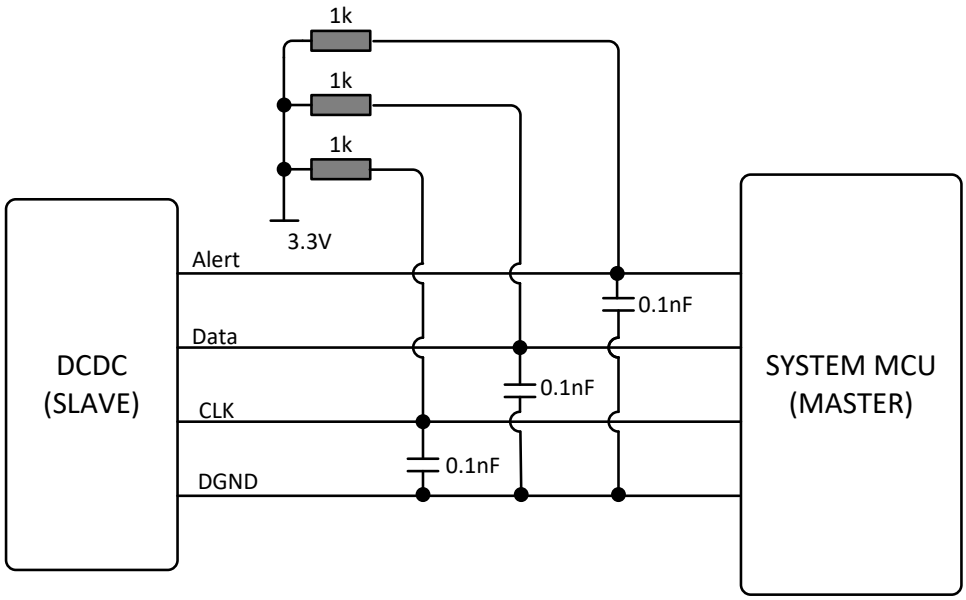


Figure 42. Power Management Bus Application Circuit

NOTE:

1. Projects without DGND use Vout(-).

PARAMETER	NOTES	MIN	NOM	MAX	UNITS
Logic Input Low (VIL)	1	0	-	0.8	V
Logic Input High (VIH)	1	2.1	-	3.3	V
Logic Output Low (VOL)	2	-	-	0.65	V
Logic Output High (VOH)	3	2.3	-	-	V
Power Management Bus Operating Frequency Range		-	100/400	-	kHz
Output Current Reading Accuracy	4	-5	-	+5	%
	5	-3.75	-	+3.75	A
Output Voltage Reading Accuracy		-2	-	+2	%
Input Voltage Reading Accuracy		-4	-	+4	%
Temperature Reading Accuracy		-5	-	+5	°C

Notes	
1	Data, CLK pin
2	Data, Alert, CLK pin; IOL = 4 mA
3	Data, Alert, CLK pin; IOH = -4 mA
4	Vin = 54 V, Io = 50% ~ 100% of Iomax
5	Vin = 54 V, Io = 5% ~ 50% of Iomax

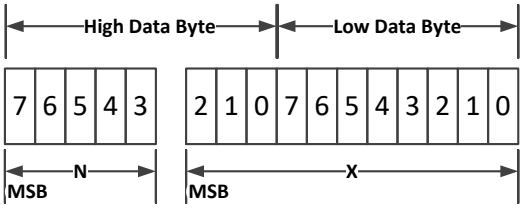
BLACK BOX

Black Box function is supported which has 10K erase cycles. Vin UVLO and Vin OVP event may not accurately record in black box. Black box only stores at the first fault event until next Vin power cycle or remote on/off cycle. 20 history information are stored in flash memory and each history information has 32 record content which is shown as below. EVENT# is the history event offset value. Every 20 history event store operation erase the flash once.

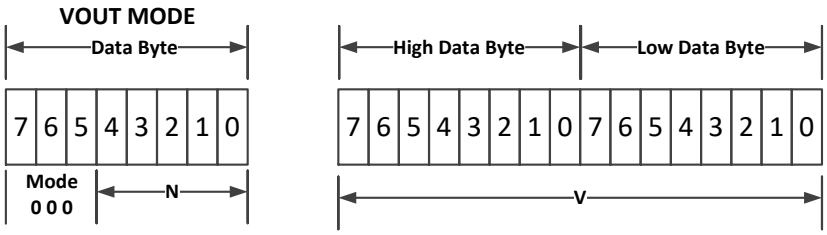
ADDRESS OFFSET	CONTENT
0	EVENT#
1	STATUS_WORD_HIGH_BYTE
2	STATUS_WORD_LOW_BYTE
3	STATUS_VOUT
4	STATUS_IOUT
5	STATUS_INPUT
6	STATUS_TEMPERATURE
7	STATUS_CML
8	VIN_DATA_HIGH_BYTE
9	VIN_DATA_LOW_BYTE
10	VOUT_DATA_HIGH_BYTE
11	VOUT_DATA_LOW_BYTE
12	IOUT_DATA_HIGH_BYTE
13	IOUT_DATA_LOW_BYTE
14	TEMPERATURE_DATA_HIGH_BYTE
15	TEMPERATURE_DATA_LOW_BYTE
16	FAULT_TIME_FIRST_BYTE
17	FAULT_TIME_SECOND_BYTE
18	FAULT_TIME_THIRD_BYTE
19	FAULT_TIME_FOURTH_BYTE
20~31	N/A

POWER MANAGEMENT BUS DATA FORMAT

For commands which is except to the output voltage, including input voltage, output current, temperature, PWM frequency, duty cycle, the controller will use the 2-byte linear format as defined by the Power Management Bus system management protocol. The linear data format contains 2 bytes which include a 5-bit two's complement exponent and an 11-bit two's complement mantissa as below. The transmitted value Y is reported as the form $Y = X*2^N$.



For example, to set the over temperature fault threshold 130 deg C by OT_FAULT_LIMIT command, the read/write data can be calculated refer to below: the binary number of N is 0, whose decimal number is 0.
$X = T_{OTP}/2^{(0)} = 130$, whose binary is 0b00010000010.
Combine X and N, the binary is 0b0000000010000010. The hexadecimal of OT_FAULT_LIMIT is 0x0082.
The output voltage parameters use the Power Management Bus Vout linear format. The data format is shown below.



The voltage will be in the form $Voltage = V*2^N$. The Mantissa and exponent in this equation will be read and reported using 3 bytes. The first byte is the VOUT_MODE byte which will always contain 000 in the 3 MSB's. The 5 LSB's are the exponent. The exponent N is fixed and equals -10. The other 2 bytes N will contain the Mantissa. In the above format N is a 5-bit two's complement binary integer and V is a 16-bit unsigned binary integer. All 16 bits are reported to be compatible with the Power Management Bus protocol.
For example, to set Vout to 12V by VOUT_COMMAND, the read/write data can be calculated refer to below process:
$V = Vout/2^{(-10)} = 12/2^{(-10)} \approx 12288$
Convert the decimal to hexadecimal format is 0x3000. So the VOUT_COMMAND is 0x3000.

SUPPORTED POWER MANAGEMENT BUS COMMANDS

The main Power Management Bus commands described in the Power Management Bus 1.2 specification are supported by the module. Partial Power Management Bus commands are fully supported; Partial Power Management Bus commands have difference with the definition in Power Management Bus 1.2 specification. All the supported Power Management Bus commands are detailed summarized in the below table.

COMMAND	CODE	COMMAND DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DATA UNITS	NOTE
OPERATION	0x01	Configures the operational state of the module	R/W byte	Bit field	0x80	/	1
ON_OFF_CONFIG	0x02	Configures the combination of CONTROL pin input and serial bus commands needed to turn the module on and off	Read byte	Bit field	0x1C	/	1,2
CLEAR_FAULTS	0x03	Clear any fault bits that have been set	Send byte	/	/	/	/
WRITE_PROTECTION	0x10	Set or Clear the bit of Write protection	R/W byte	Bit field	0x80	/	1
RESTORE_DEFAULT_ALL	0x12	Restore the factory settings to the non-volatile memory	Write	/	/	/	5
STORE_USER_ALL	0x15	Store the current settings to the non-volatile memory	Write	/	/	/	5
VOUT_MODE	0x20	Vo data format	Read byte	mode + exponent	0x16	/	/
VOUT_COMMAND	0x21	Set the output voltage normal value	R/W word	Vout linear	12.0	Volts	/
VOUT_MAX	0x24	Set an upper limit on the output voltage the module can command	Read word	Vout linear	12.6	Volts	/
VOUT_MARGIN_HIGH	0x25	Set the output voltage margin high value	Read word	Vout linear	12.5	Volts	/
VOUT_MARGIN_LOW	0x26	Set the output voltage margin low value	Read word	Vout linear	10	Volts	/
VOUT_MIN	0x2B	Set a lower limit on the output voltage the module can command	Read word	Vout linear	8	Volts	/
MAX_DUTY	0x32	Set the maximum duty cycle	Read word	Linear	50	%	/
FREQUNCY_SWITCH	0x33	Set the primary side switching frequency	Read word	Linear	150	kHz	/
VOUT_OV_FAULT_LIMIT	0x40	Set the output over voltage fault threshold	R/W word	Vout linear	13.5	Volts	4
VOUT_OV_FAULT_RESPONSE	0x41	Instructs what action to take in response to an output overvoltage fault	Read byte	Bit field	0x80	/	1
IOUT_OC_FAULT_LIMIT	0x46	Set the output overcurrent fault threshold	R/W word	Linear	180	A	3,4
IOUT_OC_FAULT_RESPONSE	0x47	Instructs what action to take in response to an output overcurrent fault	Read byte	Bit field	0xF8	/	1
OT_FAULT_LIMIT	0x4F	Set the over temperature fault threshold	R/W word	Linear	130	Deg C	3,4
OT_FAULT_RESPONSE	0x50	Instructs what action to take in response to an over temperature fault	Read byte	Bit field	0xB8	/	1
MFR_C1_C2_CONFIG	0x6C	Configure C2 pin function	R/W byte	Bit field	0x00	/	1
MFR_C2_CONFIG	0x6D	Configure C2 pin logic	R/W byte	Bit field	0x00	/	1
MFR_PGOOD_POLARITY	0x6E	Configure power good logic	R/W byte	Bit field	0x00	/	1
STATUS_WORD	0x79	Returns the information with a summary of the unit's fault condition	Read word	Bit field	0	/	1,6
STATUS_VOUT	0x7A	Returns the information with a summary of the unit's output voltage condition	Read byte	Bit field	0	/	1,6
STATUS_IOUT	0x7B	Returns the information with a summary of the unit's output current condition	Read byte	Bit field	0	/	1,6
STATUS_TEMPERATURE	0x7D	Returns the information with a summary of the unit's temperature condition	Read byte	Bit field	0	/	1,6
STATUS_CML	0x7E	Returns the information with a summary of the unit's communication condition	Read byte	Bit field	0	/	1,6
READ_VIN	0x88	Returns the input voltage of the module	Read word	Linear	/	Volts	/
READ_VOUT	0x8B	Returns the output voltage of the module	Read word	Vout Linear	/	Volts	/

COMMAND	CODE	COMMAND DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DATA UNITS	NOTE
READ_IOUT	0x8C	Returns the output current of the module	Read word	Linear	/	A	/
READ_TEMPERATURE_1	0x8D	Returns the temperature of the module	Read word	Linear	/	Deg C	/
POWER MANAGEMENT BUS_REVISION	0x98	Reads the revision of the Power Management Bus	Read byte	Bit field	0x22	/	1
MFR_ID	0x99	Reads the ID of the manufacture	Read block	ASCII	BELF	/	/
FIRMWARE_REV	0x9B	Reads the revision of the firmware	Read block	ASCII	A1	/	7
BLACKBOX_EN	0xDF	Enable or disable the black box overwrite function	Read byte	Bit field	0x01	/	1
READ_HISTORY EVENTS	0xE0	Read history event from black box	Read block	Bit field	/	/	1
SET_HISTORY_EVENT_OFFSET	0xE1	Set history event offset	R/W byte	Bit field	/	/	1

NOTES:

1. Refer to below detailed command description.
2. OPERATION command controls module on/off.
3. Before write operation, it is necessary to read the register data and parse out the corresponding linear format N value, then convert write value based on N.
4. In order to ensure that the product works properly, the adjustment range of the protection limit value is limited, when the set value exceeds the upper or lower limits, the lower limit value is automatically set. The following table shows the upper and lower limits.

COMMAND	CODE	THE LOW LIMIT	THE UPPER LIMIT
VOUT_OV_FAULT_LIMIT	0x40	10	14
IOUT_OC_FAULT_LIMIT	0x46	20	200
OT_FAULT_LIMIT	0x4F	120	140

5. Read or write this command, PSU will shut down until next vin power cycle.
6. ALL the fault bits set in all the status registers remain set, even if the fault condition is removed or corrected, until one of the following occur:

   1) A remote on/off cycle;

   2) The device receives a CLEAR_FAULTS command;

   3) Vin power is removed from the module.
7. Block read command, byte count=2. The default value will be changed with the revision of the firmware.

OPERATION (0x01)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7	Turn the module on/off	1	On	1
		0	Off	
6	Reserved	/	/	0
5:4	Control the source of the output voltage command	00	VOUT_COMMAND	00
		01	VOUT_MARGIN_LOW	
		10	VOUT_MARGIN_HIGH	
		11	/	
3:0	Reserved	/	/	0000

ON_OFF_CONFIG (0x02)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:5	Reserved	/	/	000
4	Module powers up regardless of the state of the CONTROL pin and OPERATION command or not	0	/	1
		1	Wait CONTROL and OPERATION	
3	Module powers up regardless of the state of the OPERATION command or not	0	/	1
		1	Wait OPERATION command	
2	Module powers up regardless of the state of the CONTROL pin or not (Not supported)	0	/	1
		1	Wait CONTROL pin	
1:0	Reserved	/	/	00

WRITE_PROTECTION (0x10)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7	Enable / Disable the protection	1	Protection is enabled	1
		0	Protection is disabled	
6:0	Reserved	/	/	0000000

VOUT_OV_FAULT_RESPONSE (0x41)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:6	Response when fault happens	00-01	/	10
		10	The module shuts down and response according to the retry setting in bits [5:3]	
		11	/	
5:3	Retry setting	000	Module does not attempt to restart until a RESET signal or OPERATION command, or Bias power is removed	000
		001-110	/	
		111	Attempts to restart continuously until it is commanded off	
2:0	Reserved	/	/	000

IOUT_OC_FAULT_RESPONSE (0x47)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:6	Response when fault happens	00-10 11	/ The module shuts down and response according to the retry setting in bits [5:3]	11
5:3	Retry setting	000 001-110 111	Module does not attempt to restart until a RESET signal or OPERATION command, or Bias power is removed / Attempts to restart continuously until it is commanded off	111
2:0	Reserved	/	/	000

OT_FAULT_RESPONSE (0x50)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:6	Response when fault happens	00-01 10 11	/ The module shuts down and response according to the retry setting in bits [5:3] /	10
5:3	Retry setting	000 001-110 111	Module does not attempt to restart until a RESET signal or OPERATION command, or Bias power is removed / Attempts to restart continuously until it is commanded off	111
2:0	Reserved	/	/	000

MFR_C1_C2_CONFIG (0x6C)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:4	Reserved	/	/	0000
3:0	Pin configuration	0000 0010	C2 pin: POWER_GOOD C2 pin: ON/OFF (Secondary)	0000

MFR_C2_CONFIG (0x6D)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:2	Reserved	/	/	000000
1	ON/OFF Configuration	1 0	And- Primary and secondary side on/off C2 pin signal is ignored	0
0	Secondary Side ON/OFF logic	1 0	Positive Logic (High level enable: input > 2.64V) Negative Logic (Low level enable: input < 0.66V)	0

MFR_PGOOG_POLARITY (0x6E)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:1	Reserved	/	/	0000000
0	Power Good Logic	1 0	Positive PGOOD logic Negative PGOOD logic	0

STATUS_WORD (0x79)				
HIGH BYTE				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7	VOUT	1	An output voltage fault has occurred	0
		0	Not occurred	
6	IOUT/POUT	1	An output current or output power fault has occurred	0
		0	Not occurred	
5	INPUT (Not supported)	1	An input overvoltage fault has occurred	0
		0	Not occurred	
4	Reserved	/	/	0
3	Power_Good	1	Power_Good signal is negated	0
		0	Power_Good signal is ok	
2:1	Reserved	/	/	00
0	UNKNOWN	1	A fault type not given in bits [15:1] of the SATUS_WORD has been detected	0
		0	Not occurred	

STATUS_WORD (0x79)				
LOW BYTE				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7	Busy	1	A fault was declared because the device was busy and unable to respond	0
		0	Not occurred	
6	Off	1	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled	0
		0	Not occurred	
5	VOUT_OV_FAULT	1	An output overvoltage fault has occurred	0
		0	Not occurred	
4	IOUT_OC_FAULT	1	An output overcurrent fault has occurred	0
		0	Not occurred	
3	VIN_UV_FAULT (Not supported)	1	An input under voltage fault has occurred	0
		0	Not occurred	
2	TEMPERATURE	1	A temperature fault has occurred	0
		0	Not occurred	
1	CML	1	A communication, memory or logic fault has occurred	0
		0	Not occurred	
0	NONE_OF_THE_ABOVE	1	A fault not listed in bits [7:1] of this byte has occurred	0
		0	Not occurred	

STATUS_VOUT (0x7A)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7	VOUT_OV_FAULT	1	Occurred	0
		0	Not occurred	
6:5	Reserved	/	/	00
4	VOUT_UV_FAULT	1	Occurred	0
		0	Not occurred	
3:0	Reserved	/	/	0000

STATUS_IOUT (0x7B)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7	IOUT_OC_FAULT	1	Occurred	0
		0	Not occurred	
6:0	Reserved	/	/	0000000

STATUS_TEMPERATURE (0x7D)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7	OT_FAULT	1	Occurred	0
		0	Not occurred	
6:0	Reserved	/	/	0000000

STATUS_CML (0x7E)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7	Invalid or unsupported command received	1	Occurred	0
		0	Not occurred	
6	Invalid or unsupported data received	1	Occurred	0
		0	Not occurred	
5:0	Reserved	/	/	000000

POWER MANAGEMENT BUS_REVISION (0x98)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:4	Indicate the revision of Power Management Bus Specification Part I to which the device is compliant	0000	1.0	1.2
		0001	1.1	
		0010	1.2	
		0011	1.3	
3:0	Indicate the revision of Power Management Bus Specification Part II to which the device is compliant	0000	1.0	1.2
		0001	1.1	
		0010	1.2	
		0011	1.3	

BLACKBOX_EN (0xDF)				
Bit number	**Purpose**	**Bit value**	**Meaning**	**Default settings**
7:1	Reserved	/	/	0000000
0	Enable/Disable the black box overwrite function	1 0	Overwrite function is enabled Overwrite function is disabled	1

Note: if overwrite function is disabled, black box only records 20 times faults, then it will lock and no more faults will be recorded. If overwrite function is enabled. When fault log is full, the new fault will overwrite all the previous fault, and recount from history event offset value 1.

HISTORY EVENT READ

0xE1 command: Write the offset value to slave to decide which history event for read.

0XE0 command: Read the history data after 0xE1 command.

READ HISTORY EVENT OFFSET (0xE1)

Send read command 0xE1 and read one byte, it will return the next history event log offset value x.

START	DEVICE ADDRESS & W	COMMAND (0xE1)	REPEATED START	DEVICE ADDRESS & R

EVENT LOG OFFSET VALUE	PEC	STOP

SET HISTORY EVENT OFFSET (0xE1)

Then send write command 0xE1 and write the offset value X-1 to read back the last history event. The maximum value of the offset is 20, if the history data is large than 20, it will recount from 1.

READ_HISTORY EVENTS [0xE0]

START	DEVICE ADDRESS & W	COMMAND (0XE0)	REPEATED START	DEVICE ADDRESS & R	Byte Count=20	EVENT#

STATUS_WORD_HIGH_BYTE	STATUS_WORD_LOW_BYTE	STATUS_VOUT	STATUS_IOUT	STATUS_INPUT

STATUS_TEMPERATURE	STATUS_CML	VIN_DATA_HIGH_BYTE	VIN_DATA_LOW_BYTE	VOUT_DATA_HIGH_BYTE

VOUT_DATA_LOW_BYTE	IOUT_DATA_HIGH_BYTE	IOUT_DATA_LOW_BYTE	TEMPERATURE_DATA_HIGH_BYTE

TEMPERATURE_DATA_LOW_BYTE	FAULT_TIME_FIRST_BYTE	FAULT_TIME_SECOND_BYTE

FAULT_TIME_THIRD_BYTE	FAULT_TIME_FOURTH_BYTE	PEC	STOP

17. SOLDERING INFORMATION

The modules are designed to be compatible with a reflow soldering process. The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended reflow profile using Sn/Ag/Cu solder is shown in the following. Recommended reflow peak temperature is 245°C while the part can withstand peak temperature of 260°C maximum for 10 seconds. This profile should be used only as a guideline. Many other factors influence the success of SMT reflow soldering. Since your production environment may differ, please thoroughly review these guidelines with your process engineers.

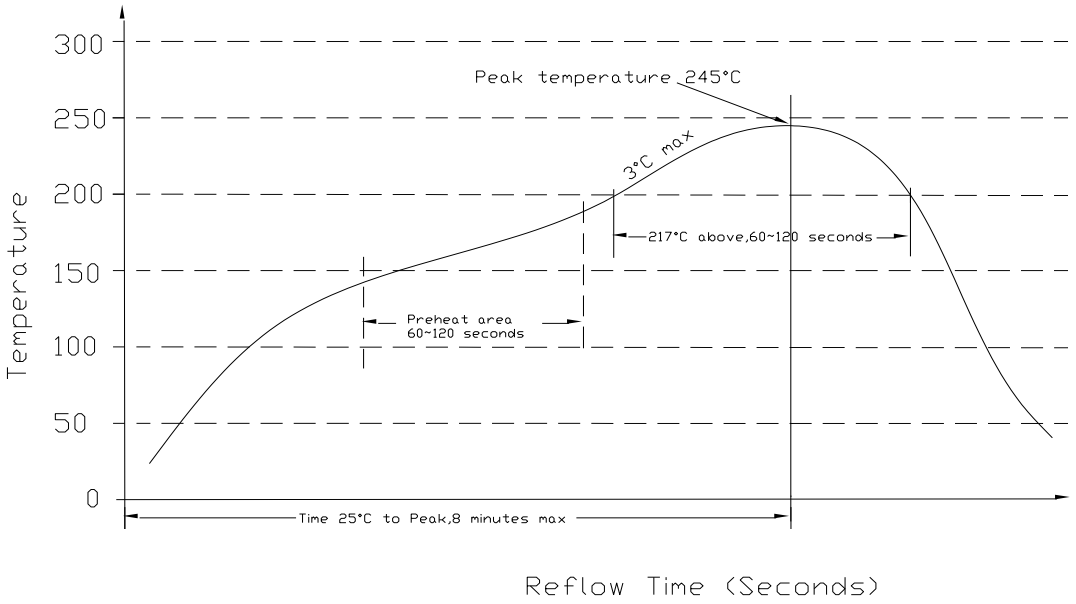


Figure 43. Soldering Temperature

18. MSL RATING

The modules have a MSL rating of 3.

19. STORAGE AND HANDLING

The modules are designed to be compatible with J-STD-033 Rev: A (Handling, Packing, Shipping and Use of Moisture /Reflow Sensitive surface Mount devices). Moisture barrier bags (MBB) with desiccant are applied. The recommended storage environment and handling procedure is detailed in J-STD-033.

20. PRE-BAKING

This component has been designed, handled, and packaged ready for pb-free reflow soldering. If the assembly shop follows J-STD-033 guidelines, no pre-bake of this component is required before being reflowed to a PCB. However, if the J-STD-033 guidelines are not followed by the assembler, Bel recommends that the modules should be pre-baked @ 120~150°C for a minimum of 4 hours (preferably 24 hours) before reflow soldering.

21. MECHANICAL DIMENSIONS

OUTLINE

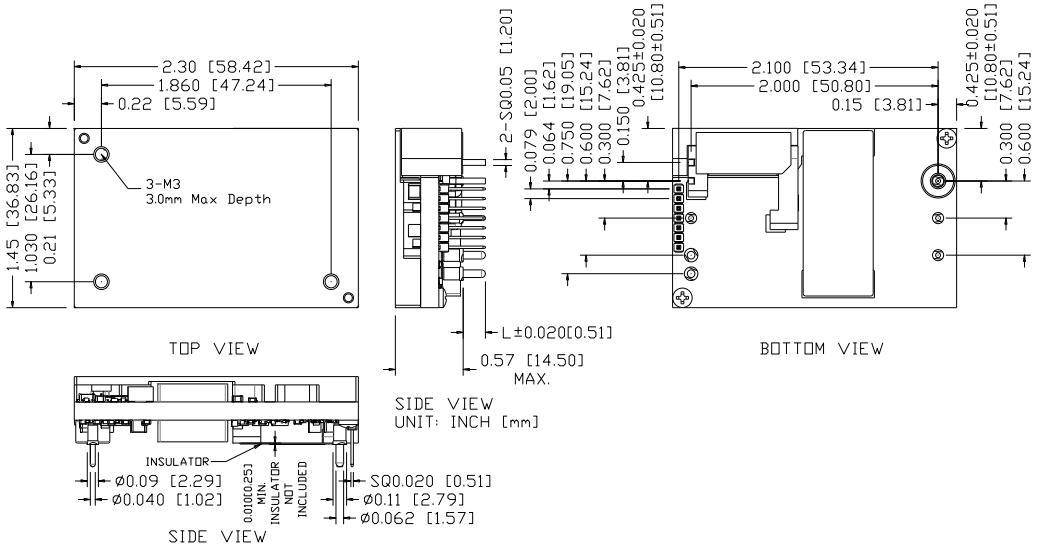


Figure 44. Mechanical Drawing

NOTES:

1） All Pins: Material - Copper Alloy;
Finish – Tin plated
2） Un-dimensioned components are shown for visual reference only.
3） Pin length according to part number explanation.
4） All dimensions in inch [mm]; Tolerances: x.xx +/-0.02 inch [0.51 mm] x.xxx +/-0.010 inch [0.25 mm].
5） The value of L refers to PART NUMBER EXPLANATION in section 1 or next page.

RECOMMENDED PAD LAYOUT

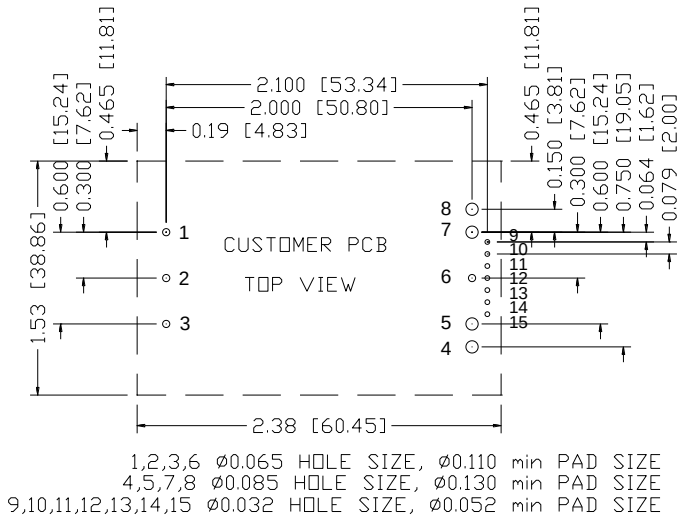


Figure 45. Recommended Pad Layout-1

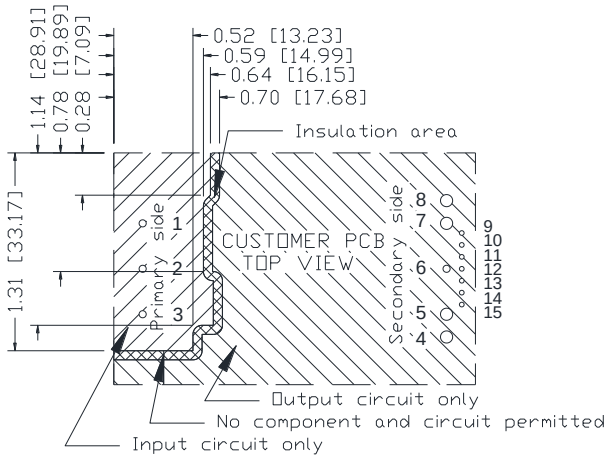


Figure 46. Recommended Pad Layout-2

PIN DEFINITIONS AND DIFFERENCES BETWEEN PINS

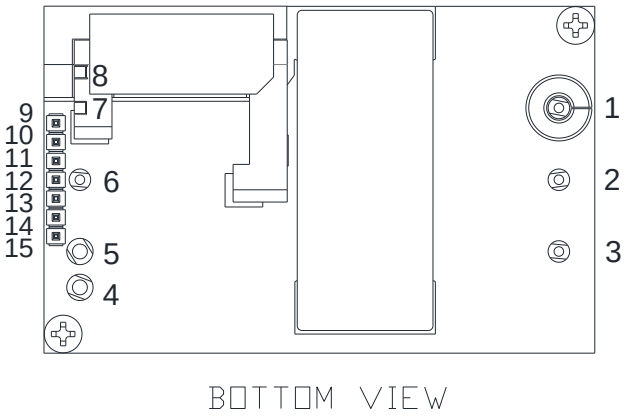


Figure 47. Pins

			TQPX8M12B-LNAT	TQPX8M12B-LNBT	TQPX8M12B-LNCT	TQPX8M12B-LNDT
PIN	**FUNCTION**	**PIN SIZE**				
1	Vin (+)	0.040”	✔	✔	✔	✔
2	ON/OFF	0.040”	✔	✔	✔	✔
3	Vin (-)	0.040”	✔	✔	✔	✔
4	Vout(-)	0.062”	✔	✔	✔	✔
5	Vout(-)	0.062”	✔	✔	✔	✔
6	PG	0.040”	✔	✔	✔	✘
7	Vout(+)	SQ0.05"	✔	✔	✔	✔
8	Vout(+)	SQ0.05"	✔	✔	✔	✔
9	Addr0	SQ0.02”	✔	✔	✔	✘
10	Addr1	SQ0.02”	✔	✔	✔	✔
11	CLK	SQ0.02”	✔	✔	✔	✔
12	Alert	SQ0.02”	✔	✔	✔	✔
13	Data	SQ0.02”	✔	✔	✔	✔
14	DGND	SQ0.02”	✔	✔	✔	✘
15	C2	SQ0.02”	✔	✔	✔	✘
	PIN LENGTH (L)					
	0.11”				✔	
	0.145”			✔		
	0.18”		✔			✔

Note: Symbol ✘ indicates that the PIN is not used in this part number.

22. FEATURE DISCRIPTIONS

OUTPUT OVER CURRENT PROTECTION

The module is equipped with internal output current limiting circuitry, and can endure limiting current continuously. If the output current exceeds the limited value, the module will shutdown and enter either hiccup mode or latch mode, which is stated in the output spec table previously.

For hiccup mode, the module will try to restart after shutdown. If the over current situation still exists, the module will shut down continuously until this fault condition is cleared. The hiccup interval time is 250ms.

For latch mode, the module will latch off once shutdown. The latch mode can be reset by cycling the input power or resetting the remote on/off pin.

OVER TEMPERATURE PROTECTION

The module is equipped with internal over temperature protection circuitry to safeguard against thermal damage. If the maximum device reference temperature exceeds the limited value, the module will shutdown and enter either auto-recovery mode or latch mode, which is stated in the general spec table previously.

For auto-recovery mode, the module will keep monitoring the reference temperature after shutdown and auto restart once the temperature is lower than the protection threshold by ~20C hysteresis.

For latch mode, the module will latch off once shutdown. The latch mode can be reset by cycling the input power or resetting the remote on/off pin.

UNDER/OVER INPUT VOLTAGE PROTECTION

The module is equipped with internal input UVLO and OVLO protection. If the input voltage is below the UV threshold or above the OV threshold, the module will shutdown and auto-restart once the input voltage is within the limited range which is stated in the input spec table previously.

23. REVISION HISTORY

DATE	REVISION	CHANGES DETAIL	APPROVAL
2024-03-25	AA	Add safety certificate. Delete watermark. Update output current reading accuracy from ±3A to ±3.75A.	S.Wang