TET3600-48-104xA

3600 W AC-DC Front-End Power Supply

Bel Power Solutions **TET3600-48-104xA** series is a 3600 Watt AC-DC power-factor-corrected (PFC) and DC-DC power supply that converts standard AC mains power or high voltage DC bus voltages into a main output of 54.5 VDC (42 – 58 VDC) for supplying 48 VDC power distribution in high performance and reliability data center equipment, servers, routers, and network switches.

The TET3600-48-104xA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



RoHS Compliant

Key Features & Benefits

- Best-in-class efficiency of up to 97% at half load
- Wide input voltage range: full power at 200 - 277 VAC or 240 - 380 VDC, reduced output power at 90-180 VAC
- AC input with power factor correction, usable also with high voltage DC
- 3600 W main output with programmable voltage set-point of 42-58 VDC
- Standby output 12 VDC / 30 W
- One single rear side connector for input and output power and signaling
- Parallel operation with active digital current sharing through CAN bus
- Hot-plug capable
- High density design: 56 W/in^3
- Small form factor (W x H x L): 104 x 40 x 256 mm (4.09 x 1.57 x 10.08 in)
- Full digital controls for improved performance
- Support both I2C (Power Management Bus protocol) and CAN communication interfaces for control, programming and monitoring
- Over temperature, output overvoltage and overcurrent protection
- Status LED with fault signaling
- Black Box recorder optional
- Isolated signals and communication interfaces
- Safety to UL/CSA 62368-1 and IEC 62368-1
- RoHS Compliant

Applications

- High Performance Servers
- Routers and Switches
- Data Center
- Industrial Power Supplies

Please read our datasheet & drawing disclaimer here.

1. ORDERING INFORMATION

TET	3600	-	48	-	104	x	A	Option Code
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**	
TET Front-Ends	3600 W		48 V		104 mm	N: Normal R: Reverse[1)]	A: AC	Blank: Standard model

[1)] Front to Rear

2. OVERVIEW

The TET3600-48-104xA is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonant-soft-switching technology and highly integrated conversion stages to reduce component stresses, providing increased system reliability, very high efficiency and high-power density. With a wide input operating voltage range and minimal linear derating of output power with respect to ambient temperature, the TET3600-48-104xA maximizes power availability in demanding server, switch, and router applications. The power supply is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range when using AC input voltage. When operated with high voltage DC the PFC circuit is still in operation, but input current is controlled to be DC.

The DC-DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The optional always-on +12V standby output provides power to external power distribution and management controllers. Its protection with an active OR-ing device provides for maximum reliability.

Status information is provided with front-panel LED. In addition, the power supply can be monitored and controlled (i.e. fan speed setpoint) via the I2C bus or CAN bus. Both buses allow full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Both buses all support the bootloader to allow field update of the firmware in the DSP controllers.

Cooling is managed by a fan, controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus or CAN bus.

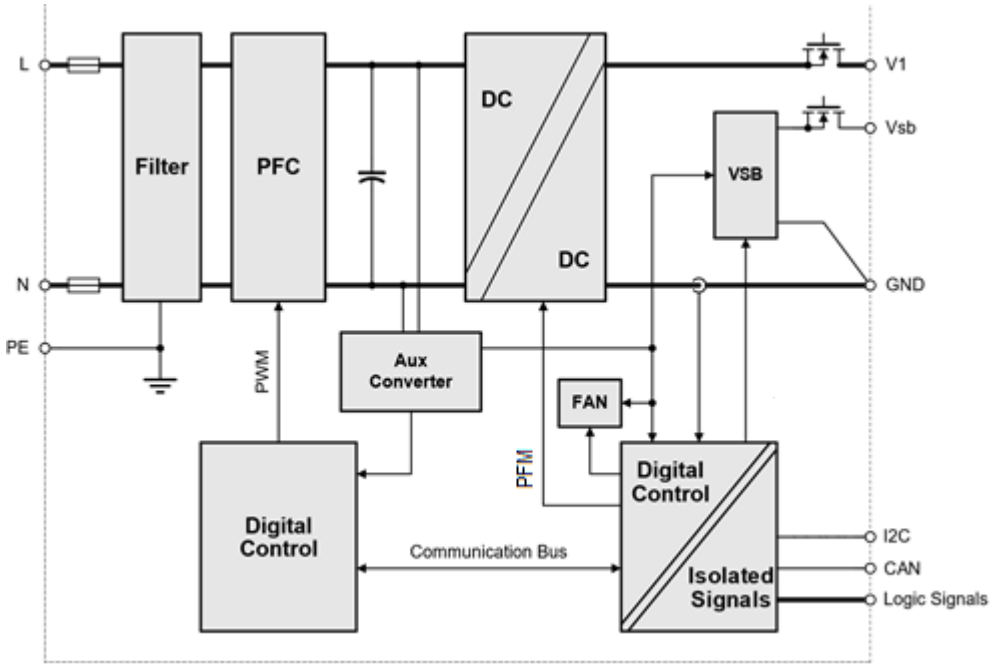


Figure 1. TET3600-48-104xA Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the power supply.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
$V_{i\ maxc}$	Maximum Input	Continuous		305 400	VAC VDC

4. INPUT

General Condition: T_A = 0…50 °C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ AC\ nom}$	Rated AC Input Voltage	Rated AC Input Voltage	100	230	277	VAC
$V_{i\ AC\ operating}$	AC Input Voltage Range	Operating AC Input Voltage ($V_{i\ AC\ min}$ to $V_{i\ AC\ max}$)	90		305	VAC
$V_{i\ AC\ HL}$	High line AC Input Voltage	AC Input Voltage Range with full output power	180		305	VAC
$V_{i\ AC\ Red}$	Derated AC Input Voltage	AC Input Voltage Range with reduced output power	90		180	VAC
$V_{i\ DC\ nom}$	Rated DC Input Voltage	Rated DC Input Voltage	240		380	VDC
$V_{i\ DC\ operating}$	DC Input Voltage range	Operating DC Input Voltage ($V_{i\ DC\ min}$ to $V_{i\ DC\ max}$)	192		400	VDC
$I_{i\ max}$	Max Input Current	$V_{i\ AC}$ > 200 VAC or $V_{i\ DC}$ > 200 VDC			21	A_{rms}
$I_{i\ p}$	Inrush Current Limitation	$V_{i\ AC\ min}$ to $V_{i\ AC\ max}$ or $V_{i\ DC\ min}$ to $V_{i\ DC\ max}$			50	A_p
F_i	Input Frequency		47	50/60	63	Hz
PF	Power Factor	$V_{i\ AC\ nom}$, 50Hz, I_1 > 0.2 $I_{1\ nom}$	0.96			W/VA
THD	Total Harmonic Distortion on Input Current	$V_{i\ AC\ HL}$, > 50 % $P_{1\ nom}$		3	5	%
$V_{i\ AC\ on}$	Turn-on AC Input Voltage[2]	Ramping up	86	88	90	VAC
$V_{i\ AC\ off}$	Turn-off AC Input Voltage	Ramping down	80	83	86	VAC
$V_{i\ DC\ on}$	Turn-on DC Input Voltage	Ramping up	183	186	188	VDC
$V_{i\ DC\ off}$	Turn-off DC Input Voltage	Ramping down	176	181	185	VDC
η	Efficiency[3]	V_i = 230 VAC, 0.1·$I_{x\ nom}$, $V_{x\ nom}$, T_A = 25°C		92		%
		V_i = 230 VAC, 0.2·$I_{x\ nom}$, $V_{x\ nom}$, T_A = 25°C		95.2		
		V_i = 230 VAC, 0.5·$I_{x\ nom}$, $V_{x\ nom}$, T_A = 25°C		96.6		
		V_i = 230 VAC, $I_{x\ nom}$, $V_{x\ nom}$, T_A = 25°C		95.8		
T_{hold}	Hold-up Time	After last AC zero crossing, V_1 > 41 V, $V_{i\ AC\ nom}$, $P_{1\ nom}$	10			ms
$T_{hold\text{-}up,\ vsb\text{-}to\text{-}vo1}$	Time from Vo1 to Vsb Leaving Regulation	All hold-up conditions	40			ms

[2] The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges
[3] Efficiency measured without fan loss included in PSU losses

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4.1. INPUT FUSE

Fast-acting 30 A input fuses in series with both the L- and N-line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2. INRUSH CURRENT

The power supply exhibits an X capacitance of 4.66 µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitors will be charged through NTC resistors which will limit the inrush current.

NOTE:

Do not repeat plug-in / out operations below 30 sec interval time, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current may result.

4.3. INPUT UNDER-VOLTAGE

If the input voltage is reduced below the input under-voltage lockout threshold $V_{i\ AC\ off}$ or $V_{i\ DC\ off}$, the supply will be inhibited. Once the input voltage rises above $V_{i\ AC\ on}$ or $V_{i\ DC\ on}$, the supply will return to normal operation again.

4.4. POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load range. The input current will follow the shape of the input voltage. If, for instance, the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform.

4.5. EFFICIENCY

The high efficiency is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The rpm of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions. *Figure 2* shows the measured efficiency with AC input voltage applied, while *Figure 3* represents the efficiency when operating with high voltage DC input.

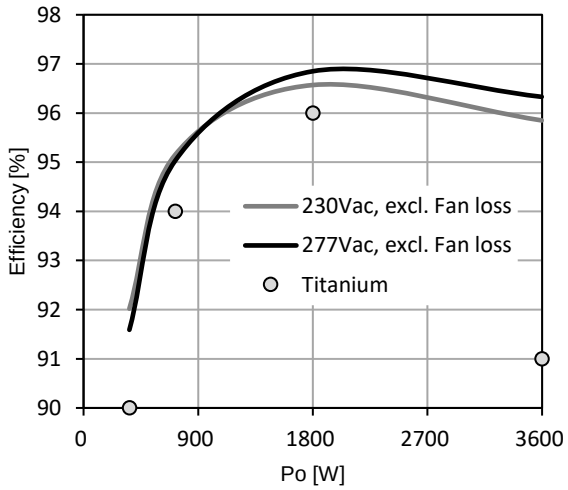


Figure 2. Typical Efficiency vs. Load Current at AC Input

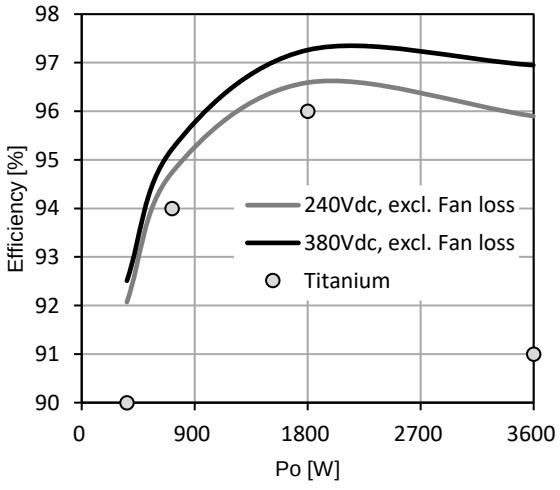


Figure 3. Typical Efficiency vs. Load Current at HVDC Input

5. OUTPUT

General Condition: T_A = 0…50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 ·$I_{1\ nom}$, T_a ≤ 50°C		54.5		VDC
$V_{1\ prg}$	Programmable Output Voltage Range	0.5 ·$I_{1\ nom}$, T_a ≤ 50°C	42		58	VDC
$V_{1\ set}$	Output Setpoint Accuracy	0.5 ·$I_{1\ nom}$, T_a ≤ 50°C	-0.5		+0.5	% $V_{1\ nom}$
$dV_{1\ tot}$	Total Regulation	$V_{i\ AC\ min}$ to $V_{i\ AC\ max}$ or $V_{i\ DC\ min}$ to $V_{i\ DC\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-3		+3	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	$V_{i\ AC\ HL}$ or $V_{i\ DC\ operating}$, T_a ≤ 50°C, V_1 ≥ 48.0 V		3600		W
		$V_{i\ AC\ HL}$ or $V_{i\ DC\ operating}$, T_a = 60°C, V_1 ≥ 48.0 V		2900		W
$I_{1\ nom}$	Nominal Output Current	$V_{i\ AC\ HL}$ or $V_{i\ DC\ operating}$, T_a ≤ 50°C, V_1 = 54.5 V		66		ADC
		$V_{i\ AC\ HL}$ or $V_{i\ DC\ operating}$, T_a = 60 °C, V_1 = 54.5 V		53.2		ADC
		$V_{i\ AC\ HL}$ or $V_{i\ DC\ operating}$, T_a ≤ 50°C, V_1 = 48.0 V		75		ADC
		$V_{i\ AC\ HL}$ or $V_{i\ DC\ operating}$, T_a ≤ 50°C, V_1 = 58.0 V		62		ADC
$P_{1\ red}$	Available Output Power at V_i < 180 VAC	$V_{i\ AC\ Red}$, T_a ≤ 50°C, V_1 ≥ 48.0 V		21Arms*Vin – 400W[4]		W
$P_{1\ red}$	Low Line Output Power	V_i = 120 VAC, T_a ≤ 50°C, V_1 ≥ 48.0 V		2120		W
$I_{1\ ol}$	Short Time Over Load Current, Maximum duration 10 ms	$V_{i\ AC\ Red}$, $V_{i\ AC\ HL}$, $V_{i\ DC\ operating}$, relative to static output current available			110	%
$v_{1\ pp}$	Output Ripple Voltage	20 MHz BW with min Capacitive load			1000	mVpp
$dV_{1\ Load}$	Load Regulation	V_i = $V_{i\ AC\ nom}$ or $V_{i\ DC\ nom}$, 0 - 100 % $I_{1\ nom}$		-12		mV/A
$dV_{1\ Line}$	Line Regulation	$V_{i\ AC\ min}$ to $V_{i\ AC\ max}$ or $V_{i\ DC\ min}$ to $V_{i\ DC\ max}$		0		mV
dI_{share}	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 25% $I_{1\ nom}$	-3		+3	ADC
dV_{dyn}	Dynamic Load Regulation	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1A/µs, f = 2 ... 50 Hz.	-2		2	V
T_{rec}	Recovery Time	Within 1% of V_1 final steady state I_1 = 10 … 100% $I_{1\ nom}$			2	ms
$t_{AC\ V1}$	Start-up Time from AC	Time from V_i in range to V_1 in regulation, T_A > 10 °C			4[5]	sec
$t_{V1\ rise}$	Rise Time	V_1 = 10 … 90% $V_{1\ nom}$		20		ms
C_{V1}	Maximum Capacitive Load		1		15	mF

[4] Example: At nominal grid 120 VAC the max. output power is 2120 W, will be provided also with grid fluctuation -10 % down to 108 VAC.
[5] At low ambient temperature T_A < 10 °C this time can rise to max 10 s

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5.1. STANDBY OUTPUT

A standby output is available, delivering 12 V with up to 2.5 A, to provide power to system management controls.

The output is always enabled if the input voltage is within operating range, and provides over current, over voltage and over temperature protections. Current share on standby output is provided by passive droop sharing.

General Condition: T_A = 0…50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Standby output VSB						
$V_{SB\ nom}$	Nominal Output Voltage	I_{SB} = 1.25 A, T_A = 25 °C		12		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-1		+1	% $V_{SB\ nom}$
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100 % $I_{SB\ nom}$, $T_{A\ min}$ to $T_{A\ max}$	-5		+3	% $V_{SB\ nom}$
$P_{SB\ nom}$	Nominal Output Power			30		W
$I_{SB\ nom}$	Nominal Output Current			2.5		ADC
$V_{SB\ pp}$	Output Ripple Voltage	20 MHz BW			150	mVpp
$dV_{SB\ Load}$	Load Regulation	0 - 100 % $I_{SB\ nom}$		200		mV
$dV_{SB\ Line}$	Line Regulation	V_i = $V_{i\ AC\ min}$ … $V_{i\ AC\ max}$ or $V_{i\ DC\ min}$ ... $V_{i\ DC\ max}$		0		mV
dI_{share}	Current Sharing	Deviation from $I_{SB\ tot}$ / N			2	ADC
dV_{dyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_{SB}/dt = 1A/µs, f = 2 ... 50 Hz.	-600		600	mV
T_{rec}	Recovery Time	Within 1% of V_{SB} final steady state			2	ms
$t_{AC\ VSB}$	Start-up Time from AC	Time from V_i in range to V_{SB} in regulation, T_A > 10°C			3[6]	sec
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10 … 90% $V_{SB\ nom}$		5		ms
C_{VSB}	Maximum Capacitive Load				1500	µF

5.2. OUTPUT VOLTAGE RIPPLE

The internal output capacitance at the power supply output (behind OR-ing element) is minimized to prevent disturbances during hot plug. To provide low ripple voltage at the application, external capacitors (a parallel combination of 10 µF low ESR capacitor in parallel with 0.1 µF ceramic capacitors) should be added at the input of the connected load circuits.

5.3. OVERSUBSCRIPTION

The main output has the capability to allow a load current of up to 10 A above the nominal output current rating for a maximum duration of 5 ms. This allows the system to consume extended power for short time dynamic processes. Oversubscription can be used with maximum 10% duty cycle. If the output current is less than 10 A above nominal output current, then the oversubscription time can be longer.

5.4. OUTPUT ISOLATION

Main and standby output (if available) and all signals are isolated from the chassis and protective earth connection, although the applied voltage must not exceed 100 Vpeak to prevent any damage to the power supply.

The main output return path serves as main and standby power return.

The all signals are referenced to signal ground SGND. These signals and SGND are isolated from main output and chassis allowing a maximum voltage of 50 Vpeak between signals/SGND and main return GND. Signal ground SGND may be connected to power ground GND within the application, shown as dotted lines in *Figure 4*, allowing powering of system communication and logic from VSB output.

[6] At low ambient temperature T_A < 10 °C this time can rise to max 10s

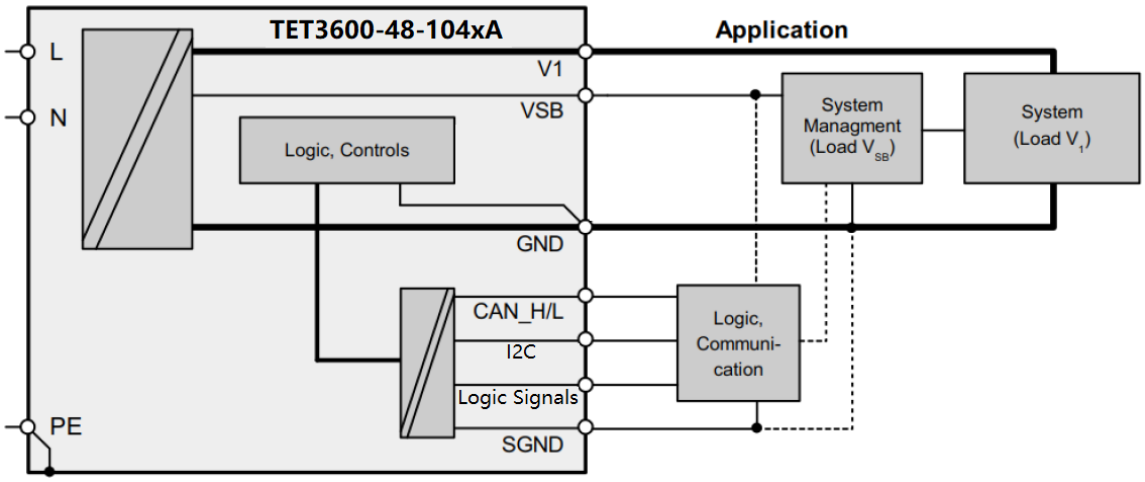


Figure 4. Output connection

6. PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuses (L+N)	Not user accessible, fast-acting (F)		30		A
$V_{1\ OV}$	OV Threshold V_1	Hardware protection	110		120	% $V_{1\ nom}$
$t_{V1\ OV}$	OV Latch Off Time V_1				1	ms
$P_{1\ lim}$	Nominal Power Limitation	$V_{i\ AC\ HL}$, $T_a \leq 50°C$, $V_1 \geq 48$ V		3600		W
		$V_{i\ AC\ HL}$, $T_a = 60°C$, $V_1 \geq 48$ V		2900		W
$I_{1\ lim}$	Nominal Current Limitation	$V_{i\ AC\ HL}$, $T_a \leq 50°C$, $V_1 = 54.5$ V	69	72	75	ADC
		$V_{i\ AC\ HL}$, $T_a = 60°C$, $V_1 = 54.5$ V	56	59	62	ADC
		$V_{i\ AC\ HL}$, $T_a \leq 50°C$, $V_1 = 42$ … 48 V	78	81	85	ADC
		$V_{i\ AC\ HL}$, $T_a \leq 50°C$, $V_1 = 58$ V	65	67	70	ADC
$I_{1\ ol\ lim}$	Current Limit during short time over load V1	$V_{i\ AC\ HL}$, $T_a \leq 50°C$, $V_1 = 54.5$ V, Maximum duration 10ms	73	76		ADC
$t_{1\ SC\ off}$	Short Circuit Latch off time	Time to latch off when in short circuit or output under voltage ($V_1 < V_{1\ UV}$)		10		ms
$V_{1\ UV}$	Output Under Voltage Protection		39	40	41	VDC
$t_{1\ UV}$	Output Under Voltage Protection Delay time	$V_1 < V_{1\ UV}$		250		ms
T_{SD}	Over Temperature on critical points	Inlet Ambient Temperature PFC Primary Heatsink Temperature DC/DC Primary Heatsink Temperature Secondary Sync Mosfet Temperature		75 105 105 120		°C
$V_{SB\ OV}$	OV Threshold V_{SB}		13		14.5	VDC
$V_{SB\ UV}$	Output Under Voltage Protection Standby		11.1	11.2	11.3	VDC
$I_{SB\ Lim}$	Standby Over Current Limit		3		3.5	ADC

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6.1. PROTECTION BEHAVIOR

Main Output: A fault on the main output will turn off only the main output. For all faults, the output is turned off and auto restart after 1sec, except:

- OVP – output will latch off.
- SCP – output will latch off.
- OTP – once the temperature cools down to recovery point, the output will restart.

Standby Output: A fault on the standby output will turn off both the standby output and main output. The outputs are turned off and auto restart after 1sec, except:

- OTP_{VSB} – once the temperature cools down to recovery point, the output will restart.

The latch off can be cleared by:

- Recycle PSON
- Recycle Input Voltage (at least 1sec off-time)
- Send 0x00 to OPERATION command and then send 0x80 to OPERATION command through I2C or CAN communication.

6.2. OVER VOLTAGE PROTECTION

For both Main and Standby outputs, the over voltage protection is implemented with a comparator. Once an OV condition is triggered, the output is turned off. Refer to Section 6.1 for protection behavior.

6.3. UNDER VOLTAGE DETECTION

For both Main and Standby outputs, the under voltage protection is implemented in firmware. Once a UV condition is triggered, the output is turned off. Refer to Section 6.1 for protection behavior.

6.4. CURRENT LIMITATION MAIN OUTPUT

Two different over current protection features are implemented on the main output.

The 1st protection is a static over current protection will shut down the output, if the output current is increased slowly and exceeds $I_{1\ lim}$ for more than 50ms, this protection will shut down the supply.

The 2nd protection is a substantially rectangular output characteristic controlled by a software feedback loop. This protects the power supply and system during the 50 ms blanking time of the static over current protection. If the output current is rising fast and reaches $I_{1\ ol\ lim}$, the supply will immediately reduce its output voltage to prevent the output current from exceeding $I_{1\ ol\ lim}$. When the output current is reduced below $I_{1\ ol\ lim}$, the output voltage will return to its nominal value. In case the output voltage drop below the under-voltage level $V_{1\ UV}$ the output will turn off after 10 ms, signaling an under-voltage fault.

The main output current limitation level $I_{1\ lim}$ and $I_{1\ ol\ lim}$ are decreased if the ambient (inlet) temperature increases beyond 50°C (see Figure 6). The current limit depends on programmed output voltage, to keep output power constant at about 3600 W. See also *Figure 5* for output characteristic and current limitation at different output voltage settings.

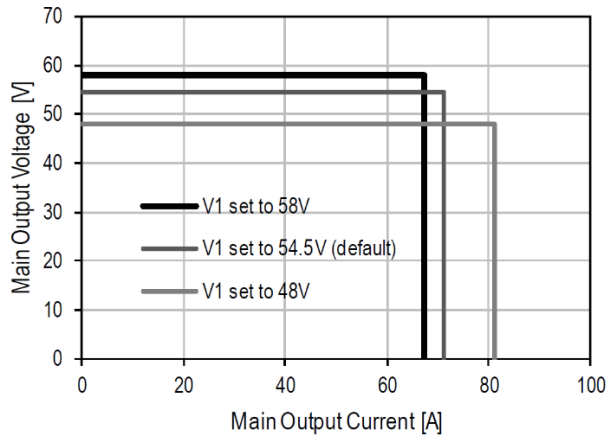


Figure 5. Output characteristics V_1

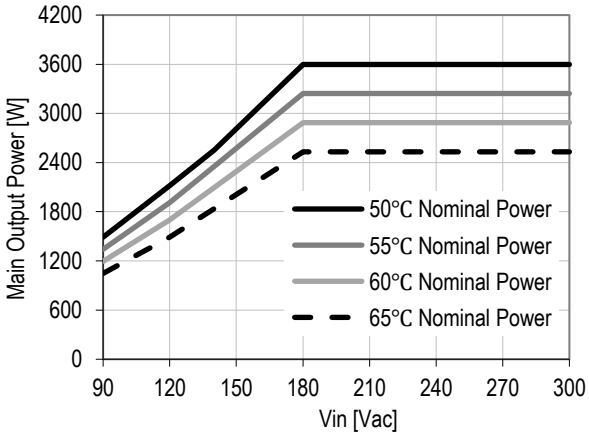


Figure 6. Derating on V1 vs Ta & Vin

6.5. CURRENT LIMITATION STANDBY OUTPUT

The standby output has a hiccup current limitation implemented. If the standby current exceeds $I_{SB\ Lim}$ the standby converter switches off and retries automatically after 1 second off time.

7. MONITORING

The power supply provides information about operating conditions through its I2C bus or CAN bus interface. Details can be found in the I2C or CAN Communication Manual BCA.G4002. Accuracy of sensors within PSU is given in following table.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input RMS Voltage	$V_{i\ min} \le V_i \le V_{i\ max}$	-3		+3	V_{rms}
$I_{i\ mon}$	Input RMS Current		-1		+1	A
$P_{i\ mon}$	True Input Power		-150		+150	W
$V_{1\ mon}$	V_1 Voltage	V_1 > 40 VDC	-1		+1	%
$I_{1\ mon}$	V_1 Current	I_1 > 25 A	-3		+3	%
		$I_1 \le$ 25 A	-1		+1	A
$V_{SB\ mon}$	V_{SB} Voltage	I_{SB} = 0 … 2.5A	-0.25		+0.25	V
$I_{SB\ mon}$	V_{SB} Current	I_{SB} = 0 … 2.5A	-0.5		+0.5	A
$P_{1\ mon}$	P_1 Output Power	P_1 > 1000W	-3		+3	%
		$P_1 \le$ 1000W	-30		+30	W
$T_{a\ mon}$	Inlet air temperature	T_a = 0 ... 50°C	-5		+5	°C

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8. SIGNALING AND CONTROL

8.1. ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
PSKILL/ PSON_L / Inputs						
V_{IL}	Input Low Level Voltage (Main output enabled)		-0.2		0.8	V
V_{IH}	Input High Level Voltage(Main output disabled)		2.4		5.25	V
$I_{IL, H}$	Maximum Input Sink or Source Current		0		1	mA
$R_{puPSKILL_H}$	Internal Pull Up Resistor on PSKILL to internal 5V			10		kΩ
R_{puPSON_L}	Internal Pull Up Resistor on PSON_L to internal 5V			10		kΩ
PWOK_L Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	-0.2		0.4	V
V_{OH}	External pull up voltage				13	V
R_{puPWOK_L}	No internal pull up resistor, Recommended external pull up resistor on PWOK_L at V_{puACOK_L} = 5V			10		kΩ
Low level output	Output voltage within regulation limits					
High level output	Output voltage out of regulation limits					
VINOK_L Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	-0.2		0.4	V
V_{OH}	External pull up voltage				13	V
$R_{puVINOK_L}$	No internal pull up resistor, Recommended external pull up resistor on VINOK_L at $V_{puVINOK_L}$ = 5 V			10		kΩ
Low level output	Input voltage within operating range					
High level output	No input voltage, or low input voltage					
SMB_ALERT_L Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	-0.2		0.4	V
V_{OH}	External pull up voltage				13	V
$R_{puSMB_ALERT_L}$	No internal pull up resistor, Recommended external pull up resistor on SMB_ALERT_L at $V_{puSMB_ALERT_L}$ = 5 V			10		kΩ

8.2. PSKILL INPUT

The PSKILL input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL input state.

8.3. PSON_L OUTPUT

The PSON_L is an input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition.

8.4. PWOK _L OUTPUT

The PWOK_L is an isolated open drain output referred to SGND. It requires an external pull-up resistor. PWOK_L is a power OK signal and will be pulled Low by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK_L will be de-asserted to a HIGH state. The start of the PWOK_L delay time shall inhibited as long as any power supply output is in current limit.

8.5. SMB_ALERT_L OUTPUT

The SMB_ALERT _L is an isolated open drain output referred to SGND. It requires an external pull-up resistor. The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits.

8.6. VINOK_L OUTPUT

The VINOK_L is an isolated open drain output referred to SGND. It requires an external pull-up resistor. A low voltage on this pin reflects input voltage to be within operating range.

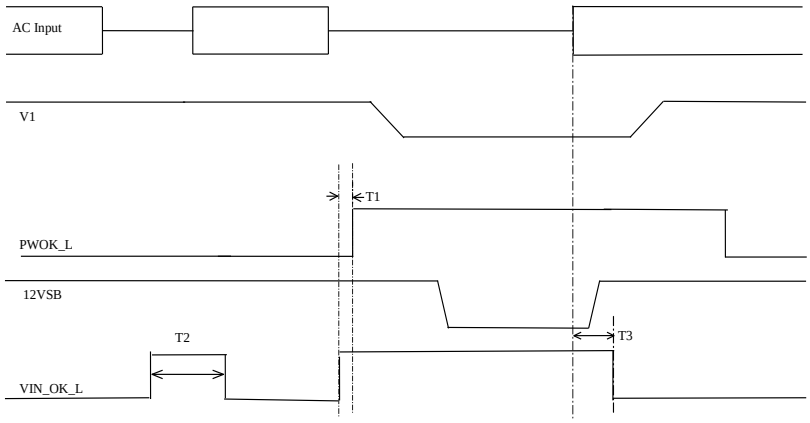


Figure 7. VIN_OK_L Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T1	VIN_OK_L & PWOK_L	3			ms
T2 *	VIN_OK_L Dwell Time	75		120	ms
T3	VIN_OK_L delay to AC		200		ms

* T2 is the minimum VIN_OK_L de-assertion dwell time that is initiated when the PSU has declared a loss of input voltage.

Table 1. VIN_OK_L Timing Requirements

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8.7. TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. All outputs must rise monotonically. T*able 2* shows the timing requirements for the power supply being turned on and off two ways:
1) Via the AC input with PSON_L held low;
2) Via the PSON_L signal with the AC input applied.
The PSU needs to remain off for 5 second minimum after PWOK_L is de-asserted.

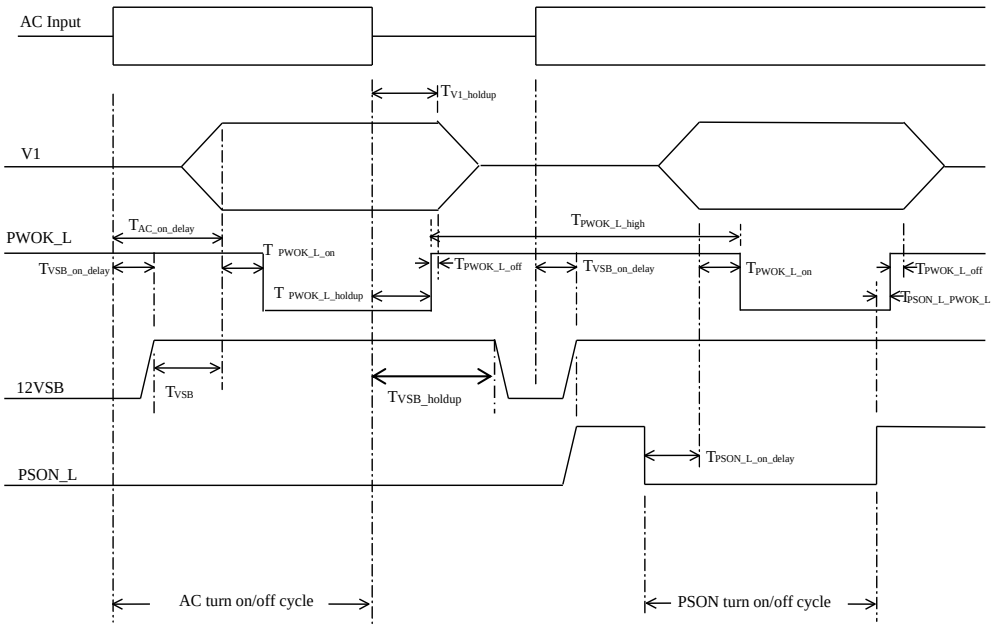


Figure 8. Turn On/Off Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$T_{VSB_on_delay}$	Delay from AC being applied to 12VSB being within regulation.			3000	ms
$T_{AC_on_delay}$	Delay from AC being applied to all output voltages being within regulation.			4000	ms
T_{V1_holdup}	Time V1 > 41 V after loss of AC.	10			ms
$T_{PWOK_L_holdup}$	Delay from loss of AC to de-assertion of PWOK_L	5			ms
$T_{PSON_L_on_delay}$	Delay from PSON_L active to output voltages within regulation limits.	5		400	ms
$T_{PSON_L_PWOK_L}$	Delay from PSON_L deactivate to PWOK_L being de-asserted.			5	ms
$T_{PWOK_L_on}$	Delay from output voltages within regulation limits to PWOK_L asserted at turn on.	100		500	ms
$T_{PWOK_L_off}$	Delay from PWOK_L de-asserted to output voltages dropping out of 75%.	1			ms
$T_{PWOK_L_high}$	Duration of PWOK_L being in the de-asserted state during an off/on cycle using AC or the PSON_L signal.	100			ms
T_{VSB}	Delay from 12VSB being in regulation to O/Ps being in regulation at AC turn on.	50		1000	ms
T_{VSB_holdup}	Time the 12VSB output voltage stays within regulation after loss of AC.	40			ms

Table 2. Timing Requirements

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8.8. CAN BUS INTERFACE

The CAN bus interface serves for information exchange between paralleled power supplies (e.g. for current share) and for communication with a system controller (e.g. voltage setting, monitoring). The CAN bus operates at 1000 kbit/s with a Bel defined protocol. System wiring requires only interconnection of CAN_H and CAN_L lines, in addition a 120 Ohm termination resistor is required at each end of the CAN bus to prevent signal reflections.

NOTE: To enable active current share between paralleled power supplies, their CAN bus interface must be interconnected.

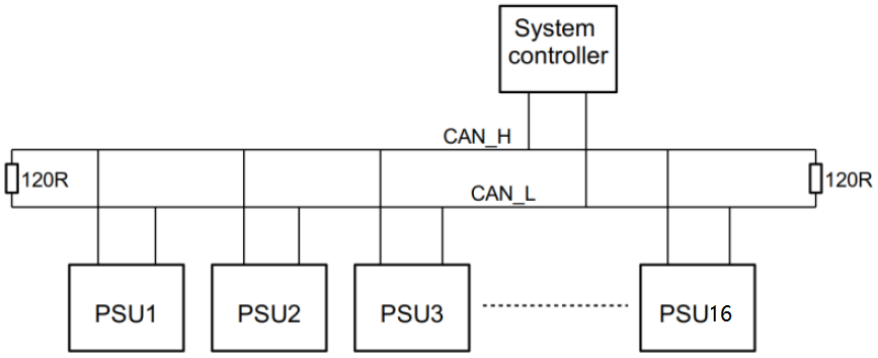


Figure 9. CAN bus wiring

8.9. ADDRESSING

The address for I²C communication can be configured by pulling address input pins A3, A2, A1 and A0 either to SGND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A3 / A2 / A1 / A0 pin to be in High Level if left open. A fixed addressing offset exists for the Controller.

A3	A2	A1	A0	I2C Address
0	0	0	0	0xB0
0	0	0	1	0xB2
0	0	1	0	0xB4
0	0	1	1	0xB6
0	1	0	0	0xB8
0	1	0	1	0xBA
0	1	1	0	0xBC
0	1	1	1	0xBE
1	0	0	0	0xC0
1	0	0	1	0xC2
1	0	1	0	0xC4
1	0	1	1	0xC6
1	1	0	0	0xC8
1	1	0	1	0xCA
1	1	1	0	0xCC
1	1	1	1	0xCE

Table 3. Address and Protocol Encoding

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8.10. FRONT LED

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and yellow, and indicates AC and DC power presence and warning or fault conditions. *Table 4* lists the different LED status.

OPERATING CONDITION	LED STATE
Output ON and OK	Solid GREEN
No AC power to all power supplies	OFF
AC present / Only 12VSB on (PS off)	2Hz Blink GREEN
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink YELLOW
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	Solid YELLOW
Power supply in FW upload mode	2Hz Blink GREEN

Table 4. LED Status

8.11. CURRENT SHARE

The front-end has an active current share scheme implemented for V1. CAN bus interface of the paralleled power supplies need to be interconnected to activate the sharing function.

The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +1 V.

The standby output uses a passive current share method (droop output voltage characteristic).

Due to non-ideal current share the maximum total output power of paralleled power supplies is less than the theoretical maximum and is defined in Table 5.

No of paralleled PSUs	Maximum available power on main output V		Maximum available power on standby output (optional)	
	without redundancy	n+1 redundancy	without redundancy	n+1 redundancy
1	3600 W	-	30 W	-
2	7000 W	3600 W	47 W	30 W
3	10400 W	7000 W	65 W	47 W
4	13800 W	10400 W	83 W	65 W
5	17200 W	13800 W	101 W	83 W
6	20600 W	17200 W	119 W	101 W

Table 5. Power available when PSU in redundant operation

9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The TET3600-48-104RA is provided with a reverse airflow, which means the air enters through the front of the supply and leaves at the rear.

9.1. FAN CONTROL

The average speed of the two individual fans within the dual-axis-fan is controlled to meet the reference. The reference is given by the maximum of following 3 items:

- Load depending Fan Speed curve, see *Figure 10*.
- Fan Speed depending ambient temperature.
- System commanded Fan Speed through CAN bus or I2C bus.

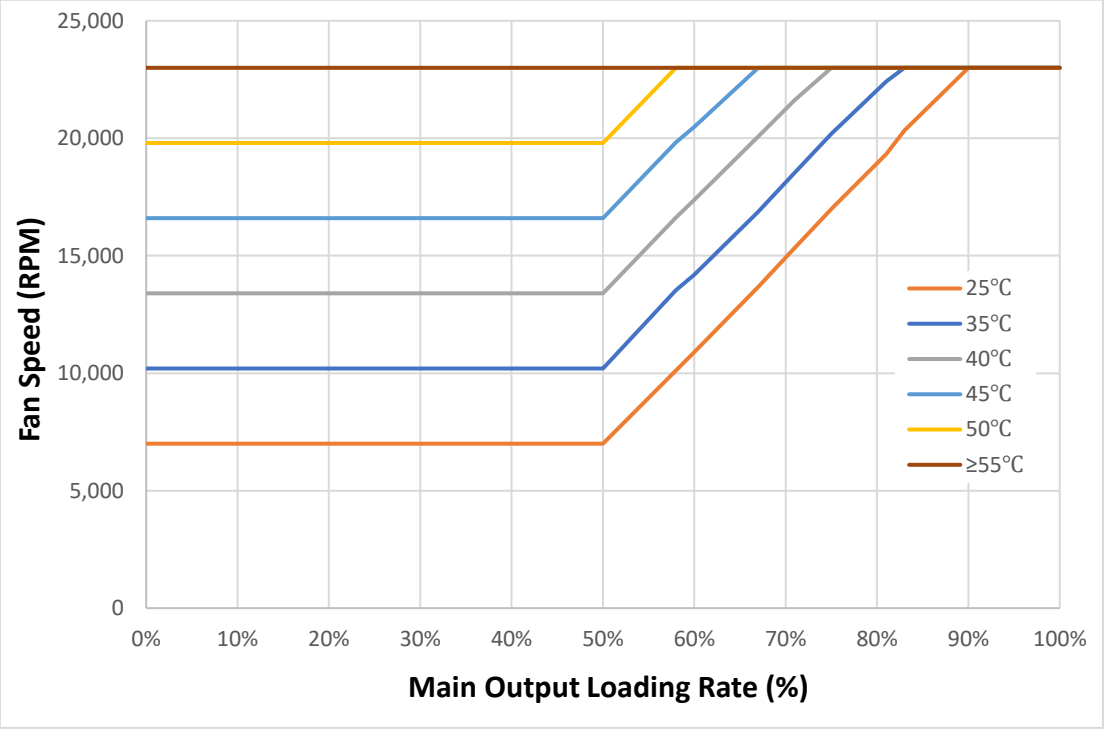


Figure 10. Fan speed versus main output load

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10. ELECTROMAGNETIC COMPATIBILITY

10.1. IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55035.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV (non-metallic user accessible surfaces)	A
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation	A
Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute	A
Surge	IEC / EN 61000-4-5, level 3 Line to earth: ±2 kV Line to line: ±1 kV @	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms	A
Voltage Dips and Interruptions	IEC/EN 61000-4-11 1: Vi 230 Volts, 80% Load, Phase 0 °, Dip 100%, Duration 10 ms 2: Vi 230 Volts, 100% Load, Phase 0 °, Dip 100%, Duration < 100 ms 3. Vi 230 Volts, 100% Load, Phase 0 °, Dip 100%, Duration > 150 ms	A V1: B, VSB: A B

10.2. EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN55032 / CISPR 32: 0.15 … 30 MHz, QP and AVG	Class A
Radiated Emission	EN55032 / CISPR 32: 30 MHz … 1 GHz, QP	Class A
Harmonic Emissions	IEC61000-3-12, Vin = 230 VAC, 50 Hz, 100% Load	Class A
Audible Noise LpA	$V_{i\,nom}$, 50% $I_{o\,nom}$, T_A = 25°C, at the bystander position	65 dBA
AC Flicker	IEC / EN 61000-3-3, d_{max} < 3.3%	PASS

For HVDC input, 80% load can meet EMC performance.

11. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to UL/CSA 62368-1, EN/IEC 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Agency Approvals	Approved to the latest edition of the following standards: UL/CSA 62368-1, EN/IEC 62368-1		Approval		
	Isolation Strength	Input (L/N) to case (PE) Input (L/N) to output Output to case (PE)		Basic Reinforced Functional		
d_C	Creepage / Clearance	Primary (L/N) to protective earth (PE) Primary to secondary		According to UL/CSA 62368-1, EN/IEC 62368-1		
	Electrical Strength Test	Input to case Input to output (tested by manufacturer only) Output to case	2500 5000 500			VDC

12. ENVIRONMENTAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	$V_{i\,min}$ to $V_{i\,max}$, I_{nom}, $I_{SB\,nom}$ at 5000 m	0		+45	°C
		$V_{i\,min}$ to $V_{i\,max}$, I_{nom}, $I_{SB\,nom}$ at 2000 m	0		+50	°C
T_{Aext}	Extended Temp. Range	Derated output	+50		+65	°C
T_S	Storage Temperature	Non-operational	-40		+70	°C
	Altitude	Operational, above Sea Level (see derating)	-		5000	m

13. MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		103.6		mm
		Heigth		40		mm
		Depth		255.8		mm
m	Weight			1.66		kg

NOTE: A 3D step file of the power supply casing is available on request.

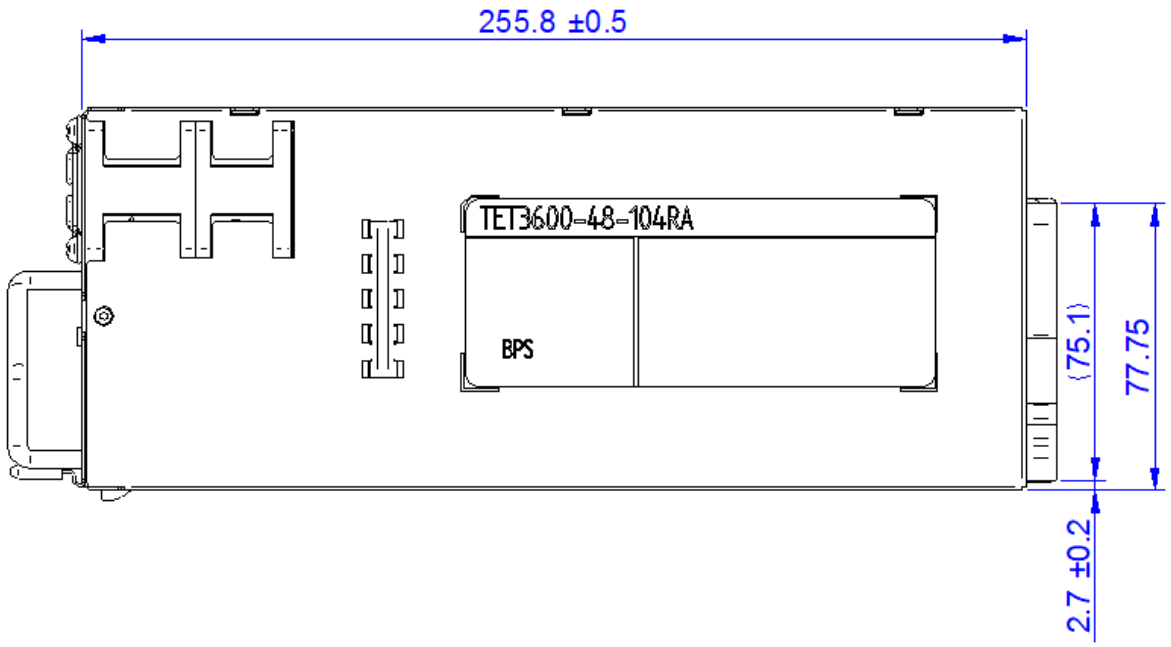


Figure 11. Top view

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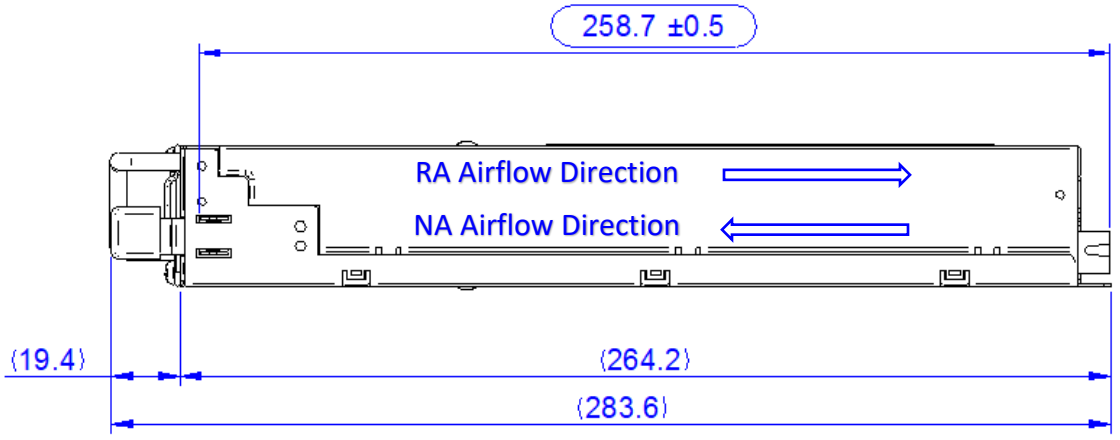


Figure 12. Side view

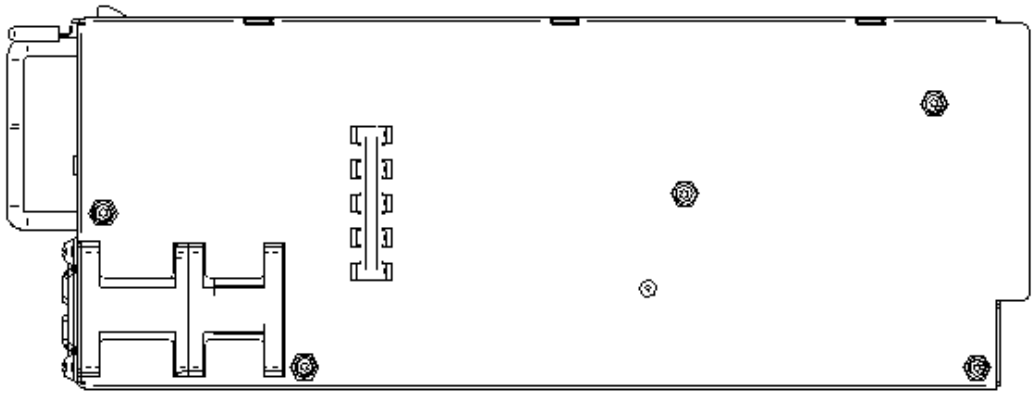


Figure 13. Bottom view

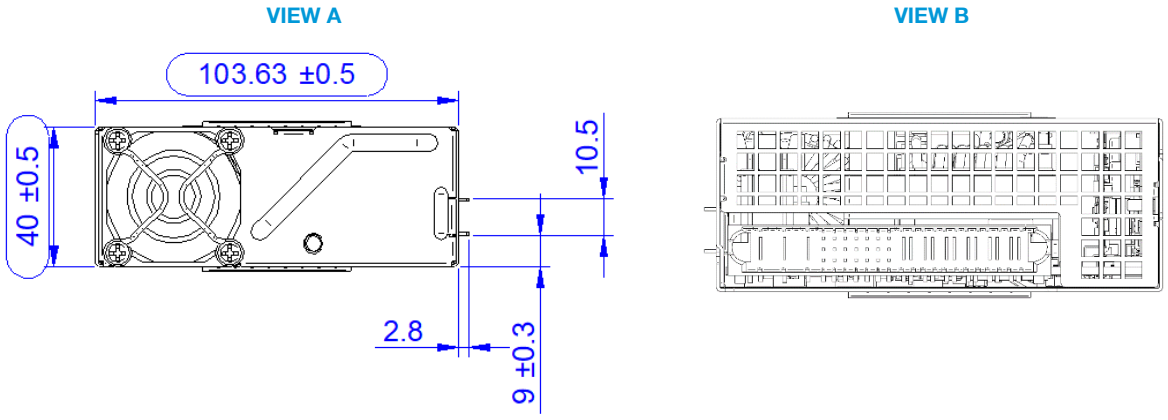


Figure 14. Front and Rear view

14. CONNECTORS

Rear side PSU connector serves as interface for input power, output power and signals. To guarantee proper mating sequence, the below noted connector P/N is required to be used.

PSU side: FCI Pwr Blade ULTRA 10127397-10H2410LF or equivalent

Mating connector: FCI Pwr Blade ULTRA 10127401-09H2410LF

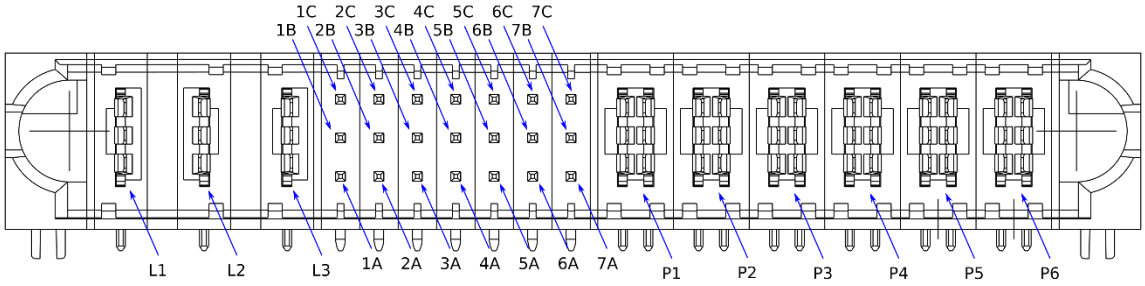


Figure 15. PSU rear side connector, view from mating side

PIN NUMBER	SIGNAL NAME	COMMENTS
P6-P4	Positive Power	Positive Output Voltage Pin
P3-P1	Negative Power	Negative Output Voltage Pin
1A	PSKILL	Short Pin. Short to Signal GND to enable PSU. PSU off if floating.
1B	NC	Reserved for future use.
1C	ADDR3	Digital Input. Defines bit 3 of address.
2A	Signal GND	
2B	Vsb+	Positive output rail of Vsb output. Referred to negative power pin.
2C	Vsb+	Positive output rail of Vsb output. Referred to negative power pin.
3A	ADDR0	Digital Input. Defines bit 0 of address.
3B	PRESENT_L	Power supply seated, active-low
3C	ADDR1	Digital Input. Defines bit 1 of address.
4A	SCL	PMBus SCL signal
4B	ADDR2	Digital Input. Defines bit 2 of address.
4C	CAN_L	CAN bus differential pair low signal
5A	SDA	PMBus SDA signal
5B	Signal GND	
5C	CAN_H	CAN bus differential pair high signal
6A	SMB_ALERT	SMB Alert signal output: active-low
6B	Signal GND	
6C	PSON_L	Digital Input. Pull low to enable the PSU output
7A	VINOK_L	Open Drain Output. Pulled low if input voltage is present and in operating range
7B	PWOK_L	Open Drain Output. Pulled low if the output voltage of the main and standby output is in range within the regulation limits.
7C	Signal GND	
L1	Line	AC line input
L2	Neutral	AC neutral input
L3	PE	Protective Earth

Table 6. Pin assignment

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15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PN	SOURCE
	**Interface Utility** Windows compatible GUI to program, control and monitor Bel products	N/A	belfuse.com/power-solutions
	**Evaluation Board** Connector board to operate TET3600-48-104xA. Includes an onboard USB to I2C converter (use I2C Utility as desktop software)	YTM.20002.0	Bel Power Solutions

16. REVISION HISTORY

REV	DESCRIPTION		PSU PRODUCT VERSION	DATE	AUTHOR
1	Initial Draft.		V001	31-May-2021	GT
A	Release to A	Update the spec based on final test results	A	25-Apr-2022	GT
B		Add “or equivalent” to output connector at section 14 Update the safety approve standard at section 11	B	18-Aug-2023	Xiao Xue

For more information on these products consult: tech.support@psbel.com

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TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.