TET3000 Series

TET3000-12-054xDSxxx
TET3000-12xDS412
DC-DC Front-End Power Supplies

The TET3000 series is a 3000 Watt DC to DC power supply that converts -40 to -72 VDC voltage into an insulated main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The TET3000 series utilizes full digital control architecture for greater efficiency, control, and functionality.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

RoHS Compliant

Key Features & Benefits

- High Efficiency, typ. 95% efficiency at half load
- Wide input voltage range from -40 to -72 VDC
- 3000 W continuous output power capability
- Always-on standby output (Optional for 12VSB / 3 A or 5VSB / 3 A)
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- High power density design: 71 W/in^3
- Small form factor: 54.5 x 40.0 x 321.5 mm (2.14 x 1.57 x 12.66 in)
- Power Management Bus communication interface for control, programming and monitoring
- Over temperature, output over voltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- Black Box recorder available
- Status LED with fault signaling

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

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Please read our datasheet & drawing disclaimer here.

1. ORDERING INFORMATION

MODELS WITH 5 V STANDBY OUTPUT

TET	3000	-	12	-	054	x	D	x
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow	Input	Specific code[2]
TET Front-End	3000 W		12 V		54.0 mm	N: Normal [1] R: Reverse [1]	DC	x = Blank x = S+3 digits

MODELS WITH 12 V STANDBY OUTPUT

TET	3000	-	12	x	D	S412
Product Family	Power Level	Dash	V1 Output	Airflow	Input	VSB output
TET Front-End	3000 W		12 V	N: Normal [1] R: Reverse [1]	DC	12VSB

[1] "N" Normal Airflow (NAF) from Output connector to Input DC connector, "R" Reverse Airflow from Input DC connector to Output connector.

[2] Contact factory for availability of Specific code.

2. OVERVIEW

The TET3000 series DC/DC power supply is a DSP controlled, highly efficient front-end power supply. It incorporates state of the art technology and uses an interleaved forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency.
With a wide input DC voltage range the TET3000 series maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.
An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.
The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.
Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.
Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

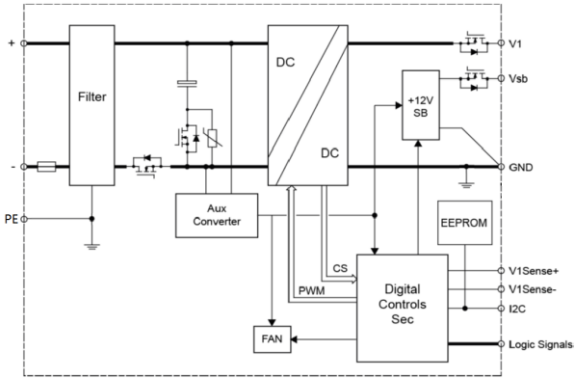

Figure 1. TET3000 Series Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
Vi maxc	Maximum Input	Continuous		-75	VDC

4. INPUT

General Condition: T_A = -5… +50 °C, unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi nom	Nominal input voltage		-48		-60	VDC
Vi	Input voltage	Normal operation (from Vi min to Vi max)	-40		-72	VDC
Ii	Input current	Vi > Vi min			86	A
Ii pk	Inrush current limitation	From Vi min to Vi max, T_A = 25°C, cold start			80	A
Vi_{VSB_on}	Turn-on standby input voltage	Ramping up	-30		-32	VDC
Vi_{VSB_off}	Turn-off standby input voltage	Ramping down	-28		-30	VDC
Vi_{V1_on}	Turn-on V1 input voltage[1]	Ramping up	-38		-40	VDC
Vi_{V1_off}	Turn-off V1 input voltage	Ramping down	-37		-39	VDC
η	Efficiency [2]	Vi = -48 VDC; -60 VDC; 20% load	90	94.5		%
		Vi = -48 VDC; -60 VDC; 50% load	94	95.3		%
		Vi = -48 VDC; -60 VDC; 100% load	91	92.5		%
T_{V1_holdup}	Hold-up Time V1	V_1 > 10.8 V, V_i = -48 VDC, $P_{0\ nom}$ *(from DC input lost to V1 lost to 10.8 V)*	1			ms
T_{VSB_holdup}	Hold-up time Vsb	V, V_i = -48 VDC, $P_{0\ nom}$	3			ms

4.1 INPUT FUSE

120 A (or equivalent) input fuse in the negative voltage path inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

4.3 INPUT UNDER-VOLTAGE

If the input voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 EFFICIENCY

High efficiency (*see Figure 2*) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

[1] The Front-End is provided with a minimum hysteresis of 1V during turn-on and turn-off within the ranges.
[2] Efficiency measured without fan power per EPA server guidelines.

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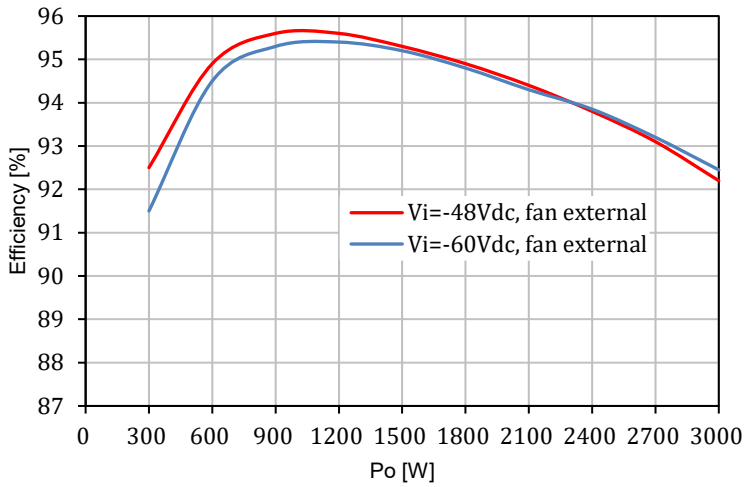

Figure 2. Efficiency vs. Output Power

4.5 DC LINE TRANSIENT TEST

MINUS 72 VDC LINE TRANSIENT TEST

A standard line voltage momentary transient test is shown below. This test simulates a momentary voltage overshoot. This should not affect the operation of the PSU; the output voltage should remain in regulation. This test shall be conducted every 10 secs for 30 min (180 times total).

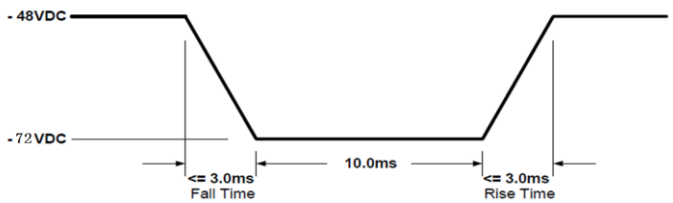

Figure 3. Minus 72 VDC Line Transient Test

0 V LINE TRANSIENT TEST

A standard line voltage momentary blackout test is shown below. This test simulates a momentary switch throw off-on, see graph below. The power supply should restart, not latch. This test shall be conducted 3 times in 10 min intervals.
Practically a blackout of any duration should not damage the power supply in any way and not cause a latch off condition.

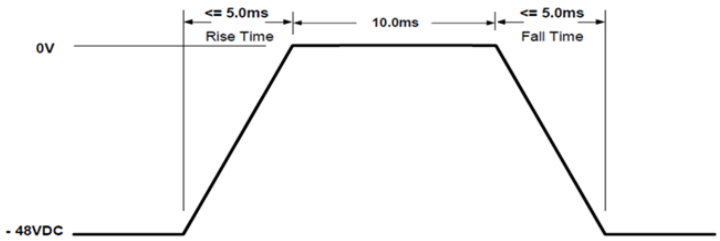

Figure 4. 0 V Line Transient Test

5. OUTPUT

General condition: T_A = -5…+50 °C, V_i = -48 VDC unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.0		VDC
$V_{1\ set}$	Output Set Point Accuracy		-0.5		+0.5	%$V_{1\ nom}$
$dV1$ load	Load Regulation	0 to 100% $I_{1\ nom}$		150		mV
$dV1$ line	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$		50		mV
$dV_{1\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$	-5		+5	%$V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power[1]	$V_{i\ min}$ to $V_{i\ max}$		3000		W
$I_{1\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$		250		ADC
$V_{1\ pp}$	Output Ripple Voltage [2]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, 20MHz Bandwidth			150	mVpp
$dI_{1\ share}$	Current Sharing	Deviation from I1 tot / N, I_N > 20%	-5		+5	A
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ nom}$		8		VDC
$dV_{1\ dyn}$	Dynamic Load Regulation[3]	ΔI1 =40% $I_{1\ nom}$, I1 = 5% … 100% $I_{1\ nom}$, dI1/dt = 1A/µs, 2000µF capacitive loading	-5		+5	% $V_{1\ nom}$
t_{rec}	Recovery Time	recovery within 1% of $V_{1\ nom}$		2		ms
$t_{V1\ rise}$	Output Voltage Rise Time	V_1 = 10…90% $V_{1\ nom}$			30	ms
$t_{VIN\ V1}$	Start-up Time from DC	V_1 = 90% $V_{1\ nom}$			3	s
$t_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{1\ nom}$			0.6	V
$C_{V1\ load}$	Capacitive Loading				30	mF
12V Standby Output						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 ·$I_{SB\ nom}$, T_A = 25°C		12.0		VDC
$V_{SB\ set}$	Output Set point Accuracy		-0.5		+0.5	%$V_{SB\ nom}$
dV_{SB} load	Load Regulation	0 to 100% $I_{SB\ nom}$		100		mV
dV_{SB} line	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$		20		mV
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	%$V_{SB\ nom}$
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		36		W
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$		3		ADC
$V_{SB\ pp}$	Output Ripple Voltage [1]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, 20 MHz bandwidth			120	mVpp
$dV_{SB\ dyn}$	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5% … 100% $I_{SB\ nom}$, dI_{SB}/dt = 1 A/µs,	-5		+5	% $V_{SB\ nom}$
t_{rec}	Recovery Time	recovery within 1% of $V_{SB\ nom}$		2		ms
$t_{VSB\ rise}$	Output Voltage Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$,			30	ms
$t_{VIN\ VSB}$	Start-up Time from DC	V_{SB} = 90% $V_{SB\ nom}$			2.7	s
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{SB\ nom}$			0.6	V
$C_{VSB\ load}$	Capacitive Loading				1000	µF

[1] When Vi is below 44V, output power operation at 2800W, only for products with Normal Airflow.
[2] Ripple noise and dynamic load measured with a 10 µF low ESR capacitor in parallel with a 0.1 µF ceramic capacitor at the point of measurement.
[3] Dynamic load testing the input voltage needs to be above 40.8V.

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5V Standby Output						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_A = 25°C		5.0		VDC
$V_{SB\ set}$	Output Set point Accuracy		-1		+1	%$V_{SB\ nom}$
dV_{SB} load	Load Regulation	0 to 100% $I_{SB\ nom}$		100		mV
dV_{SB} line	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$		20		mV
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	%$V_{SB\ nom}$
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		15		W
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$		3		ADC
$V_{SB\ pp}$	Output Ripple Voltage [1]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, 20 MHz bandwidth			75	mVpp
$dV_{SB\ dyn}$	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5% … 100% $I_{SB\ nom}$, dI_{SB}/dt = 1 A/µs,	-5		+5	% $V_{SB\ nom}$
t_{rec}	Recovery Time	recovery within 1% of $V_{SB\ nom}$		2		ms
$t_{VSB\ rise}$	Output Voltage Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$,			30	ms
$t_{VIN\ VSB}$	Start-up Time from DC	V_{SB} = 90% $V_{SB\ nom}$			2.7	s
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{SB\ nom}$			0.25	V
$C_{VSB\ load}$	Capacitive Loading				1000	µF

5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 5.* Alternatively, separated ground signals can be used as shown in *Figure 6.* In this case the two ground planes should be connected together at the power supplies ground pins.

NOTE: Within the power supply the output GND pins aren't connected to the Chassis.

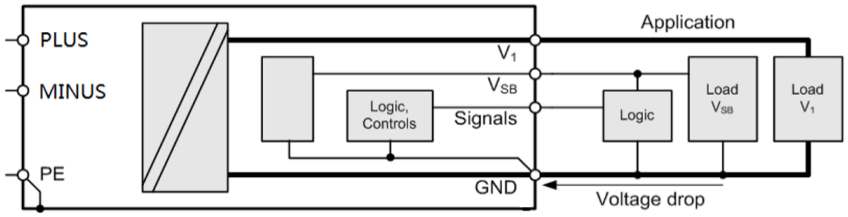

Figure 5. Common Low Impedance Ground Plane

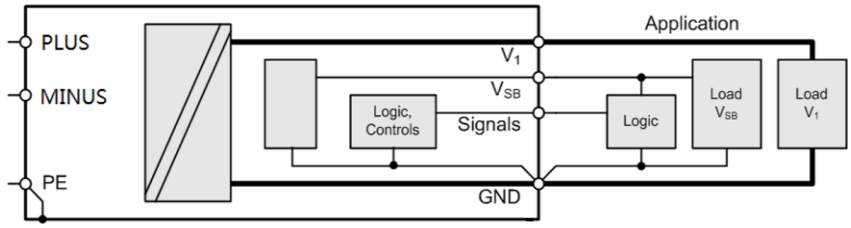

Figure 6. Separated Power and Signal Ground

5.2 RIPPLE / NOISE

The test set-up shall be as follows.

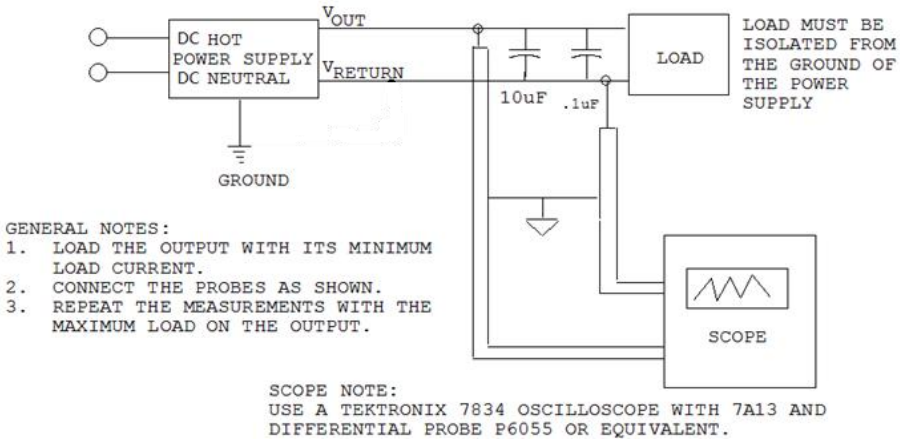

Figure 7. Output ripple Test Setup

NOTES: Load must be isolated from the safety ground to *Figure 7.*

When performing this test, the probe clips and capacitors should be located close to the load.

6. PROTECTION

General Condition: T_A = -5… +50 °C, unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)	Not user accessible		120		A
$V_{1\,OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type	13.0		14.5	VDC
$V_{VSB\,OV}$	OV Threshold V_{SB}	Over Voltage V_{sb} Protection, Automatic recovery Type	105		120	%VSB
$V_{1\,UV}$	UV Threshold V_1	Under Voltage V_1 Protection, Latch-off Type		11.2		VDC
$V_{VSB\,UV}$	UV Threshold V_{SB}	Under Voltage V_{sb} Protection, Automatic recovery Type		90		%VSB
$I_{V1\,OC}$	OC Limit V_1	Over Current Limitation, Five “hiccup” auto recovery cycles, followed by a latched shutdown	252		288	A
		Vi<44V, for products with normal airflow	235		260	A
$I_{VSB\,OC}$	OC Limit V_{SB}	Over Current Limitation, Automatic recovery Type	3.1		4.5	A
T_{SD}	Over Temperature on Critical Points	Automatic shut-down		120		°C

6.1 OVER VOLTAGE PROTECTION

The TET3000 Series supplies provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the main output will shut down and latch the fault condition. the standby output VSB will turn off the whole power supply if standby output VSB over-voltage protection has been triggered. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input. VSB will be auto-recovered after removing OVP limit.

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6.2 UNDER VOLTAGE DETECTION

Both main and standby outputs are monitored. PWOK_H pin signal if the output voltage exceeds ±5% of its nominal voltage. The main output will latch off if the main output voltage when V1 falls below 11.2 V (typically in an overload condition), the latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input.
If the standby output leaves its regulation bandwidth for more than 10ms then the main output is disabled to protect the system.

6.3 CURRENT LIMITATION

When main output runs in current limitation mode its output will turn OFF below 2 V but will retry to recover every 1 s interval. If current limitation mode is still present after the unit retry, after five "hiccup" auto recovery cycles, followed by a latched shutdown, The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input.

The main output power will decrease if the ambient (inlet) temperature increases beyond 50°C. see Figure 19 Temperature and Fan Control for additional information.

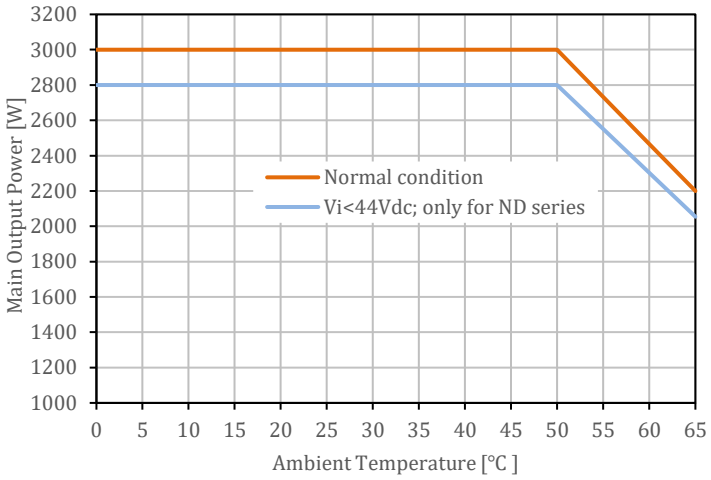

Figure 8. Power Derating Curve with Ambient Temperature

The standby output has a hiccup current limitation implemented. If the standby current exceeds ISB Lim the standby converter switches off and retries automatically after 1 second off time.

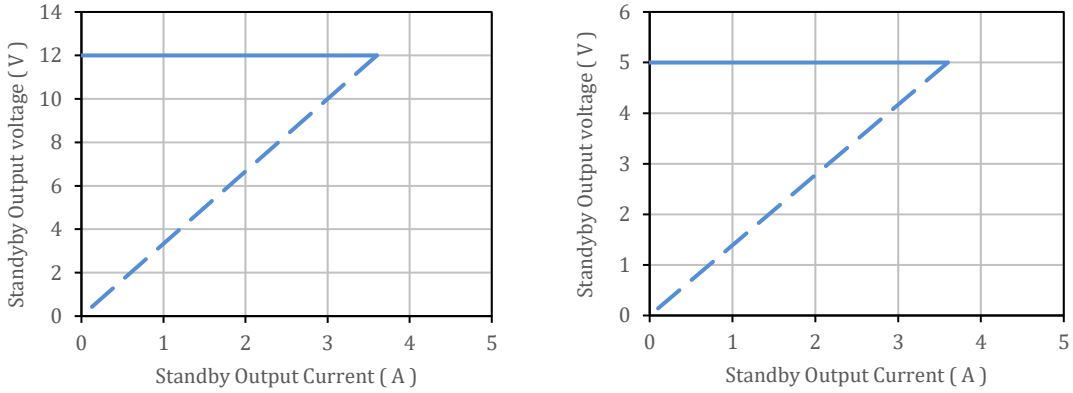

Figure 9. Current Limitation on 12VSB / 5VSB

NOTE: A failure on the main output does not shut down the standby output. But failure on the Standby output will shut down both Main and Standby outputs.

6.4 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature.
In an OTP condition the PSU will shut down, when the power supply temperature drops to within specified limits, the power supply shall restore power automatically, the OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition, the OTP trip temperature level shall be at least 5°C higher than over temperature warning threshold level.

7. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to TET3000 series Power Management Bus Communication Manual.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,mon}$	Input Voltage	$V_{i\,min\,LL} \leq V_i \leq V_{i\,max}$	-2		+2	VDC
$I_{i\,mon}$	Input Current	$I_i \leq 20A$ $I_i > 20A$	-1 -5		+1 +5	ADC %
$P_{i\,mon}$	Input Power	120 W ≤ Pi ≤ 1000 W Pi > 1000 W	-60 -6		+60 +6	W %
$V_{1\,mon}$	V_1 Voltage		-2		+2	%
$I_{1\,mon}$	V_1 Current	$10A < I_1 \leq 50A$ $I_1 > 50A$	-2.5 -5		+2.5 +5	A %
P_{nom}	V_1 Output Power	120 W ≤ P_o ≤ 700 W P_o > 700 W	-35 -5		+35 +5	W %
$V_{SB\,mon}$	Standby Voltage		-0.3		+0.3	V
$I_{SB\,mon}$	Standby Current	$I_{SB} \leq I_{SB\,nom}$	-0.5		+0.5	A
T_{ambmon}	*Ambient Temperature*	-5°C ≤ T_{amb} ≤ 50°C	-3		+3	°C

Table 1 Power Management Bus Sensors Accuracy

8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
PSON_L						
V_{IL}	Input Low Level Voltage		-0.2		0.8	V
V_{IH}	Input High Level Voltage		2.4		3.5	V
$I_{IL,\,H}$	Maximum Input Sink or Source Current		0		1	mA
$R_{pu_intPSON_L}$	Internal Pull Up Resistor on PSON_L			10		kΩ
PWOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 50 uA	2.6		3.5	V
R_{puPWOK_H}	Internal Pull Up Resistor on PWOK_H			1		kΩ
INOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V

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V_{OH}	Output High Level Voltage	I_{source} < 50 µA	2.6		3.5	V
R_{pulNOK_H}	Internal Pull Up Resistor on INOK_H			1		kΩ

SMB_ALERT_L Output						
V_{ext}	Maximum External Pull Up Voltage				12	V
V_{OL}	Output Low Level Voltage	I_{source} < 4 mA	0		0.4	V
I_{OH}	Maximum High-Level Leakage Current				10	µA
$R_{puSMB_ALERT_L}$	Internal Pull Up Resistor on SMB_ALERT_L			NA		kΩ

8.2 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.
With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.3 CURRENT SHARE

The TET3000 series supplies have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.
The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.
The 12 VSB output is not required to actively share current between power supplies (passive sharing).

8.4 PRESENT_L OUTPUT

The PRESENT_L pin is wired to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low level voltage if power supply is seated.

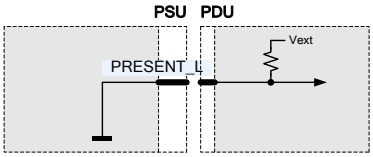

Figure 10. PRESENT_L Connection

8.5 PSON_L INPUT

The PSON_L is an internally pulled- up (3.3V) input signal to enable / disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. *Figure 11* shows PSON_L circuit used in PSU and proposed connections.

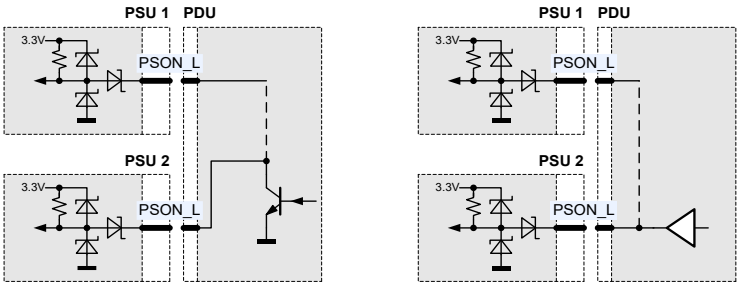

Figure 11. PSON_L connection

8.6 PWOK_H OUTPUT

PWOK_H is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when DC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK_H will be de-asserted to a LOW state.

8.7 SMB_ALERT_L OUTPUT

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, over-current, under voltage. This signal may also indicate the power supply is operating in an environment exceeding the specified limits.

8.8 IN_OK_H OUTPUT

This signal will be asserted, driven high, by the power supply to indicate that the input voltage meets the minimum requirements of the parametric PSU specification.

The PSU shall de-assert (drive low) under input over-voltage condition.

8.9 TIMING REQUIREMENTS

These are the timing requirements for power supply operation. All outputs must rise monotonically.

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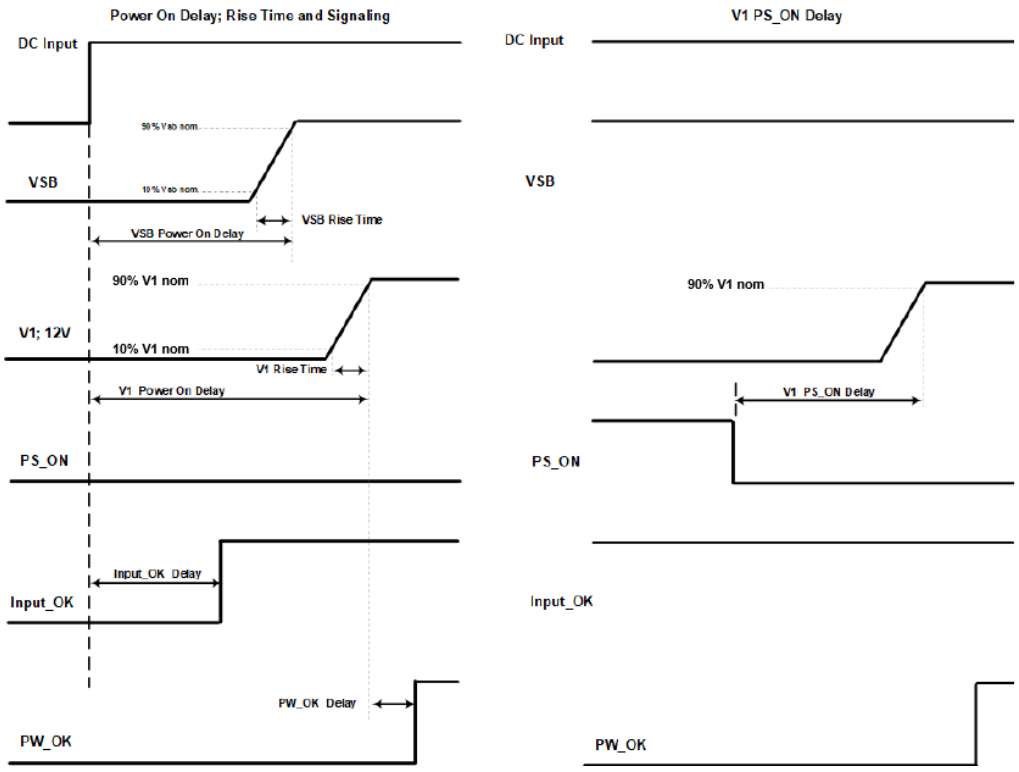

Figure 12. Turn On Timing

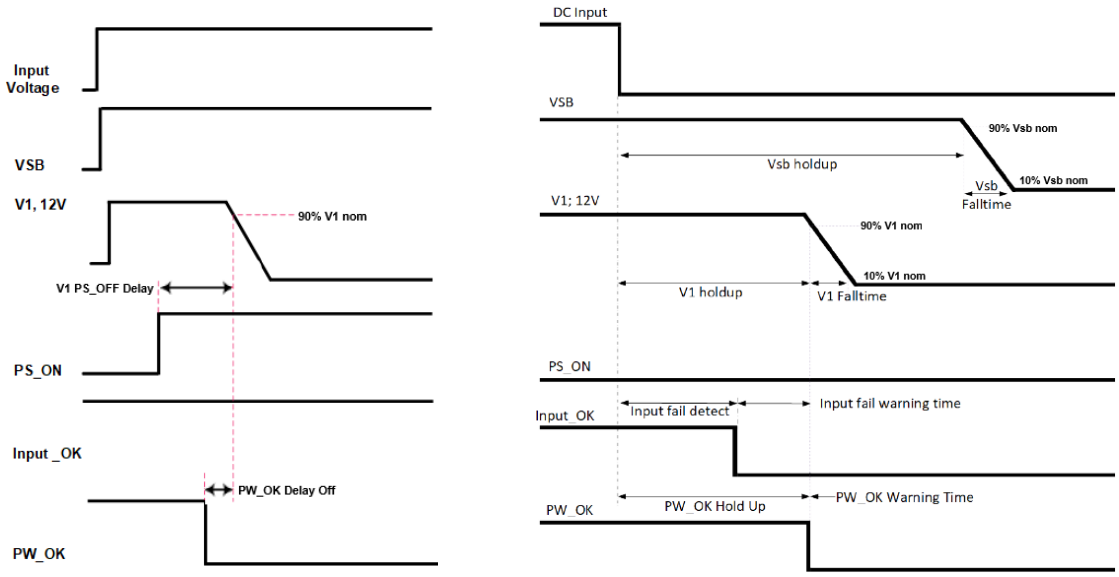

Figure 13. Turn Off Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
V1 Rise time	V1 rising from 10% to 90% V1 nom.			30	ms
Vsb Rise time	Vsb rising from 10% to 90% Vsb nom.			30	ms
Vsb Power-on-delay	From application of Vin nom. to Vsb reaching 90% Vsb, nom.			2700	ms
V1 Power-on-delay	From application of Vin to V1 reaching 90% of Vout nom.			3000	ms
V1 PS_ON delay	From PS_ON signal edge to V1 reaching 90% of Vout nom.			500	ms
V1 PW_OK delay	From V1 reaching 90% to asserted PW_OK signal.			150	ms
Input_OK delay	From application of Vin to assertion of Input_OK Signal edge.			1200	ms
V1 PS_OFF delay	From the rising edge of PS_ON signal to V1 falling below 90% V1 nom.			7	ms
PW_OK_Delay_Off	Warning time, loss of V1 output (falls to 90% Vout nom.) due to PS_ON signal being negated (upon change from low to high state)	100			us
Vsb holdup	From loss of Vin to Vsb falling to 90% Vsb nom.	3			ms
V1 holdup	From loss of Vin to V1 falling to 90% Vout nom.	1			ms
Input fail detect	From loss of Vin to falling edge of Input_OK signal.			2	ms
Input fail warning time	Input_OK signal warning time: loss of output due to loss of input, measured from falling edge of Input_fail detect to V1 falling to 90% Vout nom.	0.2			ms
PW_OK Hold Up	From loss of input power	0.5			ms
PW_OK Warning Time	This signal does not guarantee V1 loss warning time. (due to loss of input power)	-1.0		1.5	ms

Table 2. Timing Requirements

8.10 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and yellow and indicates DC and DC power presence and warning or fault conditions. *Table 3* lists the different LED status.

POWER SUPPLY CONDITION	LED STATUS
12V main on and in voltage regulation band (Active mode)	Solid Green
12V main off (Standby mode)	Green blinking (1Hz)
No DC input power to any of the system power supplies	OFF
No DC input power, but other PSU in the system operating	Solid Yellow
Warning event (Output OCW/ OTW/ Fan Warming)	Yellow blinking (1Hz)
Fault event (Input OVP, Output OVP/UVP, OCP, OTP, Fan Fail, Other internal fault)	Solid Yellow
FW update	Green blinking (2Hz)

Table 3. LED Characteristics

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9. I²C / POWER MANAGEMENT BUS COMMUNICATION

The TET3000 series supplies are communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in *Table 4* further characterized through:

- SCL/SDA pull-up resistor is 3kΩ in PSU side
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >35 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

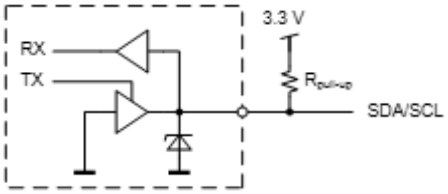

Figure 14. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input DC voltage is provided. If no DC is present, communication to the unit is possible as long as it is connected to a life V_{SB} output or V_1 output (provided e.g. by the redundant unit).

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
V_{iL}	Input low voltage		-0.5		1.0	V
V_{iH}	Input high voltage		2.3		5.5	V
V_{hys}	Input hysteresis		0.15			V
V_{oL}	Output low voltage	3 mA sink current	0		0.4	V
t_r	Rise time for SDA and SCL		20+0.1Cb[1]		300	Ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < Cb[3] < 400 pF	20+0.1Cb[2]		250	Ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10		10	µA
C_i	Internal Capacitance for each SCL/SDA				0	pF
f_{SCL}	SCL clock frequency		0		100	kHz
R_{pu}	External pull-up resistor	f_{SCL} ≤ 100 kHz			1000 ns / Cb	Ω
R_{pu_int}	Internal pull-up resistor			3		KΩ
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0			µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7			µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0			µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7			µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0		3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250			ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0			µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5			ms

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 4. I²C / SMBus Specification

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

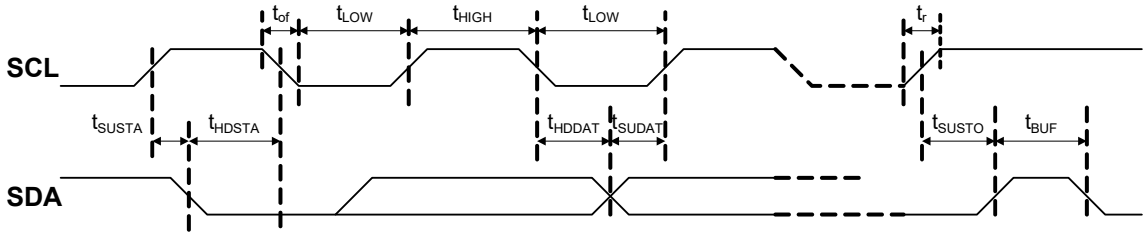

Figure 15. I²C / SMBus Timing

9.1 ADDRESS / PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the address by connecting a resistor to V1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

NOTE: - If the APS pin is left open, the supply will operate with the Power Management Bus protocol at controller / EEPROM addresses 0xBE / 0xAE.

- The APS pin is only read at start-up of the power supply. Therefore, it is not possible to change address dynamically.

.

R_{APS} (Ω) [1]	Protocol	I2C Address [2]	
		Controller	EEPROM
820	Power Management Bus	0xB0	0xA0
2700		0xB2	0xA2
5600		0xB4	0xA4
8200		0xB6	0xA6
15000	Power Management Bus	0xB8	0xA8
27000		0xBA	0xAA
56000		0xBC	0xAC
180000		0xBE	0xAE

Table 5. Address and Protocol Encoding

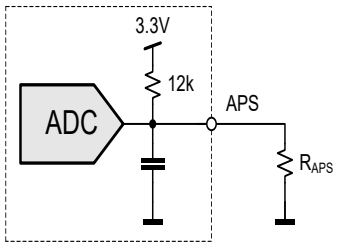

Figure 16. I2C address setting

9.2 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see *Figure 17*).

An I2C driver device assures logic level shifting (3.3/5V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, firstly the write protection needs to be disabled by sending the appropriate command to the DSP. By default, the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

---

2 E12 resistor values, use max 5% resistors, see also *Table 5*

3 The LSB of the address byte is the R/W bit

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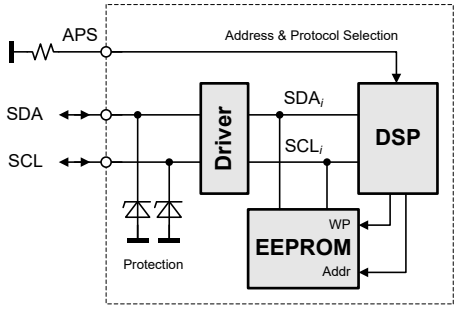


Figure 17. I2C Bus to DSP and EEPROM

9.3 EEPROM PROTOCOL

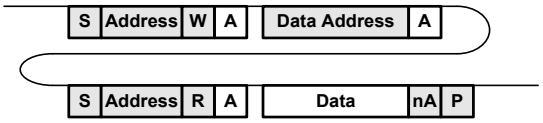
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



9.4 POWER MANAGEMENT BUS PROTOCOL

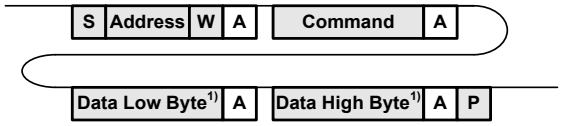
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed.
The TET3000 series supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >35 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions.

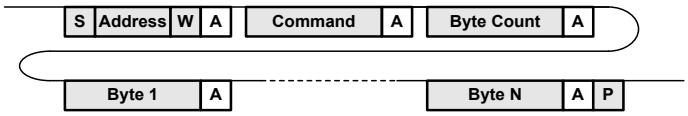
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



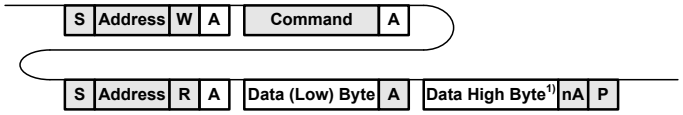
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes.



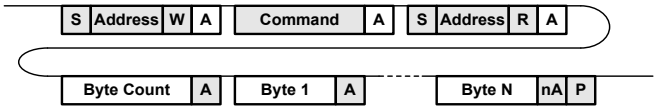
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes.



9.5 POWER SUPPLY BLACK BOX RECORDER

The power supply shall save the latest data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible via the Power Management Bus communication interface with an external source providing power to the 12V main output bus or standby by 12Vsb output bus.
Critical Events to trigger an update to the Event Recorder includes:

- Output OVP
- Output OCP
- Input UV Fault
- Fan fault
- OTP
- Other faults to cause output shutdown.

Refer to BCA.G6202 Power Management Bus Communication Application Note for further information about the Power Management Bus commands to support this function.

9.6 FIRMWARE UPDATE

The power supply shall have the capability to update its firmware via the Power Management Bus interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 12Vstby pins.

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10. TEMPERATURE AND FAN CONTROL

10.1 FAN CONTROL

To achieve the best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the air-flow at the rear of the supply by placing large objects directly at the output connector. The TET3000 series supply has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

Figure 18. Airflow Direction

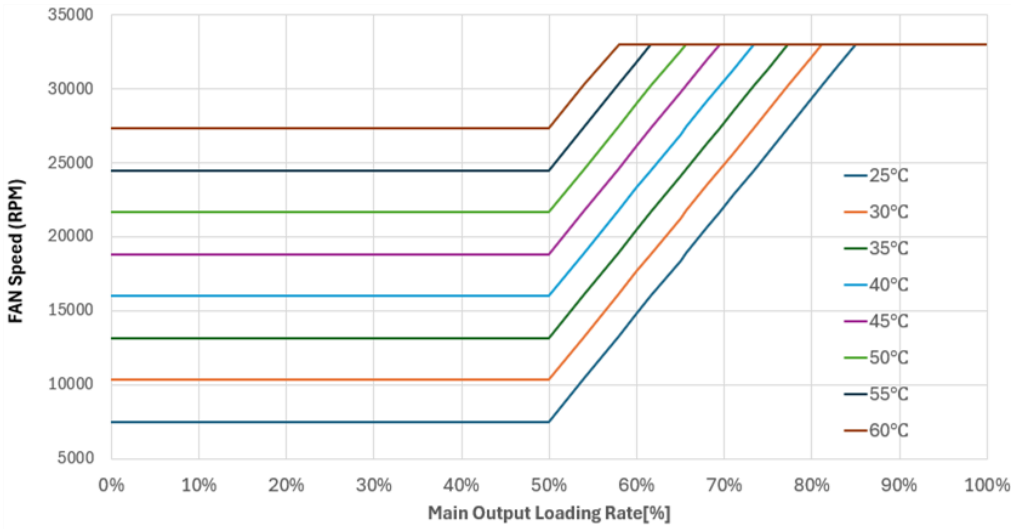

Figure 19. Fan Speed vs. Main Output Load

11. ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, Level 4, ±8 kV	A
ESD Air Discharge	IEC / EN 61000-4-2, Level 4, ±15 kV	A
Radiated Electromagnetics Filed	IEC / EN 61000-4-3, Level 3,10 V/m, 1 kHz/80% Amplitude Modulation, 80MHz - 1000MHz, 1800MHz, 2600MHz, 3500MHz, 5000MHz	A
Burst	IEC / EN 61000-4-4, Level 2, Input DC port ±1 kV	A
Surge	IEC / EN 61000-4-5, Level 2 Line to earth: ±1 kV 2Ω Line to line: ±1 kV 2Ω	A
RF Conducted Immunity	IEC / EN 61000-4-6, Level 3, 10 Vrms, CW,0.15…80MHz	A

11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55032:2015 / CISPR 32:2015: 0.15 … 30 MHz, QP and AVG	Class A
Radiated Emission	EN 55032:2015 / CISPR 32:2015: 30 MHz … 1 GHz, QP	Class A

12. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to UL/CSA 62368-1, IEC/EN 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to the latest edition of the following standards: UL/CSA 62368-1, IEC 62368-1	Approved
Isolation Strength	Input (P/N) to chassis (PE) Input (P/N) to output Output to chassis	Basic Basic Functional
Electrical Strength Test	Input to output Input to chassis Output to chassis	1500 VDC 1500 VDC 500VDC

13. ENVIRONMENTAL

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	$V_{i\,min}$ to $V_{i\,max}$, $I_{1\,nom}$, $I_{SB\,nom}$ at 3000 m	-5		+40	°C
		$V_{i\,min}$ to $V_{i\,max}$, $I_{1\,nom}$, $I_{SB\,nom}$ at 2000 m	-5		+50	°C
T_{Aext}	Extended Temp. Range	Derated output at 2000 m	+50		+65	°C
T_S	Storage Temperature	Non-operational	-40		+70	°C
	Humidity	(Operating) non-condensing	5		95	%
N_a	Audible Noise	$V_{i\,nom}$, 50% $I_{o\,nom}$, T_A = 25°C, measured at bystander position		46		dBA

NOTE: Shock and vibration per IPC9592B.

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14. MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		54.5		mm
	Heigth		40.0		mm
	Depth		321.5		mm
Weight			1.25		kg

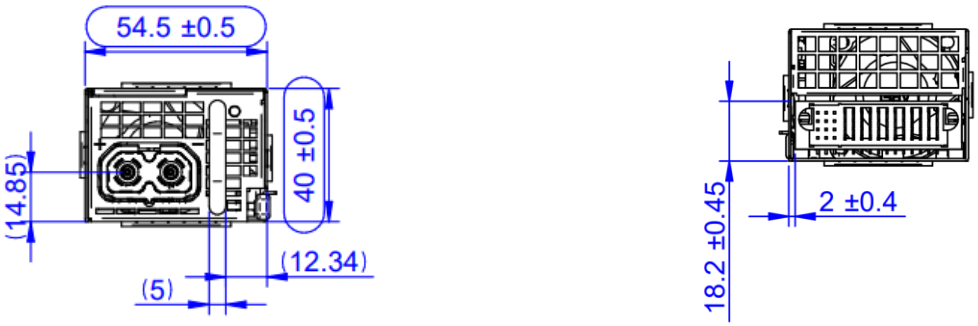

Figure 20. Front and back view

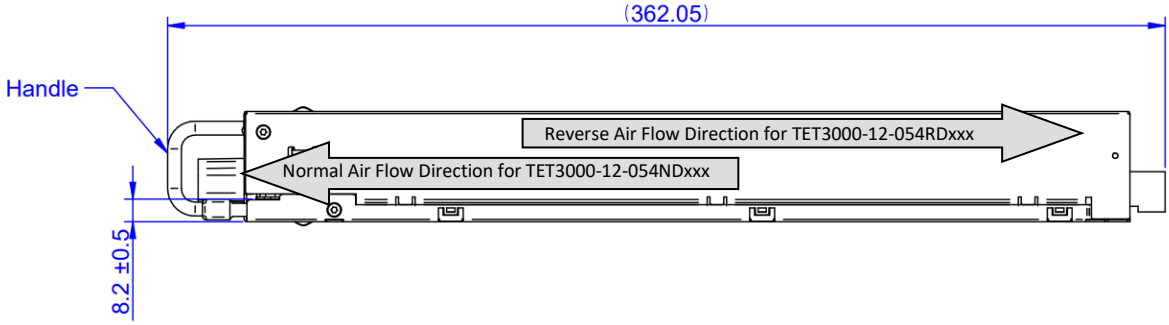

Figure 21. Side view

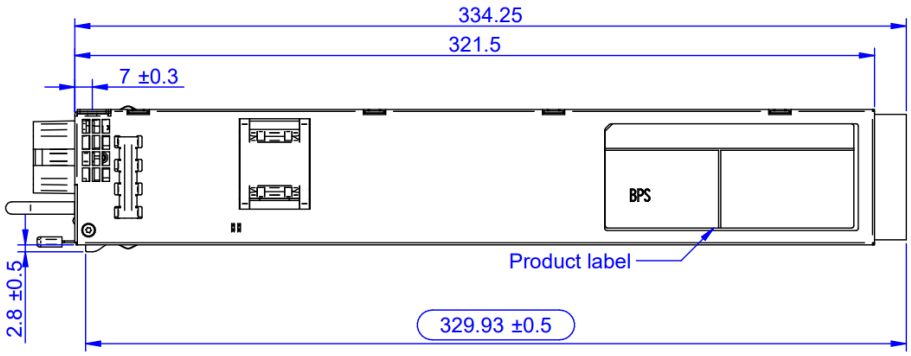

Figure 22. Top view

15. CONNECTORS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Input connector	Amphenol, RADSOK® Receptacle C10-752109-000				
Mating Input connector	Manufacturer : Amphenol Manufacturer P/N : C10-752159-00, Cable suggestion using AWG#4 or equivalent				
Output connector	Amphenol 10106262-6003006LF or equivalent				
Mating output connector	Amphenol 10106264-6003003LF				

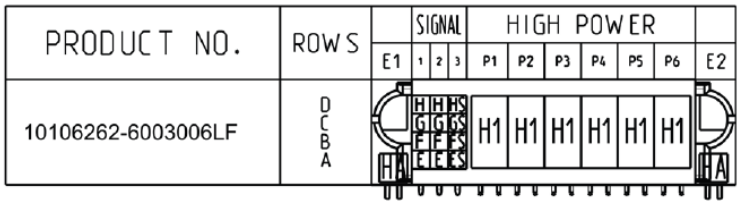

Figure 23. Power supply output connector

OUTPUT PIN ASSIGNMENT

PIN	NAME	DESCRIPTION
P4, P5, P6	V1	+12 VDC main output
P1, P2, P3	V1&VSB_RETURN	+12 VDC / VSB Output Return
A1	PRESENT_L	Power supply present pin: Active-low
B1	VSB	Standby Output
C1	INOK_H	DC input OK signal: Active-high
D1	ISHARE	Current Share Bus
A2	V1_SENSE_R	Main output negative sense
B2	V1_SENSE	Main output positive sense
C2	PWOK_H	Power OK signal output (lagging pin): Active-high
D2	APS	I^2C address (select by a pull-down resistor)
A3	SDA	I^2C data signal line
B3	SCL	I^2C clock signal line
C3	PSON_L	Power supply remote on input: Active-low
D3	SMB_ALERT_L	SMB Alert signal output: Active-low

Table 6. Output connector pin assignment

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16. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	Evaluation Board Connector board to operate TET3000 series supplies. Includes an onboard USB to I2C converter (use I2C Utility as desktop software)	YTM.G5701.0	Bel Power Solutions

17. REVISION HISTORY

DATE	REVISION	SECTION	CHANGES / UPDATES	PREPARED BY	ECO/MCO REFERENCE NO.
2025/1/15	1	/	First draft	GT Zhang	
2025/7/15	A	/	Release specs to A	GT Zhang	

For more information on these products consult: powersupport@belf.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

POWER | PROTECT | CONNECT

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