TEC5200-54-074NA

AC-DC CRPS Front-End Power Supply



TEC5200-54-074NA is a 5200 W Common Redundant Power Supply (CRPS) power supply that converts standard AC mains power or High Voltage DC bus voltages (HVDC) into a main output of 54 VDC for powering systems using distributed power architectures.

The power supply is hot-swappable and supports N+1 redundant architecture. The high-power density helps to improve the overall system efficiency and enhance system reliability. The full digital control facilitates remote set-up, monitoring and control.

TEC5200-54-074NA offers multiple protections including protection.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

RoHS Compliant

Features & Benefits

- Input Voltage Range 180 – 264 VAC / 204 – 300 VDC
- Nominal Output Voltage 54 VDC
- Standby Output 12 V_{SB} (3 A)
- Output Power up to 5200 W
- Dimensions: 265 x 73.5 x 40 mm (10.43 x 2.89 x 1.57 in)
- High Power Density
- Comply with UL/CSA 62368-1, EN/IEC 62368-1
- Supports N+1 Redundancy, Cold Redundancy, Internal ORing
- Black Box Recorder, Bootloader
- Clockwise and Counter-Clockwise Fan Rotation
- Supports Power Management Bus Communication Protocol

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

Please read our datasheet & drawing disclaimer here.

1 ORDERING INFORMATION

TEC	5200	-	54	-	074	N	A		
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**	**Option Code**	**Production Location Code**
TEC Front-End	5200 W		54 V		73.5 mm	N: Normal R: Reverse	A: AC D: DC	Blank: Standard G1S653: Custom	Blank: China (Default) G1: Malaysia (Contact Bel CS team)

2 INPUT

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Input Voltage Ranges*	AC Voltage Range 1 (4600 W); Current 25 A	180	200-220	242	V_{RMS}
	Start-up		174 ± 4		VAC
	Power Off		165 ± 5		VAC
	AC Voltage Range 2 (5000 W); Current 25 A		220-230	253	V_{RMS}
	AC Voltage Range 3 (5200 W); Current 25 A	207	230-240	264	V_{RMS}
	HVDC (4600 W); DC input current 25 A	204	240	300	VDC
	Start-up		195 ± 5		VDC
	Power Off		185 ± 5		VDC
AC Inrush Current	@ 240 VAC / 240 VDC; 5200 W; ½ AC cycle (10 ms)			35	A_{PK}
Input Frequency		47	50/60	63	Hz
Power Factor	230 VAC / 50 & 60 Hz, 10% load	0.92			
	230 VAC / 50 & 60 Hz, 20% load	0.97			
	230 VAC / 50 & 60 Hz, 50% load	0.99			
	230 VAC / 50 & 60 Hz, 100% load	0.99			
Current iTHD (Total Harmonic Distortion)	230 VAC / 50 / 60 Hz, >5% & ≤10%			20	%
	230 VAC / 50 / 60 Hz, >10% & <20%			15	
	230 VAC / 50 / 60 Hz, ≥20%			10	
	230 VAC / 50 / 60 Hz, ≥40%			8	
	230 VAC / 50 / 60 Hz, ≥50%			5	
Efficiency	230 VAC / 60 Hz, 10% load	91			%
	230 VAC / 60 Hz, 20% load	94			%
	230 VAC / 60 Hz, 50% load	96			%
	230 VAC / 60 Hz, 100% load	94			%
Hold-up Time	@ 70% of max. loading	12			ms
$12V_{SB}$ Hold-up Time	@ 100% load	70			ms
AC Line Sag	0 to 1/2 AC cycle (nom AC voltage ranges, 50/60 Hz) No loss of function or performance. (0%-70%load)		95		%
	> 1 AC cycle (nom AC voltage ranges, 50/60 Hz) Loss of function acceptable, self-recoverable	35			%
AC Line Surge	Continuous (nom AC voltage ranges, 50/60 Hz) No loss of function or performance		10		%
	0 to 1/2 AC cycle (mid-point of nom VAC ranges, 50/60 Hz) No loss of function or performance		30		%
AC Line Isolation	Primary to secondary; reinforced insulation (per IEC 62368-1)	3000 4242			VAC VDC

Notes: The Brown IN/OUT Hysteresis min is 5 V.

1. Maximum AC input current shall be measured at every input voltage range MIN rated voltage, at it's max load; (25 Arms)
2. Dc input current maximum while input voltage is 240VDC.at max load;(25 Arms)
3. 180-200 VAC PSU can support 4600 W, 200-207 VAC PSU can support 5000 W;
4. Brown-in/out loading is 80%load.

3 OUTPUT

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Output Voltage	Output voltage adjusted to 54 VDC ± 0.1 VDC @ 50% load at 230 VAC input		+54		VDC
Voltage Regulation Limits	± 3 %	+52.38	+54	+55.62	VDC
Output Power	Continuous			5200	W
Output Current	@ 180 – 200 VAC @ 200 – 207 VAC @ 207 – 264 VAC @ 240 VDC	1.0 1.0 1.0 1.0		85.2 92.6 96.3 85.2	A
Load Regulation	Static Transient		± 3 ± 5		%
Line Regulation			± 1		%
Overshoot / Undershoot			7		%
Transient Load *	Δ Step Load Size:60% of Load Max, Load Slew Rate: 5 A/µs			1000	µF
Capacitive Loading		470		22000	µF
Output Ripple & Noise	20 MHz BW			500	mVpp
+12 V_{SB} OUTPUT					
+12 V_{SB} Output Voltage			+12		V_{SB}
Voltage Regulation	± 5 %	+11.4	+12	+12.6	V
+12 V_{SB} Output Current		0.1		3	A
Load Regulation			± 5		%
Line Regulation			± 1		%
Overshoot / Undershoot			7		%
Transient Load *	Δ Step Load Size = 1 A; Load Slew Rate 0.5 A/µs			1000	µF
Capacitive Loading		100		4700	µF
Output Ripple & Noise	10 Hz to 20 MHz BW			120	mVpp

* For dynamic condition +54 V min loading is 1 A

3.1 EDPP

	Pmax_peak load	Current slope	Peak load duration	System capacitance	Voltage undershoot
EDPP-Patterm1	70 to 156%	2 A/us	5 msec	1000 uF	-7%

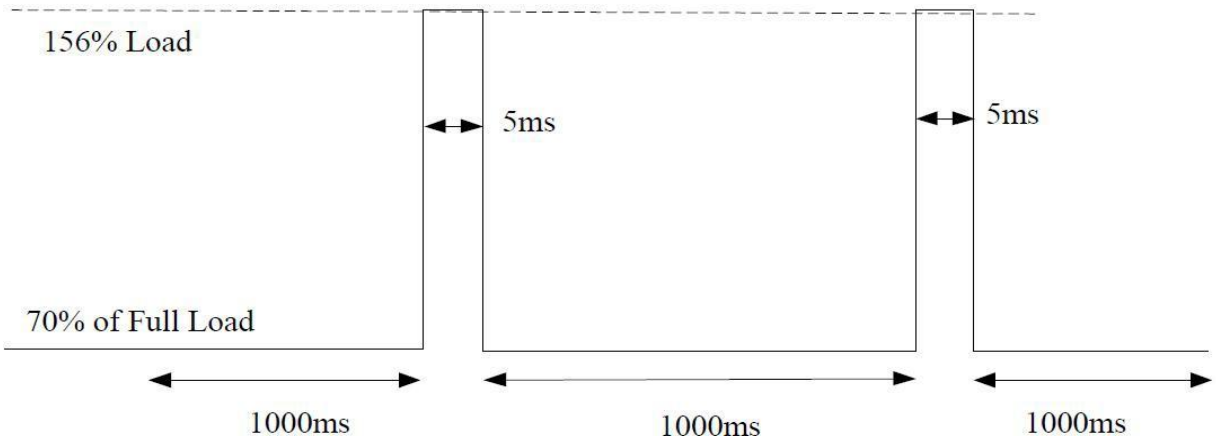

Figure 1. EDPP-Patterm1

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	Pmax_peak load	Current slope	Peak load duration	System capacitance	Voltage undershoot
EDPP-Patterm2	5 to 105%	5 A/us	100 usec Repeat patterm with time=0.1;0.5;1.0;2.5;7.5;10ms	1000 uF	-7%

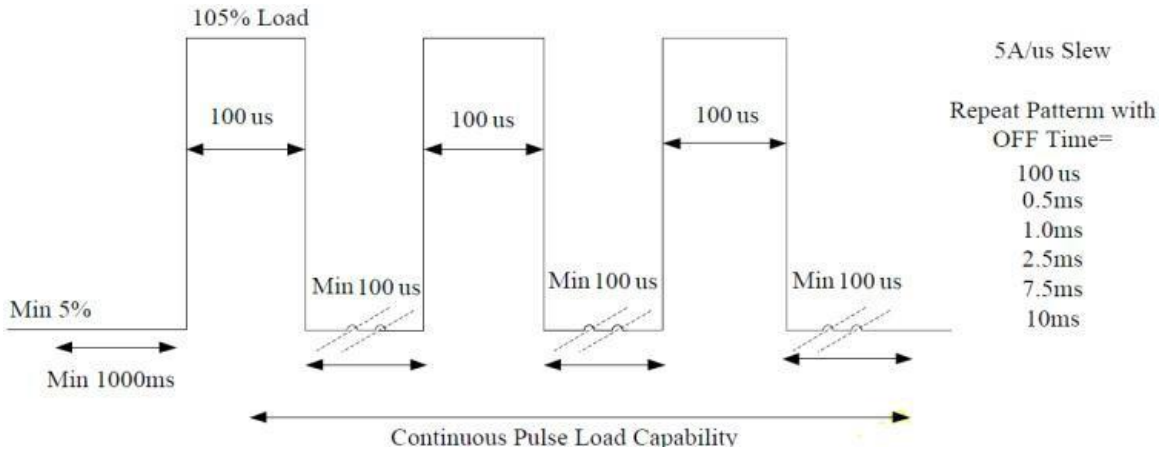

Figure 2. EDPP-Patterm2

	Pmax_peak load	Current slope	Peak load duration	System capacitance	Voltage undershoot
EDPP-Patterm3	5 to 105%	5 A/us	500 usec Repeat patterm with time=0.5;1.0;2.5;7.5;10ms	1000 uF	-7%

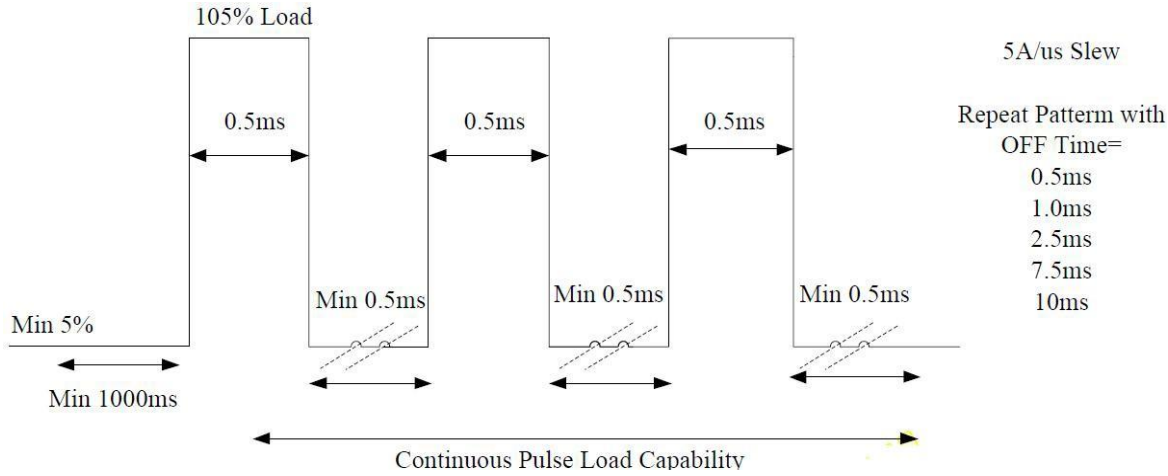

Figure 3. EDPP-Patterm3

	Pmax_peak load	Current slope	Peak load duration	System capacitance	Voltage undershoot
EDPP-Patterm4	5 to 155%	1 A/us	500 usec	1000 uF	-7%
	155 to 135%		5 ms	1000 uF	-7%
	135 to 115%		50 ms	1000 uF	-7%
	115 to 100%		200 ms	1000 uF	-7%

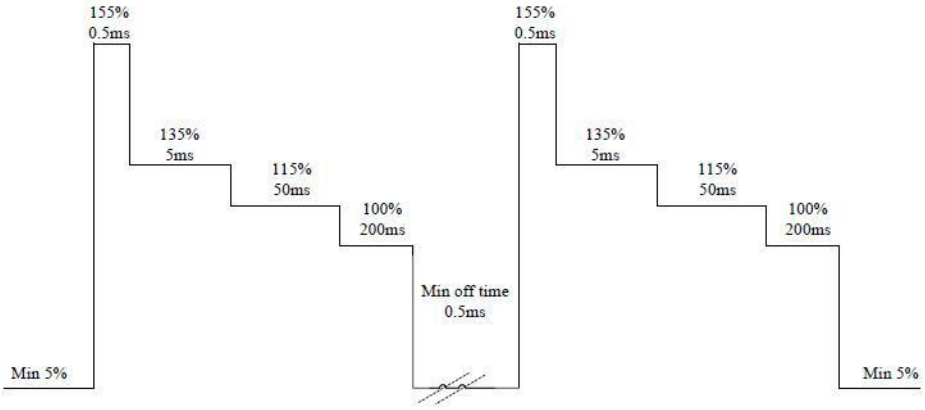

Figure 4. EDPP-Patterm4

3.2 POWER & CURRENT RATINGS

Output	Input voltage (VAC)	Input voltage (VDC)	O/P Min. (A)	Max. Current Rating (A)	20 s Peak Current (A)	260 ms Peak Current (A)	100 ms Peak Current (A)	15 ms Peak Current (A)	100 us Peak Current (A)
54 V	180 – 200	-	1.0	85.2	Rating*115%	Rating*135%	Rating*155%	Rating*165%	Rating*170%
54 V	200 – 207	-	1.0	92.6					
54 V	207 – 264	-	1.0	96.3					
54 V	-	240	1.0	85.2					
12 V_{SB}	-	-	0.1	3.0	-	-	-		-

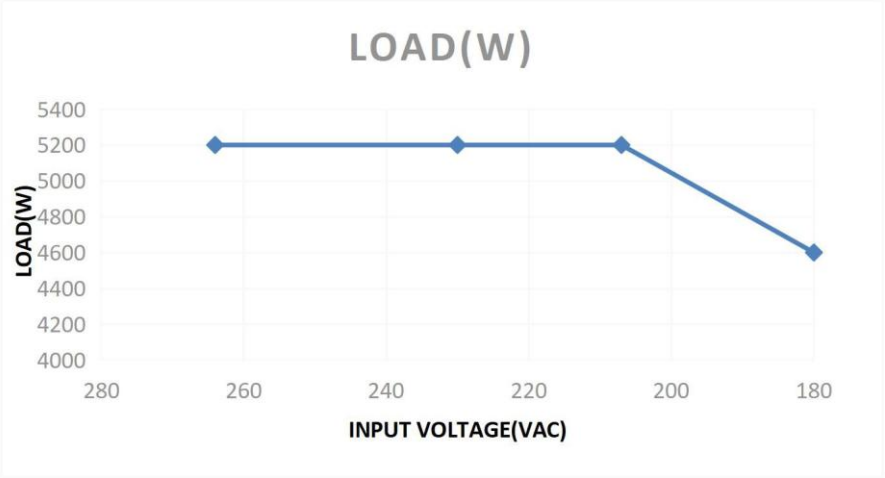

Figure 5. Power Derating Curve

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3.3 AIR FLOW & MAX OUTPUT POWER

High Line 220Vac Max Output power(W) vs Airflow Rate(CFM)				
Airflow (CFM)	Ambient Temperature			
	25°C	35°C	45°C	55°C
3.5	3240	2700	2214	1620
4.8	3888	3348	2808	2268
6.4	4536	3996	3456	2916
7.8	4968	4428	3888	3294
9.2	5200	4860	4320	3726
10.8	5200	5200	4698	4050
12	5200	5200	4968	4320
12.6	5200	5200	5200	5200

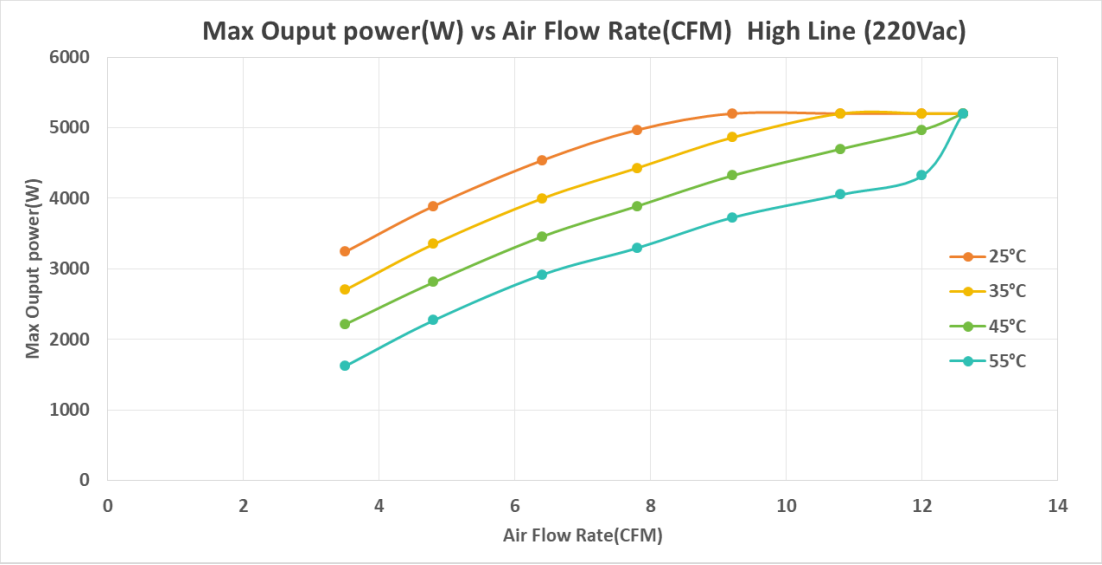

Figure 6. High Line Max Output Power vs Airflow Curve

Low Line 180Vac~200Vac Max Output power(W) vs Airflow Rate(CFM)				
Airflow (CFM)	Ambient Temperature			
	25°C	35°C	45°C	55°C
3.5	2538	2268	1998	1296
4.8	3402	2970	2538	1890
6.4	4050	3672	3186	2592
7.8	4482	4050	3510	2916
9.2	4600	4428	3888	3294
10.8	4600	4600	4212	3618
12	4600	4600	4428	3888
12.6	4600	4600	4600	4600

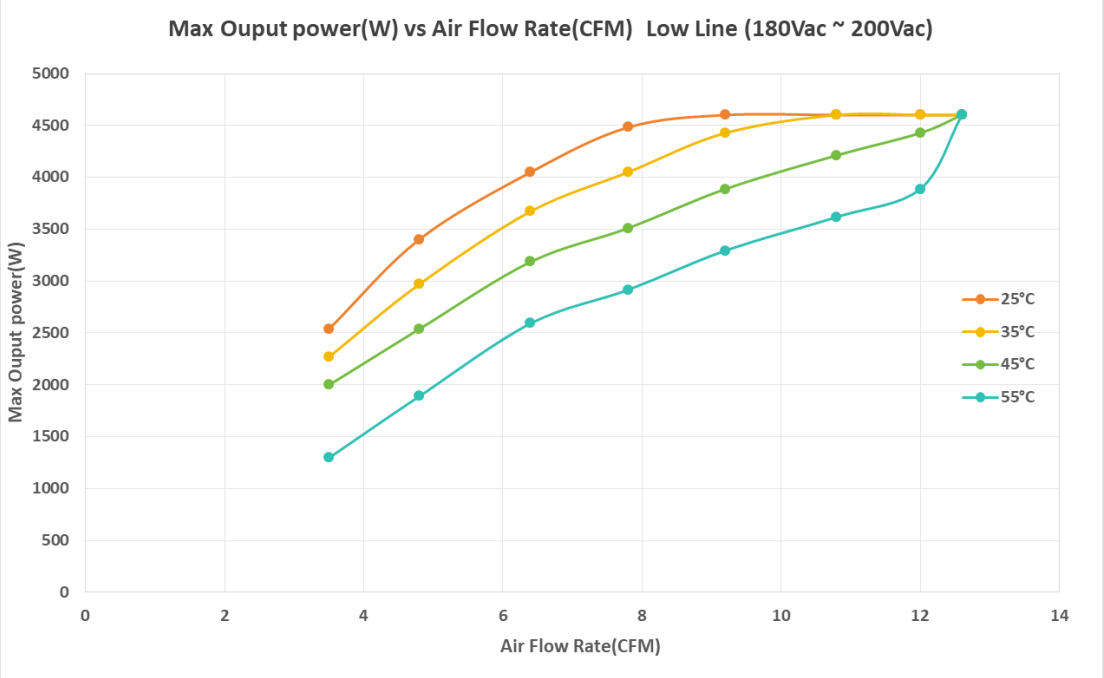

Figure 7. Low Line Max Output Power vs Airflow Curve

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3.4 LOAD SHARING

The +54V output will have active load sharing. The output will share within 3% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap / redundant 1+1 configurations.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
VSHARE; IOUT=Max	Voltage of load share bus at specified maximum output current	7.6	8.0	8.4	V
VSHARE; IOUT=75%Max	Voltage of load share bus at specified 75 % maximum output current	5.7	6.0	6.3	V
VSHARE; IOUT=50%Max	Voltage of load share bus at specified 50 % maximum output current	3.6	4.0	4.4	V
VSHARE; IOUT=25%Max	Voltage of load share bus at specified 25 % maximum output current	1.8	2.0	2.2	V
△VSHARE /△IOUT; IOUT >1A	Slope of load share bus voltage with changing load		8.00		IMAX V/A

The VLs (54V load share bus) pin shall be connected together at user system board for load sharing function of two units. All the remote sense pins of power supplies must to be placed at the same point on +54V and its return path at system side. The 12VSB output is required to actively share current between power supplies (droop control). The 12VSB output of the power supplies are connected in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

PARALLEL MODE	1+N		2+N		3+N	
	54V	12VSB	54V	12VSB	54V	12VSB
Range 1 (180 – 207 VAC) (210 – 300 VDC)	85.2A	3A	166A	5A	250A	5A
Range 2 (208 – 264 VAC)	96.3A	3A	187A	5A	283A	5A
Min. Dynamic	1A	0.1A	2A	0.2A	3A	0.3A
Min. Static	1A	0.1A	2A	0.2A	3A	0.3A
Star up current (Range 1)	85.2A	3A	85.2A	3A	85.2A	3A
Star up current (Range 2)	96.3A	3A	96.3A	3A	96.3A	3A
Max dynamic step current	57.78A	1A	80A	1A	104A	1A

Parallel mode	4+N		5+N		6+N	
	54V	12VSB	54V	12VSB	54V	12VSB
Range 1 (180 – 207 VAC) (210 – 300 VDC)	334A	5A	420A	5A	502A	5A
Range 2 (208 – 264 VAC)	379A	5A	483A	5A	570A	5A
Min. Dynamic	4A	0.4A	5A	0.5A	6A	0.6A
Min. Static	4A	0.4A	5A	0.5A	6A	0.6A
Star up Current (Range 1)	85.2A	3A	85.2A	3A	85.2A	3A
Star up Current (Range 2)	96.3A	3A	96.3A	3A	96.3A	3A
Max dynamic step current	132A	1A	164A	1A	196A	1A

3.5 TIMING REQUIREMENTS

Timing Values for Signal Timing Sequence:

ITEM	DESCRIPTION	MIN	MAX	UNITS
Tvout rise	Output voltage rise time from each main output.	24	250	ms
Toff_latch[2]	This is the time the PSU must stay off when being powered off with loss of AC input. Both outputs must meet this OFF time; 1) whenever PWOK is de-asserted for the 54Vmain output; 2) whenever the 12VSB output drops below regulation limits.	300	1000	ms
T12vsb_rise	Output voltage rise time for the +12VSB output.	15	50	ms
$T_{sb_on\ delay}$	Delay from AC being applied to 12VSB being within regulation.		1500	ms
Tac_on_delay	Delay from AC being applied to all output voltages being within regulation.		3000	ms
$T_{vout\ holdup}$	Time 54V output voltage dropping to 48.6V after loss of AC at 70% of max load condition.	13		ms
$T_{pwok\ holdup}$	Delay from loss of AC to desertion of PWOK at 70% of max load condition.	12		ms
Tpson_off_delay	Delay from PSON# de-asserted to power supply turning off		5	ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
$T_{pson\ pwok}$	Delay from PSON# deactivate to PWOK being deserted.		5	ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
$T_{pwok\ off}$[1]	Delay from PWOK de-asserted to +54V dropping out of regulation limits.	1	6[4]	ms
T_{pwok_low}	Duration of PWOK being in the deserted state during an off/on cycle using AC or the PSON# signal.	100		ms
T_{sb_vout}	Delay from 12 VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
$T_{12VSB\ holdup}$	Time the +12VSB output voltage stays within regulation after loss of AC at 70% of max load.	70		ms
Tvinok_on[3]	Delay from AC being applied to assertion of VINOK		Configurable	ms
Tvinok_off[3]	Time from loss of AC to de-assertion of VINOK		Configurable	ms

Notes:

1. The Tpwok_holdup and Tpwok_off times are the default values in the PSU when it's being energized, however the system now can configure the warning time established by Tpwok_off to have a different value.
2. Toff_latch flow diagram is shown in Figure. 13 Toff_latch flow diagram.
3. Additional logic dependencies are described Figure. 12 VINOK assertion logic as Below.
4. Tpwok_off can be configure from 1ms (default) to a maximum of 6ms.

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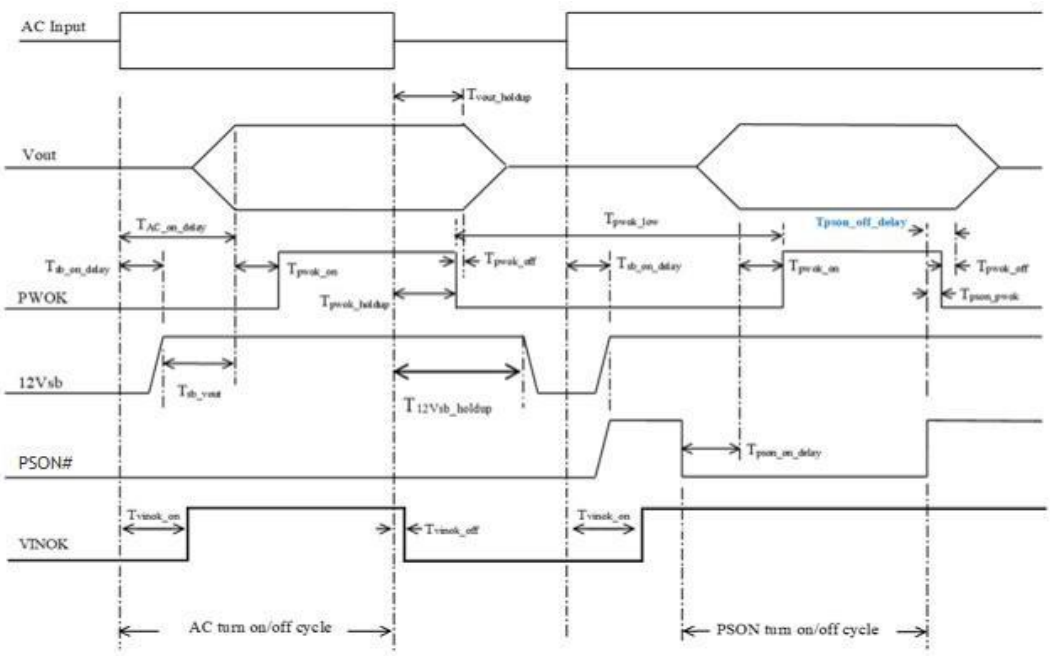

Figure 8. Signal Timing Sequence

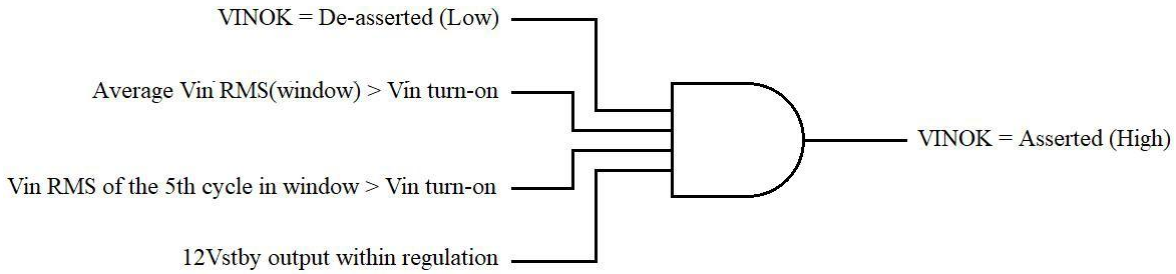

Figure 9. VINOK assertion logic

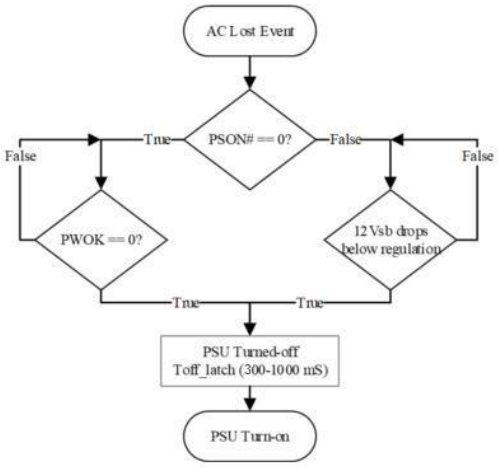

Figure 10. Toff_latch flow diagram

4 PROTECTION

Protection circuits inside the power supply cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

4.1 OVER CURRENT PROTECTION (OCP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shall shutdown. The power supply shall not be damaged from repeated power cycling in this condition. 12Vsb will be auto-recovered after removing OCP limit.

SPEC	DESCRIPTION	MIN	MAX	MIN	MAX
OCW0	Slow over current warning 0(SMBAlert#)	Rating*105%	Rating*109%	30sec	
OCP0	Slow over current protection 0 (shutdown and latch after MIN/MAX timing)	Rating*105%	Rating*109%	31sec	
OCW1	Slow over current warning (SMBAlert#)	Rating*110%	Rating*115%	20sec	
OCP1	Slow over current protection 1 (shutdown and latch after MIN/MAX timing)	Rating*110%	Rating*115%	20sec	
OCW2	Fast over current warning 2 (SMBAlert#)	Rating*116%	Rating*155%	60msec	100msec
OCP2	Fast over current protection 2 (shutdown, latch)	Rating*116%	Rating*135%	260msec	300msec
OCP3	Fast over current protection 3 (shutdown, latch)	Rating*136%	Rating*155%	100msec	120msec
OCW3	Fast over current warning 3 (SMBAlert#)	Rating*156%	Rating*165%	10msec	14msec
OCP4	Fast over current protection 4 (shutdown, latch)	Rating*156%	Rating*165%	15msec	22msec
OCP5	Fast over current protection 5 (shutdown, latch)	Rating*166%		100usec	
12Vsb OCP	12Vsb over current protection (shutdown, hiccup mode)	3.8A	4.8A	1msec	100msec

4.2 OVER VOLTAGE PROTECTION (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and then retry third time before latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Over Voltage Protection (OVP)	+54 V Output	58.5		61.5	V
	+12 V_{SB} Output	13.5		15.0	V

4.3 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 3 °C of ambient temperature hysteresis.

SENSOR	SHUTDOWN (℃)	WARNING (℃)	RECOVER (℃)
Ambient(RT600)	65	NA	57
PFC(RT3)	124	120	80
SR(RT1)	122	118	85

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4.4 SHORT CIRCUIT PROTECTION (SCP)

A short circuit is considered to be resistance of 100 mΩ or less, applied to any output during start-up or while running will not cause any damage to the power supply (connectors, components, PCB traces, etc.). The power supply shuts down and latches off for short on main outputs but recovers upon PS_ON toggled or AC re-applied.

4.5 CLOSED LOOP SYSTEM THROTTLING (CLST)

The power supply will always assert the SMBAlert# signal whenever temperature-monitored component in the power supply reaches a warning threshold. Upon reduction of the load within 2msec after the SMBAlert# signal is asserted if the load is reduced to less than the power supply rating; the power supply will continue to operate and not shutdown.

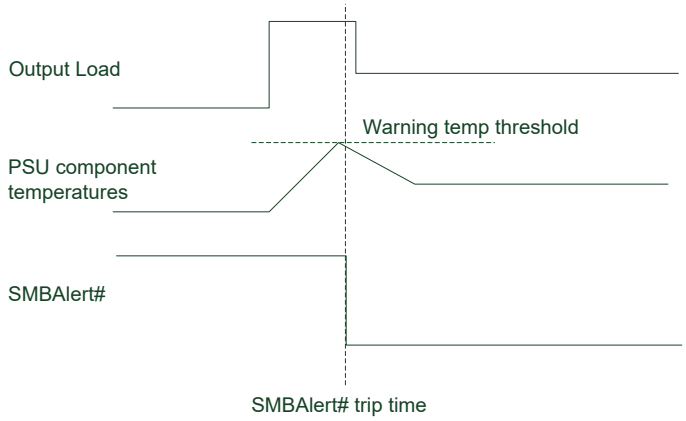

Figure 11. CLST Timing Requirements

4.6 SMART RIDE-THROUGH (SmaRT)

The power supply will assert the SMBAlert# signal < 4 ms after AC input voltage is lost to 0 VAC.

5 CONTROL

The following sections define the input and output signals from the power supply. Signals that can be defined as low true use the following convention: Signal# = low true

5.1 DEVICE ADDRESS LOCATION (A0; A1)

This signal is defined by end user system for Power Management Bus communication, to allocate address of power supply unit in particular slot location. This signal has a 10 kΩ internal resistor to internal 3.3 V located in power supply

SIGNAL TYPE	PULL-UP TO INTERNAL 3.3 V LOCATED IN POWER SUPPLY	
Adress_A0/A1 = high	Address 1	
Adress_A0/A1 = low	Address 0	
	MIN	MAX
Logical Level Low	0 V	0.4 V
Logical Level High	2.0 V	3.46 V

5.2 I2C BUS (SCL; SDA)

Each module shall provide SCL/SDA bus for EEPROM read/write of system. It's pull up from +3.3 Vdd device by a 10 kΩ resistor. SCL/SDA pin should be link together and closer. The SCL/SDA bus total capacitance must lower 100 pF from system and PDB. The max I2C bus speed is 400 kHz and the mcu of PSU is slave device in I2C bus. The time interval of I2C command is 1ms.

5.3 SMBAlert#

This is an active low signal and indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold or protection, output over-current warning and protection, Input under-voltage warning & protection. Ambient over temperature protection shall not activate this signal.

SIGNAL TYPE	OPEN COLLECTOR / DRAIN OUTPUT FROM POWER SUPPLY. PULL-UP TO 3.3 V_{SB} LOCATED IN SYSTEM.	
SMBAlert# = High	OK	
SMBAlert# = Low	Power Alert to system	
	MIN	MAX
Logic level low voltage	0 V	0.4 V
Logic level high voltage	2.0 V	3.46 V
Sink current, Alert# = low		4 mA
Source current, Alert# = high		50 µA

5.4 PSON#

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +54V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off.

The power supply shall provide an internal pull-up resistor to high. The power supply shall also provide de-bounce circuitry on PSON# to prevent it from oscillating On/Off at startup when activated by mechanical switch.

Provisions for de-bouncing will be included in the PSON# circuitry to prevent the power supply from oscillating on/off at startup..

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SIGNAL TYPE	ACCEPTS AN OPEN COLLECTOR/DRAIN INPUT FROM THE SYSTEM. PULL-UP TO INTERNAL VCC LOCATED IN POWER SUPPLY	
PSON# = Low	PSU ON	
PSON# = Open or High	PSU OFF	
	MIN	MAX
Logic level low (PSU ON)	0 V	1 V
Logic level high (PSU OFF)	2.0 V	3.46 V
Source current, $V_{PSON\#}$ = low		4 mA
Power up delay: $T_{PSON\#_ON_DELAY}$	5 ms	400 ms
Power off delay: $T_{PSON\#_PWOK}$		5 ms

5.5 PWOK

This signal should be asserted high by the power supply to indicate that all outputs are within the regulation thresholds listed in section 4.1. Conversely, this signal should be de-asserted to a low state when any of the DC outputs voltage falls below its under voltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation can't be guaranteed.

This signal must be driven low at least 1ms before any of the outputs go out of regulation. Also, that will be defined and selected for inclusion from any variation of the following three items:

A.) AC Power Loss
B.) Fan Failure
C.) Over Temperature

This signal will have an internal pull-up resistor to internal 3.3 V sources.

SIGNAL TYPE	OPEN COLLECTOR/DRAIN OUTPUT FROM POWER SUPPLY. PULL-UP TO VSB LOCATED IN THE POWER SUPPLY.	
PWOK or P_Good = High	DC Outputs O.K.	
PWOK or P_Good = Low	DC Outputs N.G.	
	MIN	MAX
Logical Level Low, I_{SINK} = 400 µA	0 V	0.4 V
Logical Level High, I_{SOURCE} = 200 µA	2.4 V	3.46 V
Sink current, PWOK = low		400 µA
Source current, PWOK = high		2 mA
PWOK delay: T_{PWOK_ON}	100 ms	500 ms
Power down delay: T_{PWOK_OFF}	1 ms	
PWOK or P_Good Rise & Fall Time		100 µs
Any PSU fault to PWOK deasertion delay		100 µs
Ripple noise (Power on & continent)		400 mV

5.6 COLD REDUNDANCY

This signal should be connected together at system board for cold redundant function (enable by system). Please refer to the Power Management Bus specification for detail.

5.7 VINOK SIGNAL

VINOK signal indicates that the input voltage is within the range where the power supply can operate normally. Details of the operation are described in Timing Requirements section.

SIGNAL TYPE (ACTIVE HIGH)	OPEN COLLECTOR/DRAIN OUTPUT FROM POWER SUPPLY. 3KΩ PULL-UP TO 3.3V LOCATED IN THE POWER SUPPLY.	
VINOK = High	Input voltage is within the operational range	
VINOK = Low	Input voltage not within the operational range	
	MIN	MAX
Logic level low voltage, Isink=10mA	0V	0.4V
Logic level high voltage, Isource=4mA	3.0V	3.46V
Sink current, VINOK = low		10 mA
Source current, VINOK = high		4mA
VINOK rise and fall time		100 us

Note: *Using 100KΩ load resistor in the system side.*

5.8 PRESENT#

This signal is an active low type signal and is connected to the power supply's output ground internally. The mating pin of this signal in system side should have a pull-up resistor which limit the max. current 4 mA to go through from this signal pin to the power supply. A Low state on this signal indicates the PSU is physically presents.

5.9 RETURN REMOTE SENSE

The power supply has return remote sense to regulate out ground drops in the system for the main output voltage. The return remote sense is able to regulate out a maximum of 300 mV of drop on the ground output.

5.10 +54 V REMOTE SENSE

The power supply uses +54V remote sense to regulate out +54V drops in the system for the main output voltage. The +54V remote sense is able to regulate out a maximum of 300mV of drop on the +54V output.

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6 FRU REQUIREMENTS

6.1 FRU DATA

The FRU data format shall be compliant with the IPMI ver.1.0 (per rev.1.1 from Sept.25, 1999) specification. The following is the exact listing of the EEPROM content. During testing this listing shall be followed and verified.

6.2 FRU DEVICE PROTOCOL

The FRU device will implement the same protocols, including the Byte Read, Sequential Read, Byte Write, and Page Read protocols.

Four pins will be allocated for the FRU information on the Power Supply connector. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Two pins are for address lines to indicate to the power supply's EEPROM which position the power supply is located in the system. The SCL and SDA signals are pulled up by system, the address lines are also pulled up by system.

ADDRESSES USED:	X	X	X	X
System addressing Address 1 / Address 0	0/0	0/1	1/0	1/1
PMBus device read / write addresses	B0h/B1h	B2h/B3h	B4h/B5h	B6h/B7h
FRU device read/write addresses	A0h/A1h	A2h/A3h	A4h/A5h	A6h/A7h

ITEM	01	BYTE VALUE		DESCRIPTION	BLOCK TITLE
		DEC	HEX		
1	0000H	1	01	COMMON HEADER FORMAT VERSION	COMMON HEADER
2	0001H	0	00	INTERNAL USE AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present	
3	0002H	0	00	CHASSIS INFO AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present.	
4	0003H	0	00	BOARD AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present.	
5	0004H	1	01	PRODUCT INFO AREA STARTING OFFSET (In Multiples Of 8 Bytes).	
6	0005H	11	0B	MULTIRECORD AREA STARTING OFFSET (In Multiples Of 8 Bytes).	
7	0006H	0	00	PAD, Write As 00H	
8	0007H	243	F3	COMMON HEADER CHECKSUM (ZERO CHECKSUM)	
1	0008H	1	01	PRODUCT AREA FORMAT VERSION 7:4 - Reserved, Write As 0000B 3:0 - Format Version Number = 1H	PRODUCT INFORMATION AREA
2	0009H	10	0A	PRODUCT AREA LENGTH (In multiples of 8 bytes)	
3	000AH	25	19	LANGUAGE CODE (ENGLISH)Z	
4	000BH	200	C8	MANUFACTURER NAME TYPE / LENGTH (C8H) 7:6 - Type Code 5:0 - Number Of Data Bytes.	
5	000CH	98	62	b	
6	000DH	101	65	e	
7	000EH	108	6C	l	
8	000FH	32	20		
9	0010H	32	20		
10	0011H	32	20		
11	0012H	32	20		
12	0013H	32	20		
13	0014H	208	D0	PRODUCT NAME Type/Length (D0h) 7:6 – Type Code	MANUFACTURER'S MODEL NUMBER

				5:0 - Number Of Data Bytes.	
14	0015H	84	54	T	
15	0016H	69	45	E	
16	0017H	67	43	C	
17	0018H	50	35	5	
18	0019H	48	32	2	
19	001AH	48	30	0	
20	001BH	48	30	0	
21	001CH	45	2D	-	
22	001DH	49	35	5	
23	001EH	50	34	4	
24	001FH	45	2D	-	
25	0020H	48	30	0	
26	0021H	55	37	7	
27	0022H	52	34	4	
28	0023H	78	4E	N	
29	0024H	65	41	A	
30	0025H	212	D4	PRODUCT PART/MODEL NUMBER Type/Length (D4h)	CUSTOMER PART NUMBER
31	0026H	71	47	G	
32	0027H	78	4E	N	
33	0028H	48	30	0	
34	0029H	65	41	A	
35	002AH	32	20	5	
36	002BH	32	20	2	
37	002CH	32	20	0	
38	002DH	32	20	0	
39	002EH	32	20	-	
40	002FH	32	20	A	
41	0030H	32	20	H	
42	0031H	32	20		
43	0032H	32	20		
44	0033H	32	20		
45	0034H	32	20		
46	0035H	32	20		
47	0036H	32	20		
48	0037H	32	20		
49	0038H	32	20		
50	0039H	32	20		
51	003AH	195	C3	PRODUCT VERSION NUMBER Type/Length (C3h)	CUSTOMER CURRENT REVISION
52	003BH	86	56	V	To be updated
53	003CH	48	30	0	To be updated
54	003DH	48	30	0	To be updated
55	003EH	211	D3	PRODUCT SERIAL NUMBER type/length byte (D3)	
56	003FH	84	54	T	To be updated
57	0040H	69	45	E	To be updated
58	0041H	67	43	C	To be updated
59	0042H	53	35	5	To be updated
60	0043H	50	32	2	To be updated
61	0044H	50	32	2	To be updated
62	0045H	78	4E	N	To be updated
63	0046H	65	41	A	To be updated
64	0047H	53	35	5	To be updated

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65	0048H	52	34	4	To be updated
66	0049H	89	59	Y	To be updated
67	004AH	89	59	Y	To be updated
68	004BH	77	4D	M	To be updated
69	004CH	77	4D	M	To be updated
70	004DH	88	58	X	To be updated
71	004EH	88	58	X	To be updated
72	004FH	88	58	X	To be updated
73	0050H	88	58	X	To be updated
74	0051H	88	58	X	To be updated
75	0052H	192	C0	FRU FILE ID Type/Length Byte	Not used, code is zero length byte
76	0053H	192	C0	FRU FILE ID Type/Length Byte	Not required
77	0054H	193	C1	ENCODED TO INDICATE NO MORE INFO FIELDS	
78	0055H	0	00	PAD (Always Zero)	
79	0056H	0	00	PAD (Always Zero)	
80	0057H	9	09	CHECKSUM(100H-(LOWER BYTE(SUM OF BYTES)))	To be updated
1	0058H	0	00	RECORD TYPE ID 0x00 =POWER SUPPLY INFORMATION	MULTI RECORD AREA
2	0059H	2	02	7:7 END OF LIST ,6:4=000B, 3:0 RECORD FORMAT VERSION=2	
3	005AH	24	18	RECORD LENGTH OF MULTIRECORD	
4	005BH	225	E1	RECORD CHECKSUM (ZERO CHECKSUM)	
5	005CH	5	05	HEADER CHECKSUM (ZERO CHECKSUM)	
1	005DH	80	50	15-12:RESERVED,WRITE AS 0000B	5200W
2	005EH	20	14	11-0:OVERALL CAPACITY(WATTS)	
3	005FH	92	5C	PEAK VALUE	5980W
4	0060H	23	17	LSB FIRST	
5	0061H	35	23	INRUSH CURRENT ,FFH IF NOT SPECIFIED	35A
6	0062H	10	0A	INRUSH INTERVAL IN MS.	10mS
7	0063H	80	50	LOW END INPUT VOLTAGE RANGE 1 180V=4650H	180V
8	0064H	70	46		
9	0065H	220	DC	HIGH END INPUT VOLTAGE RANGE 1 207V=50DCH	207V
10	0066H	80	50		
11	0067H	220	DC	LOW END INPUT VOLTAGE RANGE 2 207V=50DCH	207V
12	0068H	80	50		
13	0069H	32	20	HIGH END INPUT VOLTAGE RANGE 2 264V=6720H	264V
14	006AH	103	67		
15	006BH	50	32	LOW END INPUT FREQUENCY RANGE 50HZ=32H	50Hz
16	006CH	60	3C	HIGH END INPUT FREQUENCY RANGE 60HZ=3CH	60Hz
17	006DH	12	0C	A/C DROPOUT TOLERANCE IN mS 12mS=0CH	12mS
18	006EH	30	1E	7-5:RESERVED,WRITE AS 000B 4:TACHOMETER PULSES PER POTATION/PREDICTIVE FALL POLARITY YES=1(FAIL=1,PASS=0) 3:HOT SWAP/REDUNDANCY SUPPORT YES=1 2:AUTOSWITCH YES=1 1:POWER FACTOR CORRECTION YES=1 0:PREDICTIVE FALL SUPPLY YES=1	
19	006FH	255	FF	PEAK WATTAGE 15-12:HOLD UP TIME IN SECONDS 1S=1H	
20	0070H	255	FF	11-0 PEAK CAPACITY (WATTS)(LSB FIRST)	15S
21	0071H	0	00	COMMBINED WATTAGE 7-4:Voltage 1 3-0:Voltage 2=00H	
22	0072H	0	00	BYTE 2:3 TOTAL COMBINED WATTAGE (LSB	0

				FIRST) W=0000H	
23	0073H	0	00	BYTE 2:3 TOTAL COMBINED WATTAGE (LSB FIRST) W=0000H	
24	0074H	16	10	PREDICTIVE FAIL TACHOMETER LOWER THRESHOLD(PRM/60)1000/60=16	
1	0075H	9	09	RECORD TYPE ID 0X01 =DC OUTPUT Record	MULTIRECORD
2	0076H	2	02	7:7 END OF LIST 6:4=000 3:0 RECORD FORMAT VERSION=2	HEADER
3	0077H	13	0D	RECORD LENGTH OF MULTIRECORD	
4	0078H	93	5D	RECORD CHECKSUM	
5	0079H	139	8B	HEADER CHECKSUM	
1	007AH	1	01	+12V 7:STANDBY=0,6-4:RESERVED 000B , 3-0:OUTPUT UMBER=0001B	+54V
2	007BH	24	18	NOMINAL VOLTAGE(10mV)5400=1518H	54.0V
3	007CH	21	15		
4	007DH	118	76	MAXIMUM NEGATIVE VOLTAGE DEVIATION(10mV) 5238=1476H	52.38V
5	007EH	20	14		
6	007FH	186	BA	MAXIMUM POSITIVE VOLTAGE DEVIATION(10mV) 5562=15BAH	55.62V
7	0080H	21	15		
8	0081H	244	F4	RIPPLE AND NOISE PK-PK 10Hz TO 20MHz(mV) 500mV=01F4H	500mV
9	0082H	1	01		
10	0083H	100	64	MINIMUM CURRENT DRAW(10mA)	1.0A
11	0084H	0	00		
12	0085H	158	9E	MAXIMUM CURRENT DRAW(10mA)	96.3A
13	0086H	37	25		
1	0087H	1	01	RECORD TYPE ID 0X01 =DC OUTPUT Record	MULTIRECORD
2	0088H	130	82	7:7 END OF LIST 6:4=000 3:0 RECORD FORMAT VERSION=2	HEADER
3	0089H	13	0D	RECORD LENGTH OF MULTIRECORD	
4	008AH	195	C3	RECORD CHECKSUM	
5	008BH	173	AD	HEADER CHECKSUM	
1	008CH	130	82	+12vSB 7:STANDBY=1,6-4:RESERVED 000B , 3-0:OUTPUT UMBER=0010B	+12VSB
2	008DH	176	B0	NOMINAL VOLTAGE(10mV)1200=04B0H	12.0V
3	008EH	4	04		
4	008FH	116	74	MAXIMUM NEGATIVE VOLTAGE DEVIATION(10mV)	11.40V
5	0090H	4	04		
6	0091H	236	EC	MAXIMUM POSITIVE VOLTAGE DEVIATION(10mV)	12.60V
7	0092H	4	04		
8	0093H	120	78	RIPPLE AND NOISE PK-PK 10Hz TO 20MHz(mV) 120mV=0078H	120mV
9	0094H	0	00		
10	0095H	100	64	MINIMUM CURRENT DRAW(mA) 100mA=0064H	0.1A
11	0096H	0	00		
12	0097H	184	B8	MAXIMUM CURRENT DRAW(mA) 3000mA=0BB8H	3A
13	0098H	11	0B		
1	0099H	0	00	Unused Area	
2	009AH	0	00	Unused Area	
3	009BH	0	00	Unused Area	
4	009CH	0	00	Unused Area	
5	009DH	0	00	Unused Area	
6	009EH	0	00	Unused Area	
7	009FH	0	00	Unused Area	

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8	00A0H	0	00	Unused Area	
9	00A1H	0	00	Unused Area	
10	00A2H	0	00	Unused Area	
11	00A3H	0	00	Unused Area	
12	00A4H	0	00	Unused Area	
13	00A5H	0	00	Unused Area	
14	00A6H	0	00	Unused Area	
15	00A7H	0	00	Unused Area	
16	00A8H	0	00	Unused Area	
17	00A9H	0	00	Unused Area	
18	00AAH	0	00	Unused Area	
19	00ABH	0	00	Unused Area	
20	00ACH	0	00	Unused Area	
21	00ADH	0	00	Unused Area	
22	00AEH	0	00	Unused Area	
23	00AFH	0	00	Unused Area	
24	00B0H	0	00	Unused Area	
25	00B1H	0	00	Unused Area	
26	00B2H	0	00	Unused Area	
27	00B3H	0	00	Unused Area	
28	00B4H	0	00	Unused Area	
29	00B5H	0	00	Unused Area	
30	00B6H	0	00	Unused Area	
31	00B7H	0	00	Unused Area	
32	00B8H	0	00	Unused Area	
33	00B9H	0	00	Unused Area	
34	00BAH	0	00	Unused Area	
35	00BBH	0	00	Unused Area	
36	00BCH	0	00	Unused Area	
37	00BDH	0	00	Unused Area	
38	00BEH	0	00	Unused Area	
39	00BFH	0	00	Unused Area	
40	00C0H	0	00	Unused Area	
41	00C1H	0	00	Unused Area	
42	00C2H	0	00	Unused Area	
43	00C3H	0	00	Unused Area	
44	00C4H	0	00	Unused Area	
45	00C5H	0	00	Unused Area	
46	00C6H	0	00	Unused Area	
47	00C7H	0	00	Unused Area	
48	00C8H	0	00	Unused Area	
49	00C9H	0	00	Unused Area	
50	00CAH	0	00	Unused Area	
51	00CBH	0	00	Unused Area	
52	00CCH	0	00	Unused Area	
53	00CDH	0	00	Unused Area	
54	00CEH	0	00	Unused Area	
55	00CFH	0	00	Unused Area	
56	00D0H	0	00	Unused Area	
57	00D1H	0	00	Unused Area	
58	00D2H	0	00	Unused Area	

59	00D3H	0	00	Unused Area	
60	00D4H	0	00	Unused Area	
61	00D5H	0	00	Unused Area	
62	00D6H	0	00	Unused Area	
63	00D7H	0	00	Unused Area	
64	00D8H	0	00	Unused Area	
65	00D9H	0	00	Unused Area	
66	00DAH	0	00	Unused Area	
67	00DBH	0	00	Unused Area	
68	00DCH	0	00	Unused Area	
69	00DDH	0	00	Unused Area	
70	00DEH	0	00	Unused Area	
71	00DFH	0	00	Unused Area	
72	00E0H	0	00	Unused Area	
73	00E1H	0	00	Unused Area	
74	00E2H	0	00	Unused Area	
75	00E3H	0	00	Unused Area	
76	00E4H	0	00	Unused Area	
77	00E5H	0	00	Unused Area	
78	00E6H	0	00	Unused Area	
79	00E7H	0	00	Unused Area	
80	00E8H	0	00	Unused Area	
81	00E9H	0	00	Unused Area	
82	00EAH	0	00	Unused Area	
83	00EBH	0	00	Unused Area	
84	00ECH	0	00	Unused Area	
85	00EDH	0	00	Unused Area	
86	00EEH	0	00	Unused Area	
87	00EFH	0	00	Unused Area	
88	00F0H	0	00	Unused Area	
89	00F1H	0	00	Unused Area	
90	00F2H	0	00	Unused Area	
91	00F3H	0	00	Unused Area	
92	00F4H	0	00	Unused Area	
93	00F5H	0	00	Unused Area	
94	00F6H	0	00	Unused Area	
95	00F7H	0	00	Unused Area	
96	00F8H	0	00	Unused Area	
97	00F9H	0	00	Unused Area	
98	00FAH	0	00	Unused Area	
99	00FBH	0	00	Unused Area	
100	00FCH	0	00	Unused Area	
101	00FDH	0	00	Unused Area	
102	00FEH	0	00	Unused Area	
103	00FFH	0	00	Unused Area	

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Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	01	00	00	00	01	0B	00	F3	01	0A	19	C8	62	65	6C	20
10	20	20	20	20	D0	54	45	43	35	32	30	30	2D	35	34	2D
20	30	37	34	4E	41	D4	47	4E	30	41	20	20	20	20	20	20
30	20	20	20	20	20	20	20	20	20	20	C3	56	30	30	D3	54
40	45	43	35	32	32	4E	41	35	34	59	59	4D	4D	58	58	58
50	58	58	C0	C0	C1	00	00	09	00	02	18	E1	05	50	14	5C
60	17	23	0A	50	46	DC	50	DC	50	20	67	32	3C	0C	1E	FF
70	FF	00	00	00	10	09	02	0D	5D	8B	01	18	15	76	14	BA
80	15	F4	01	64	00	9E	25	01	82	0D	C3	AD	82	B0	04	74
90	04	EC	04	78	00	64	00	B8	0B	00	00	00	00	00	00	00
A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Hex Information

7 POWER MANAGEMENT BUS

Refer to the Power Management Bus application profile for systems for requirements.
Note. Power Management Bus signal should be pull up to 3.3 V only inside PSU.

7.1 POWER MANAGEMENT BUS COMMAND SET

The following table shows mandatory Power Management Bus commands to be supported by the PSU.

COMMAND CODE	COMMAND NAME	SMBUS TRANSACTION TYPE:		NUMBER OF DATA BYTES	COMMENT
		WRITNG DATA	READING DATA		
00h	PAGE	Write Byte	Read Byte	1	
01h	OPERATION	Write Byte	Read Byte	1	0x80 ON; 0x00 OFF Default: 0x00
02h	ON_OFF_CONFIG	Write Byte	Read Byte	1	
03h	CLEAR_FAULTS	Send Byte	N/A	0	
05h	PAGE_PLUS_WRITE	Block Write	N/A	Variable	
06h	PAGE_PLUS_READ	N/A	Block Write – Block Read	Variable	
19h	CAPABILITY	N/A	Read Byte	1	0xB0
1Ah	QUERY	N/A	Block Write – Block Read	1	
1Bh	SMBALERT_MASK	Write Word	Block Write – Block Read	2	
20h	VOUT_MODE		Read Byte	1	0x17 (n=-9)
21h	VOUT_COMMAND	Write Word	Read Word	2	

30h	COEFFICIENTS	N/A	Block Write – Block Read	5	Use for Ein/Eout
31h	POUT_MAX	N/A	Read Word	2	
3Ah	FAN_CONFIG_1_2	Write Byte	Read Byte	1	Default is RPM
3Bh	FAN_COMMAND_1	Write Word	Read Word	2	
4Ah	IOUT_OC_WARN_LIMIT		Read Word	2	
51h	OT_WARN_LIMIT		Read Word	2	
5Dh	IIN_OC_WARN_LIMIT		Read Word	2	
6Ah	POUT_OP_WARN_LIMIT		Read Word	2	
6Bh	PIN_OP_WARN_LIMIT		Read Word	2	
78h	STATUS_BYTE		Read Byte	1	
Bit 6	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC				
Bit 3	VIN_UV				
Bit 2	TEMPERATURE				
Bit 1	CML				
Bit 0	NON OF THE ABOVE				
79h	STATUS_WORD		Read Word	2	
Bit 7(H)	VOUT				
Bit 6	IOUT/POUT				
Bit 5	INPUT				
Bit 3	POWER_GOOD#				
Bit 2	FANS				
Bit 6(L)	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC_FAULT				
Bit 3	VIN_UV_FAULT				
Bit 2	TEMPERATURE				
Bit 1	CML				
Bit 0	NON OF THE ABOVE				
7Ah	STATUS_VOUT		Read Byte	1	
Bit 7	VOUT_OV_FAULT				
Bit 4	VOUT_UV_FAULT				
7Bh	STATUS_IOUT		Read Byte	1	
Bit 7	Iout OC fault				
Bit 5	Iout OC warning				
Bit 1	Pout OP fault				
Bit 0	Pout OP warning				
7Ch	STATUS_INPUT		Read Byte	1	
Bit 5	Vin UV warning				
Bit 4	Vin UV fault				
Bit 3	Unit off for insufficient input				
Bit 1	Iin over current warning				
Bit 0	Pin over power warning				
7Dh	STATUS_TEMPERATURE		Read Byte	1	
Bit 7	OT fault				
Bit 6	OT warning				
7Eh	STATUS_CML		Read Byte	1	
Bit 7	Invalid COMMAND				
Bit 6	Invalid DATA				

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Bit 5	PEC Failed				
81h	STATUS_FANS_1_2		Read Byte	1	
Bit 7	Fan 1 fault				
Bit 5	Fan 1 warning				
Bit 3	Fan1 speed overridden				
86h	READ_EIN	N/A	Block Read	6	DIRECT Data Format
87h	READ_EOUT	N/A	Block Read	6	DIRECT Data Format
88h	READ_VIN	N/A	Read Word	2	Linear
89h	READ_IIN	N/A	Read Word	2	Linear
8Bh	READ_VOUT	N/A	Read Word	2	Linear16
8Ch	READ_IOUT	N/A	Read Word	2	Linear
8Dh	READ_TEMPERATURE_ 1	N/A	Read Word	2	Ambient
8Eh	READ_TEMPERATURE_ 2	N/A	Read Word	2	SR Hotspot
8Fh	READ_TEMPERATURE_ 3	N/A	Read Word	2	PFC Hotspot
90h	READ_FAN_SPEED_1	N/A	Read Word	2	In RPM
96h	READ_POUT	N/A	Read Word	2	Linear
97h	READ_PIN	N/A	Read Word	2	Linear
98h	PMBUS_REVISION	N/A	Read Byte	1	1.2
99h	MFR_ID	Block Write	Block Read	Variable (3)	"bel"
9Ah	MFR_MODEL	Block Write	Block Read	Variable (16)	"TEC5200-54-074NA"
9Bh	MFR_REVISION	Block Write	Block Read	Variable (3)	"VXX"
9Ch	MFR_LOCATION	Block Write	Block Read	Variable (5)	"CHINA"
9Dh	MFR_DATE	Block Write	Block Read	Variable (8)	"YYYYMMDD"
9Eh	MFR_SERIAL	Block Write	Block Read	Variable (19)	Serial Number
9Fh	APP_PROFILE_SUPPOR T	N/A	Block Read	Variable (2)	PMBus 1.2
A0h	MFR_VIN_MIN	N/A	Read Word	2	180V
A1h	MFR_VIN_MAX	N/A	Read Word	2	264V
A2h	MFR_IIN_MAX	N/A	Read Word	2	
A3h	MFR_PIN_MAX	N/A	Read Word	2	
A4h	MFR_VOUT_MIN	N/A	Read Word	2	52.38V
A5h	MFR_VOUT_MAX	N/A	Read Word	2	55.62V
A6h	MFR_IOUT_MAX	N/A	Read Word	2	
A7h	MFR_POUT_MAX	N/A	Read Word	2	
A8h	MFR_TAMBIENT_MAX	N/A	Read Word	2	
A9h	MFR_TAMBIENT_MIN	N/A	Read Word	2	
AAh	MFR_EFFICIENCY_LL	N/A	Block Read	14	At 20%/50%/100%
ABh	MFR_EFFICIENCY_HL	N/A	Block Read	14	At 20%/50%/100%
C0h	MFR_MAX_TEMP_1	N/A	Read Word	2	
C1h	MFR_MAX_TEMP_2	N/A	Read Word	2	
C2h	MFR_MAX_TEMP_3	N/A	Read Word	2	
D0h	MFR_COLD_ REDUNDANCY_CONFIG	Write Byte	Read Byte	1	
D4h	MFR_HW_COMPATIBILIT Y	N/A	Read Word	2	
D5h	MFR_FWUPLOAD_CAPA BILITY	N/A	Read Byte	1	
D6h	MFR_FWUPLOAD_MOD E	Write Byte	Read Byte	1	
D7h	MFR_FWUPLOAD	Block Write	N/A		
D8h	MFR_FWUPLOAD_STAT US	N/A	Read Word	21	
D9h	MFR_FW_REVISION	N/A	Block Read	3	
DCh	MFR_BLACK_BOX	N/A	Block Read	237	
DDh	MFR_REAL_TIME	Block Write	Block Read	4	
DEh	MFR_SYSTEM_BLACK_ BOX	Block Write	Block Read	40	

DFh	MFR_BLACKBOX_CONFI G	Write Byte	Read Byte	1	
E0h	MFR_CLEAR_BLACKBO X	Send Byte	N/A	1	

Table 2. Supported Power Management Bus Command

Note: Write protocol must include PEC (Packet Error Checking).

7.1 STATUS COMMANDS

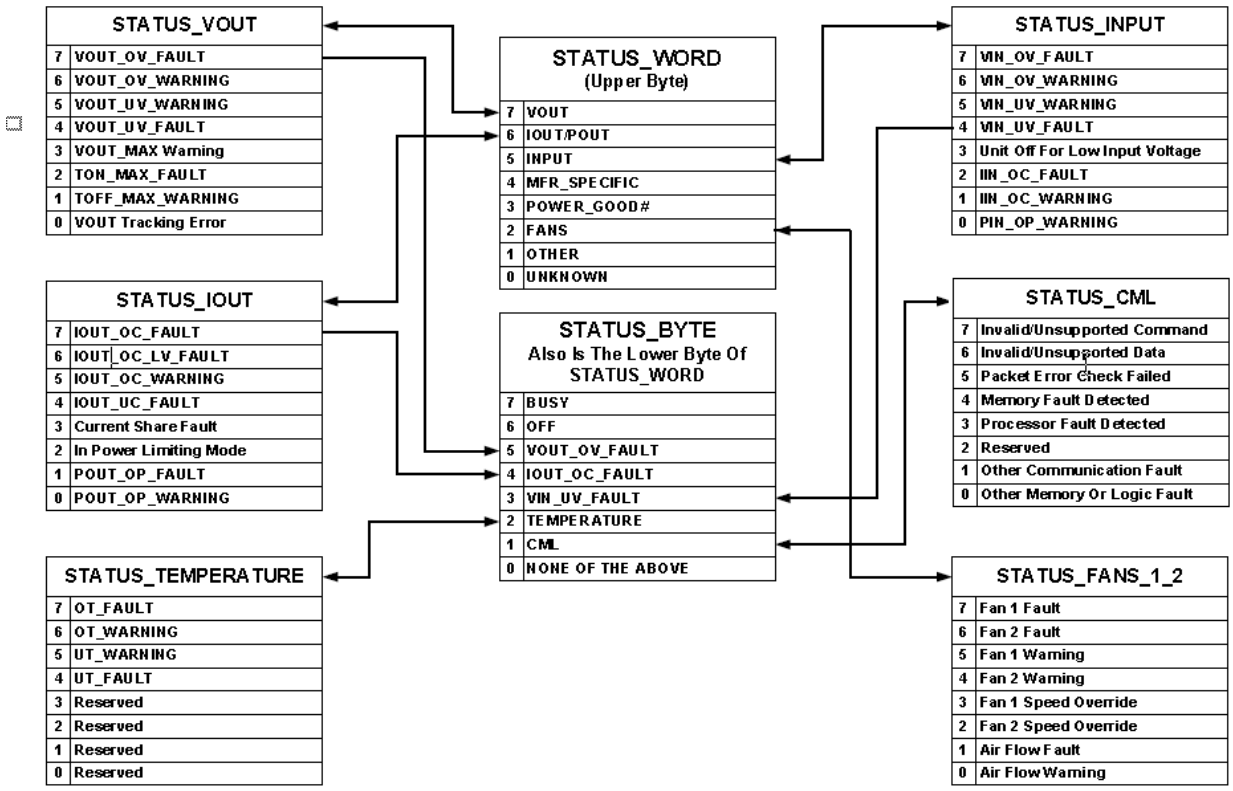

Figure 12. Summary of The Status Registers

The following Power Management Bus STATUS commands shall be supported. All STATUS commands stated in Figure 6 Supporting PAGE instances shall support the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_ PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared

The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_W RITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBAlert# signal. The new SMBALERT_MASK command is used to define which status event control the SMBAlert# signal. Default values for these mask bits are shown in the table below.

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Power Management Bus command	Bit location	PSU state when bit is asserted ('1')	Instances No PAGE'ing2 PAGE 00h = BMC PAGE 01h = ME	SMBALERT_MASK defaults for each of the three instances (No PAGE, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#
STATUS_WORD			No PAGE, 00h, 01h	
OFF	6 (lower)	OFF		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
CML	1 (lower)	ON		NA
VOUT	7 (upper)	Refer to STATUS_VOUT		NA
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		NA
INPUT	5 (upper)	Refer to STATUS_INPUT		NA
FANS	2 (upper)	Refer to STATUS_FANS		NA
STATUS_VOUT			No PAGE'ing	
VOUT_OV_FAULT	7	OFF		1, 1, 1
VOUT_UV_FAULT	4	OFF		1, 1, 1
STATUS_IOUT			No PAGE'ing, 00h,01h	
IOUT_OC_FAULT	7	OFF		1, 1, 1
IOUT_OC_WARNING	5	ON		1, 1, 0
POUT_OP_FAULT	1	OFF		1, 1, 1
POUT_OP_WARNING	0	ON		1, 1, 1
STATUS_INPUT			No PAGE'ing, 00h,01h	
VIN_UV_WARNING	5	ON		1, 1, 1
VIN_UV_FAULT 1	4	OFF		1, 1, 0
Unit off for low input voltage	3	OFF		1, 1, 1
IIN_OC_WARNING	1	ON		1, 1, 1
PIN_OP_WARNING	0	ON		1, 1, 1
STATUS_TEMPERATURE			No PAGE'ing, 00h,01h	
OT_FAULT	7	OFF		1, 1, 1
OT_WARNING	6	ON		1, 1, 0
STATUS_FANS_1_2			No PAGE'ing	
Fan 1 fault 3	7	OFF		1, 1, 1
Fan 1 warning 3	5	ON		1, 1, 1

Table 3. Power Management Bus STATUS Commands Summary

1. The Vin Fault bit in STATUS_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time; even if the PSU continues to operate normally through a momentary input dropout event.
2. 'No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.

7.2 POWER MANAGEMENT BUS TEMPERATURE READ COMMANDS

The following temperature read commands as documented by the Power Management Bus specification Part II version 1.2 should be supported.
READ_TEMPERATURE_1(8Dh), should provide the PSU inlet temperature.
READ_TEMPERATURE_2(8Eh), should provide the temperature of the SR heat sink in the PSU.
READ_TEMPERATURE_3(8Fh), should provide the temperature of the PFC heat sink in the PSU.

7.3 PAGE (00h)

Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command.

7.4 OPERATION (01h)

The OPERTION command is used to configure the operational state of the converter, in conjunction with input from the CONTROL pin. The OPERATION command is used to turn the Power Management Bus device output on and off.
Bit [7] controls whether the Power Management Bus device output is on or off.
If Bit [7] is cleared (equals 0) then the output is off. If Bit [7] is set (equals 1), then the output is on.

7.5 ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.
The default response for any PMBus device is specified by the device manufacturer.

Example conditions:
a. If bit [4] is cleared, then the unit powers up and operates any time bias power is available regardless of the setting of bits [3:0].
b. If bit [4] is set, bit [3] is set, and bit [2] is cleared, then the unit is turned on and off only by commands received over the serial bus.
c. If bit [4] is set, bit [3] is cleared, and bit [2] is set, then the unit is turned on and off only by the CONTROL pin.

If bit [4] is set, bit [3] is set, and bit [2] is set, then the unit is turned on and off only when both the commands received over the serial bus AND the CONTROL pin are commanding the device to be on. If either a command from the serial bus OR the CONTROL pin commands the unit to be off, the unit turns off.

BIT NUMBER	PURPOSE	BIT VALUE	MEANING
[7:5]		000	Reserved For Future Use
4	Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and serial bus commands	0	Unit powers up any time power is present regardless of state of the CONTROL pin
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command (as programmed in bits [3:0]).
3	Controls how the unit responds to commands received via the serial bus	0	Unit ignores the on/off portion of the OPERATION command from serial bus
		1	To start, the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit [2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.
2	Controls how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin (on/off controlled only the OPERATION command)
		1	Unit requires the CONTROL pin to be asserted to start the unit. Depending on bit [3], the OPERATION command may also be required to instruct the device to start before the output is energized.
1	Polarity of the CONTROL pin	0	Active low (Pull pin low to start the unit)
		1	Active high (Pull high to start the unit)
0	CONTROL pin action when commanding the unit to turn off	0	Use the programmed turn off delay and fall time
		1	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

Table 4. ON_OFF_CONFIG Data Byte

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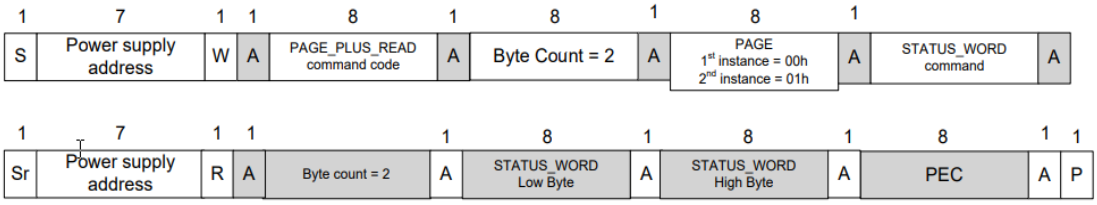
7.6 CLEAR_FAULTS COMMAND (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT# signal output if the device is asserting the SMBALERT# signal.

7.7 PAGE_PLUS_WRITE / PAGE_PLUS_READ COMMANDS (05h/06h)

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_VOUT, and STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

Reading STATUS_WORD
Block Write – Block Read Process Call with PEC



Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write – Block Read Process Call with PEC

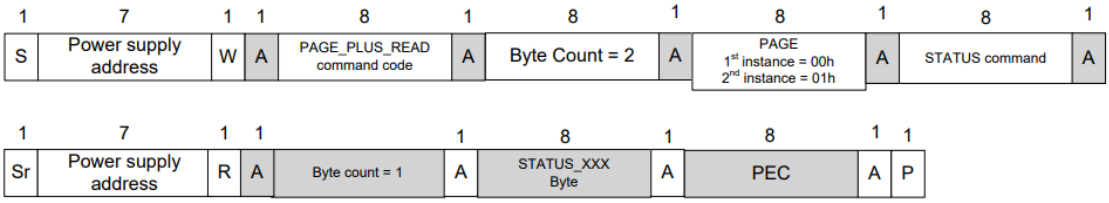


Figure 13. Reading STATUS commands with PAGE_PLUS_READ

Clearing STATUS commands (write '1' to clear a bit) STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write with PEC

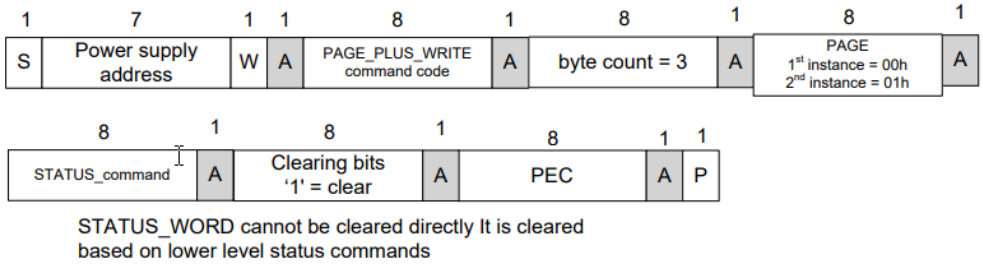


Figure 14. Clearing STATUS commands using PAGE_PLUS_WRITE

7.8 CAPABILITY (19h)

This command provides a way for a host system to determine some key capabilities of a Power Management Bus device. There is one data byte formatted as shown in table below. This command is read only.

BITS	DESCRIPTION	VALUE	MEANING
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
		01	Maximum supported bus speed is 400 kHz
		10	Reserved
		11	Reserved
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol
		1	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol
3:0	Reserved	X	Reserved

Table 5. CAPABILITY COMMAND Data Byte Format

7.9 QUERY (1Ah)

The QUERY command is used to ask a Power Management Bus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write-Block Read Process Call described in the SMBus specification.

BITS	VALUE	MEANING
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write
	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read
4:2	000	Linear Data Format used
	001	16 bit signed number
	010	Reserved
	011	Direct Mode Format used
	100	8 bit unsigned number
	101	VID Mode Format used
	110	Manufacturer specific format used
	111	Command does not return numeric data. This is also used for commands that return blocks of data.
1:0	XX	Reserved for future use

Table 6. QUERY Command Returned Data Byte Format

If bit [7] is zero, then the rest of the bits are “don’t care”.

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7.10 SMBALERT_MASK (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a '1' to the associated STATUS bits. The SMBALERT_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. It is not supported for masking the Non-PAGE'd STATUS_ commands. Below are the protocols.

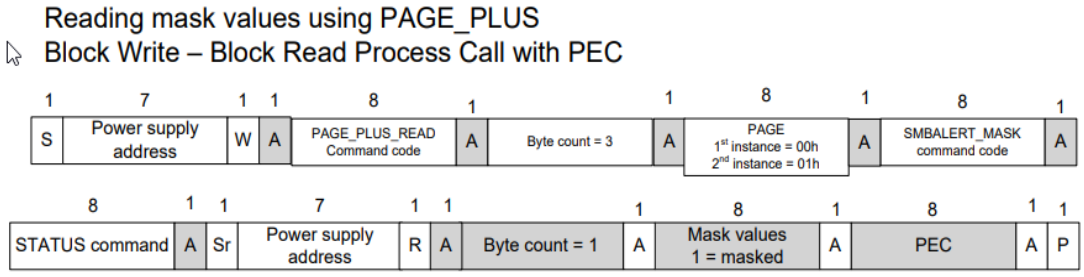

Figure 15. PAGE_PLUS_READ command.

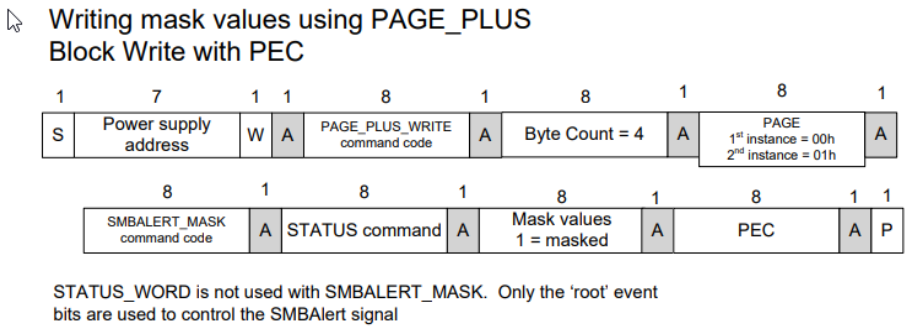

Figure 16. PAGE_PLUS_WRITE command.

7.11 COEFFICIENT (30h)

The power supply shall support the Power Management Bus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN and READ_EOUT accumulated power values.

COMMAND	COEFFICIENTS SUPPORT	M	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h

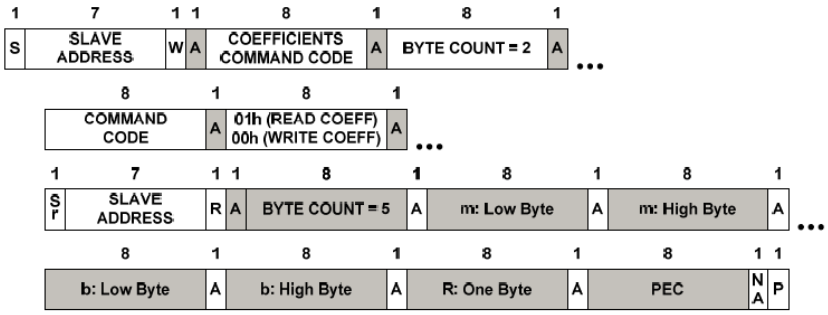

Figure 17. Retrieving Coefficients Using PEC

7.12 FAN_CONFIG_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

The first of the configuration tells the Power Management Bus device whether or not a fan associated with position 1 (or 2) is installed. Any combination of fan installation is permitted.

The second part of the configuration tells the device whether the fan speed commands are in RPM or PWM duty cycle (in percent). These settings do not have to be the same for Fan 1 and Fan 2.

The third part of the configuration data tells the Power Management Bus device the number of tachometer pulses per revolution each fan provides. This information is needed for commanding and reporting fan speed in RPM. Two bits are provided for each fan. These settings do not have to be the same for Fan 1 and Fan 2. The binary values of these bits map to pulses per revolution as follows:

- 00b = 1 pulse per revolution,
- 01b = 2 pulses per revolution,
- 10b = 3 pulses per revolution,
- 11b = 4 pulses per revolution.

This command has one data byte formatted as follows:

BITS	VALUE	MEANING
7	1	Fan in position 1
6	0	Fan 1 commanded in Duty Cycle
	1	Fan 1 commanded in RPM
5:4	00b-11b	Fan 1 Tachometer Pulses Per Revolution
3	0	No fan in position 2
2	Not used	
1:0	Not used	

Table 7. FAN_CONFIG_1_2 Command

7.13 FAN_COMMAND_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN_COMMAND_1 command. This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU minimum speed of the thermal requirement.

The default control mode of fan is RPM.

7.14 READ_FAN_SPEED_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the Power Management Bus linear format.

7.15 POWER MANAGEMENT BUS_REVISION (98h)

This is a correction to the table in the Power Management Bus part II specification regarding the POWER MANAGEMENT BUS_REVISION command.

BITS [7:4]	PART I REVISION	BITS [3:0]	PART II REVISION
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2
0011	1.3	0011	1.3

Table 8. POWER MANAGEMENT BUS_REVISION Command

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7.16 MFR-EFFIENCY_LL (AAh)

The MFR_EFFICIENCY_LL command sets or retrieves information about the efficiency of the device while operating at a low line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power is specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

BYTE NUMBER	BYTE ORDER	DESCRIPTION
0	Low Byte	The input voltage, in volts, at which the low line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power, in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percent, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer.
13	High Byte	

Table 9. MFR_EFFICIENCY_LL

7.17 MFR-EFFIENCY_HL (ABh)

The MFR_EFFICIENCY_HL command sets or retrieves information about the efficiency of the device while operating at a high line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power is specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

BYTE NUMBER	BYTE ORDER	DESCRIPTION
0	Low Byte	The input voltage, in volts, at which the high line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percent, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer.
13	High Byte	

Table 10. MFR_EFFICIENCY_HL

7.18 READ EIN (86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

	MIN	MAX	DESCRIPTION
Format	Power Management Bus Direct format m = 01h, R = 00h, b = 00h		Power Management Bus data format; refer to Power Management Bus specification for details.
Psample averaging period	4 AC cycles		Period instantaneous input power is averaged over to calculate Psample.
READ_EIN update period	80/66.7ms (50/60Hz)		Period at which the power accumulator and sample counter are updated
Range of System polling period	1 sec	100 ms	The PSU shall be polled over this range of rates while testing accuracy.

IMPORTANT:

The PSU READ_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).

Table 11. READ_EIN Requirements Summary

7.19 READ EOUT (87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

	MIN	MAX	DESCRIPTION
Format	Power Management Bus Direct format m = 01h, R = 00h, b = 00h		Power Management Bus data format; refer to Power Management Bus specification for details.
Psample averaging period	Nominal 50 ms		Period instantaneous input power is averaged over to calculate Psample.
Sampling period	Nominal 50 ms		Period at which the power accumulator and sample counter are updated
System polling rate	1 sample /s	10 samples /s	The PSU shall be polled over this range of rates while testing accuracy.

Table 12. READ_EOUT Requirements Summary

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7.20 READ_EIN & READ_EOUT FORMATS

The READ_EIN and READ_EOUT commands shall use the Power Management Bus direct format to report an accumulated power value and the sample count. The Power Management Bus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the Power Management Bus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

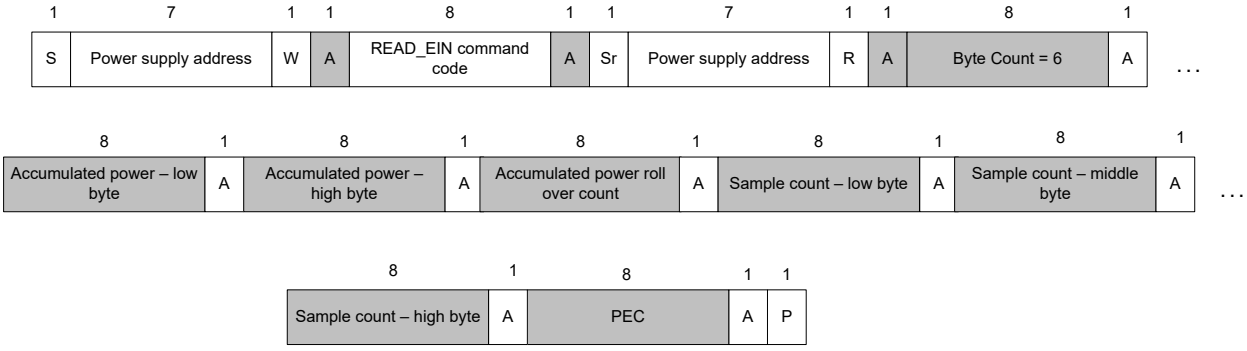

Figure 18. READ_EIN Command

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached (> 7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

IMPORTANT NOTE:

When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always alignment with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.

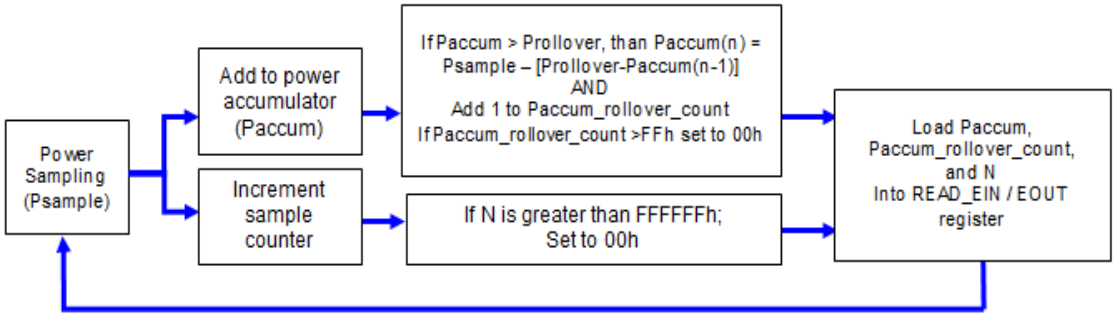

Figure 19. READ_EIN PSU Functional Diagram

VALUE	DESCRIPTION
Psample:	The sampled power value in linear or direct format
Paccum:	2 bytes in Power Management Bus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n)
N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

7.21 POWER SUPPLY ACCURACY

The following Power Management Bus commands shall be supported for the purpose of monitoring current, voltage, and power. All sensors shall continue providing real time data as long as the Power Management Bus device is powered. This means in standby mode the main output(s) of the PSU shall be zero amps and zero volts. Sensors meet the requirements at nominal input voltage; maximum deviation for the ambient temperature is ± 3 °C.

	=<100W	>100W - < 20% load	≥20% load -100 % load
Pin/Ein	±10% or ±10 W	±3%	±2%
Iin	±5% or ±0.1 A	±3%	±2%
Iout	±5% or ±1 A	±3%	±2%
Pout/Eout	±5% or ±10 W	±3%	±2%
54Vout		±3%	
Vin		±2%	
FAN		±500 rpm	
AMB Temperature		±3% °C	

Table 13. Power Management Bus Accuracy for AC-DC Models

Notes:

1. The spec is based on input voltage 230 VAC and 240 VDC measurement, the Max. output may be different between low and high line, the load definition where is taken Max. value.

2. In 240 VDC application, no matter the input polarity is positive or negative, the PSU could operate normally, but Accuracy shall be measured when positive polarity on Neutral. If customer may apply positive polarity on either one, please inform bel early.

3. For light load reporting requirement, in the normal redundant application, PSU shall report below value to system once the below condition is set, which is not included the PSU that in cold redundant mode and set as slave.

For system power calculation requirement, the reporting performance shall make sure the Pin > Pout situation.

4. The accuracy of AMB temperature is defined as the temperature around the temperature sensor inside of PSU, thereby this accuracy performance shall measure the closest point on the inlet chassis to internal temperature sensor.

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7.22 LINEAR DATA FORMAT

The Linear Data Format is typically used for commanding and reporting the parameters such as (but not only) the following:

- Output Current,
- Input Voltage,
- Input Current,
- Operating Temperatures,
- Time (durations), and Energy Storage Capacitor Voltage.

The Linear Data Format is a two byte value with:

- An 11 bit, two's complement mantissa and,
- A 5 bit, two's complement exponent (scaling factor),

The format of the two data bytes is illustrated in Figure as show below.

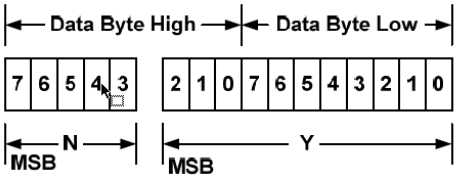

Figure 20. Linear Data Format Data Bytes

The relation between *Y*, *N* and the "real world" value is:
$X = Y \cdot 2^N$

Where, as described above:
X is the "real world" value;
Y is an 11 bit, two's complement integer; and
N is a 5 bit, two's complement integer.

Devices that use the linear format must accept and be able to process any value of N.

7.23 VOUT_MODE (20h)

The data byte for the VOUT_MODE command is one byte that consists of a three bit Mode and a five bit exponent. The three bit Mode shall be set to indicate the LINEAR mode for output voltage related commands. The five bit Exponent shall be set to indicate the value of the five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

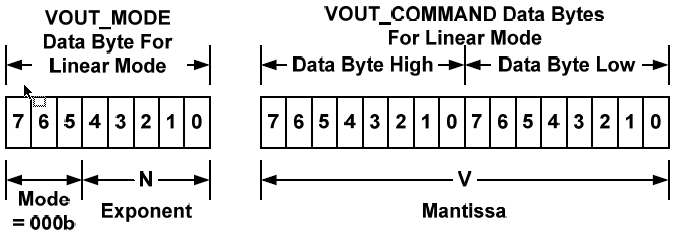

Figure 21. Linear Format Data Bytes

The voltage, in volts, is calculated from the equation Voltage = $V \cdot 2^N$, where:

- V is a 16 bit unsigned binary integer
- N is a 5 bit two's complement binary integer

Sending the VOUT_MODE command with the address set for writing is not supported. If the system sends a VOUT_MODE command for a write, the power supply shall reject the command, and set the Invalid/Unsupported Data bit in the STATUS_CML register.

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8 COLD REDUNDANCY

8.1 OVERVIEW

Below is a block diagram showing the Cold Redundancy architecture. When the power subsystem is in Cold Redundant mode; only the needed power supply to support the best power delivery efficiency are ON. Any additional power supplies; including the redundant power supply, is in Cold Standby state.

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted (pulled low) when there is a fault in any power supply OR the power supplies output voltage falls below the Vfault threshold. Asserting the CR_BUS signal causes all power supplies in Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a Power Management Bus command.

Whenever there is no Cold Redundant active power supply on the Cold Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined Cold Redundant roll (active or Cold Standby). This guarantees that incorrect programming of the Cold Redundancy states of the power supply will never cause the power subsystem to shut down or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.

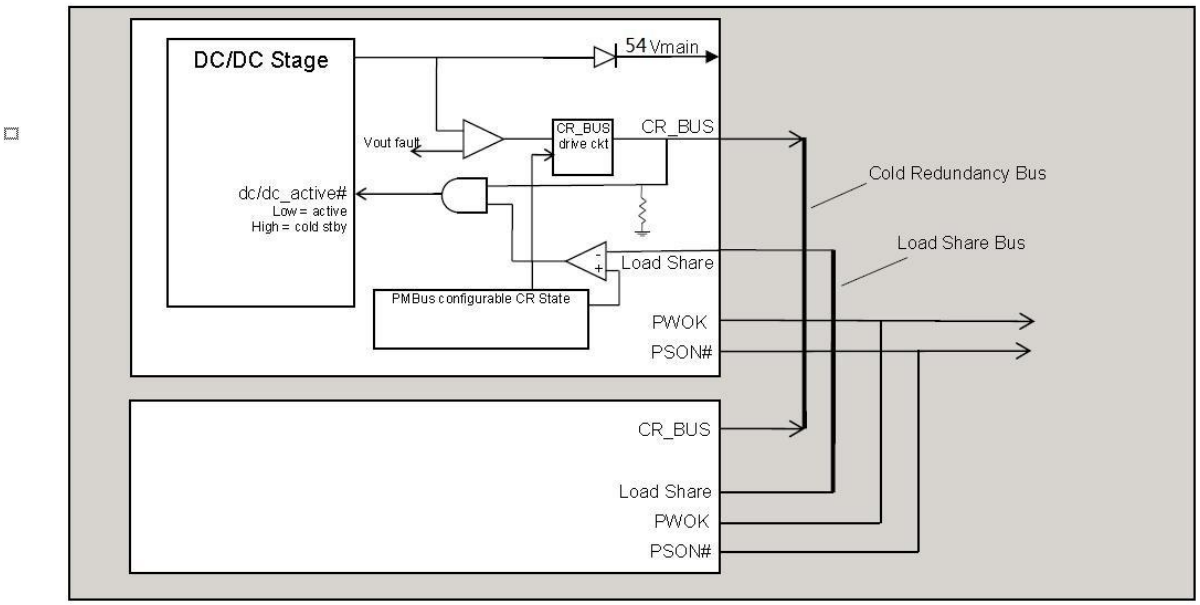

Figure 22. Cold Redundancy 1+1 Functional Block Diagram

CR_BUS	LOAD SHARE	DC/DC_ACTIVE#	COLD STANDBY POWER SUPPLY STATE(S)
High	< V_{CR_ON}	High	Cold Standby
Low	< V_{CR_ON}	Low	Active
High	> V_{CR_ON}	Low	Active
Low	> V_{CR_ON}	Low	Active

Table 14. Logic Matrix for Cold Standby Power Supplies

8.2 POWERING ON COLD STANDBY SUPPLIES TO MAINTAIN BEST EFFICIENCY

Power supplies in Cold Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the cold standby configuration; will slightly change the load share threshold that the power supply shall power on at.

	Enable Threshold for $V_{CR_ON_EN}$	Disable Threshold for $V_{CR_ON_DIS}$	CR_BUS De-asserted / Asserted States
Standard Redundancy	N/A; Ignore dc/dc_ active# signal; power supply is always ON		OK = Tri-state Fault = Low
Cold Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
Cold Standby 1 (02h)	3.2 V (40% of max)	90% x (3.2V x 1/2) = 1.44 V	OK = Tri-state Fault = Low
Cold Standby 2 (03h)	5.0 V (62% of max)	90% x (5.0V x 2/3) = 3.01 V	OK = Tri-state Fault = Low
Cold Standby 3 (04h)	6.7 V (84% of max)	90% x (6.7V x 3/4) = 4.52 V	OK = Tri-state Fault = Low

Table 15. Example Load Share Threshold for Activating Supplies

Notes:
Maximum load share voltage = 8.0 V at 100% of rated output power
These are example load share bus threshold; for any power supply these shall be customized to maintain the best efficiency curve that specific model.

8.3 POWERING ON COLD STANDBY SUPPLIES DURING A FAULT OR OVER CURRENT CONDITION

When an active power supply asserts its CR_BUS signal (pulling it low), all parallel power supplies in cold standby mode shall power on within 100 µsec.

8.4 COLD REDUNDANCY SMBUS COMMANDS

The Power Management Bus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to cold redundancy. We will call the command Cold_Redundancy_Config (D0h).
Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

VALUE	STATE	DESCRIPTION
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's CR_BUS signal shall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1*	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2*	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3*	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.
05h	Always Standby	Defines this power supply to be always in cold redundant configuration no matter what the load condition

* When the CR_BUS transitions from a high to a low state; each PSU programmed to be in Cold Standby state shall be put into Standard Redundancy mode (Cold_redundancy_Config = 00h). For the power supplies to enter Cold Redundancy mode the system must re-program the power supplies using the Cold_Redundancy_Config command.

Table 16. Cold_Redundancy_Config (D0h)

8.5 COLD REDUNDANT SIGNALS

There is an additional signal defined supporting Cold Redundancy. This is connected to a bus shared between the power supplies; the CR_BUS.

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9 BLACK BOX

9.1 BLACK BOX FUNCTION DESCRIPTION

This specification defines the requirements for power supplies with Power Management Bus capability to store Power Management Bus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shutdown. The data can be accessed via the Power Management Bus interface by applying power to the 12Vstby pins. No AC power need to be applied to the power supply.

9.2 WHEN IS DATA SAVED TO THE BLACK BOX?

Data is saved to the Black Box for the following fault events:

- General fault
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

9.3 BLACK BOX EVENTS

There are two types of data saved in the black box:

1) System Tracking Data.
2) Power supply event data.

System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

9.4 BLACK BOX PROCESS

- System writes system tracking data to the power supply RAM at power ON.
- System writes the real time clock data to the PSU RAM once every ~5 minutes.
- Power supply tracks number of PSON# and AC power cycles in EEPROM.
- Power supply tracks ON time in EEPROM
- Power supply loads warning and fault event counter data from EEPROM into RAM
- Upon a warning event; the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM
- Upon a fault event that causes the PSU to shut down all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON# power cycles, PSU ON time, warning event counters and fault event counters.

9.5 RELATED COMMAND OF BLACK BOX

The following command set will be used for Black Box function via the Host System. The commands and protocol used by the Host System and shall be implemented by the microcontroller are defined by this document.

COMMAND CODE	COMMAND NAME	SMBUS TRANSACTION TYPE	NUMBER OF DATA BYTES	REMARK
DCh	MFR_BLACK_BOX	Read only	237	Read the data of the Black box.
DDh	MFR_REAL_TIME	Read/Write	4	Read/Write the data of MFR real time.
DEh	MFR_SYSTEM_BLACK_BOX	Read/Write	40	Read/Write the data of MFR system black box.
DFh	MFR_BLACKBOX_CONFIG	Read/Write	1	Read/Write the data of MFR black box configure.
E0h	MFR_CLEAR_BLACKBOX	Write only	1	Send one byte to clear all data of black box.

1) Command Name: MFR_BLACKBOX

Format: Read Block with PEC (237 bytes)

Code: DCh

	ITEM	NUMBER OF BYTES	DESCRIPTION
System Tracking Data	System top assembly number	10	The system will write its Intel part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON# asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON# power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these time and power cycle counters in RAM. When a black box event occurs, the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System (reserved for future use)	4	This time stamp does not need to be generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON# power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply.
Power Management Bus			The power supply shall save these Power Management Bus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the Power Management Bus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	

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	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. These values shall be saved to the black box when a black box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	
	Input voltage warning; no shutdown	Lower ½	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
Power supply event data (N-1)		38	
Power supply event data (N-2)		38	
Power supply event data (N-3)		38	
Power supply event data (N-4)		38	

2) Name: MFR_REAL_TIME_BLACK_BOX

Format: Write/Read Block with PEC (4 bytes)

Code: DDh

The system shall use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSIC.

3) Name: MFR_SYSTEM_BLACK_BOX

Format: Write/Read Block with PEC (40 bytes). Low byte first.

Code: DEh

The system uses this command to write the following data to the PSU.

Item	Bytes	
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

1)

4) Name: MFR_BLACKBOX_CONFIG

Format: Read/Write Byte with PEC

Code: DFh

BIT	VALUE	DESCRIPTION
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. Intel shall receive the power supply with the black box function enabled; bit 0 = '1'.
1-7		Reserved

5) Name: MFR_CLEAR_BLACKBOX

Format: Send Byte with PEC

Code: E0h

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously.

This command is write only. There is no data byte for this command.

9.6 HARDWARE REQUIREMENTS

The SMBus interface shall be used to access the Black Box data. It may be accessed when the power supply is ON or in standby mode. It also may be accessed when no AC power is applied, and power is only applied at the standby output pins by an external source (12Vstby).

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10 BOOTLOADER

10.1 FUNCTION DESCRIPTION

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). It is desired that any other microcontroller in the power supply also be able to be updated with this same process (example: primary side microcontroller); however, this is not a requirement at this time.

10.2 FW IMAGE MAPPING

The power supply firmware image shall be made up of two parts; 1) Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1) Boot Loader:
This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling, and protections (UV, OV, OC).

2) Main Program:
This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

10.3 POWER SUPPLY OPERATING MODE DURING AND AFTER FIRMWARE UPDATE

1) Firmware update mode in ON state with no power cycle needed:
Power supply may be able to support FW upload in the ON state. The new FW will take effect once it is taken out of FW upload load.

2) Bad image after firmware update:
The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

10.4 TEC3500-48-074NA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	T	Model Name 13 bytes
Byte 12	E	
Byte 13	C	
Byte 14	5	
Byte 15	2	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	5	
Byte 20	4	
Byte 21	N	
Byte 22	A	
Byte 23		
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

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10.5 FIRMWARE UPDATE PROCESS

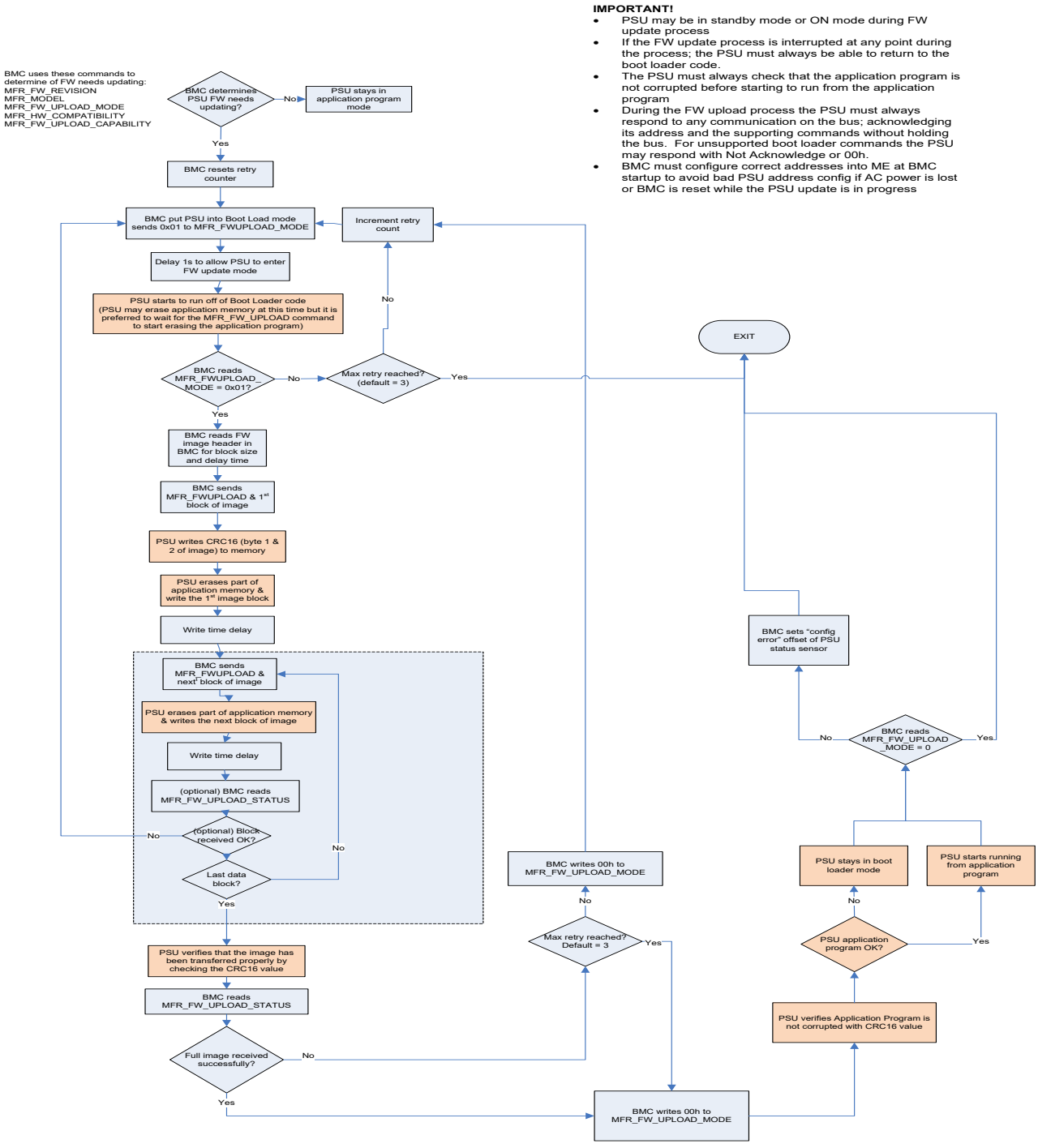

Figure 23. PSU Upload Process

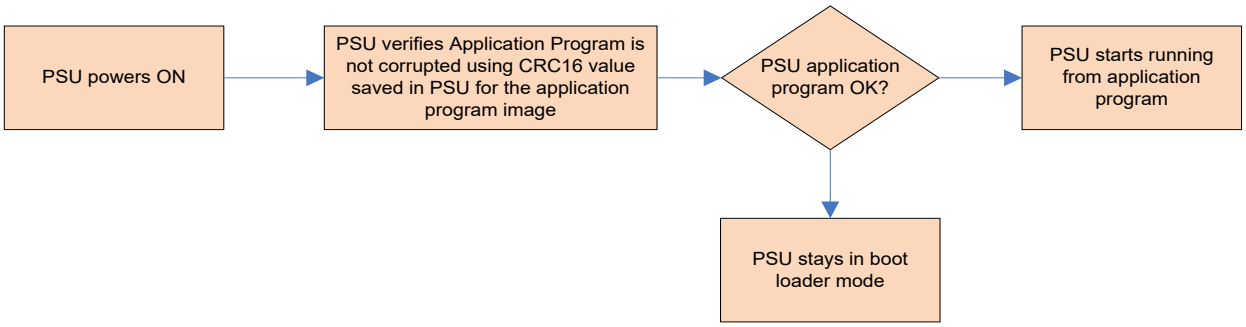

Figure 24. PSU flow during powering ON

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10.6 RELATED COMMAND OF BOOTLOADER

1) Name: MFR_HW_COMPATIBILITY

Format: Read Word

Code: D4h

BYTES	VALUE	DESCRIPTION
low	ASCI code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCI code for second letter/number of the PSU HW compatibility.	

2) Name: MFR_FWUPLOAD_CAPABILITY

Format: Read Byte

Code: D5h

The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

BIT	VALUE	DESCRIPTION
0 (for future use)	1 = PSU support FW uploading in standby mode only	For future use
1 (for future use)	1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON#.	For future use
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

3) Name: MFR_FWUPLOAD_MODE

Format: Read/Write Byte

Code: D6h

BIT	VALUE	DESCRIPTION
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7		Reserved

4) Name: MFR_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

Code: D7h

BYTES	VALUE	DESCRIPTION
Block size defined in header	Image header & image data	Command used to send each block of the FW image. Header should follow the format described in section 13.4. The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

5) Name: MFR_FWUPLOAD_STATUS

Format: Read Word

Code: D8h

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.
Reset: all bits get reset to '0' when the power supply enters FW upload mode.

BIT	DESCRIPTION
0	1 = Full image received successfully
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3 (for future use)	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.
4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5 – 15	Reserved

6) Name: MFR_FW_REVISION

Format: Block Read, 5 bytes

Code: D9h

BYTE	VALUE	DESCRIPTION
0	0 - 255	Minor revision; secondary
1	0 - 255	Minor revision; primary
2	0 - 255	Bit 7: 1-> Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed but recommended to follow. 0→ No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision
3	0 - 255	Minor revision; Third MCU
4	0 - 255	Minor revision; Fourth MCU

7) MFR_MODEL (existing Power Management Bus command)

Code: 9Ah

Maximum of 17 byte value; ending in terminator character.

8) MFR_REVISION (existing Power Management Bus command)

Code: 9Bh

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11 ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

The power supply complies with the limits defined in EN 55035.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Electrostatic Discharge	IEC / EN 61000-4-2	B
Radiated Immunity	IEC / EN 61000-4-3	B
Fast Transient / Burst	IEC / EN 61000-4-4	B
Surge Immunity	IEC / EN 61000-4-5 (3 kV line to ground and 2 kV line to line)	A
Conducted Susceptibility	IEC / EN 61000-4-6	
Power Frequency Magnetic Immunity	IEC / EN 61000-4-8	
Voltage Dips and Interruptions	IEC / EN 61000-4-11	

11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted & Radiated Emissions	EN 55032 / CISPR 32	Class A 6 dB margin
Power Harmonics	EN 61000-3-2	Class A
Voltage Fluctuation and Flicker	EN 61000-3-3	Class A
Acoustic Noise	Variable speed fan(s) incorporated, measured accord. to ECMA 74 and reported according to ISO 9296.	TBD dBA

12 SAFETY / APPROVALS

PARAMETER	DESCRIPTION / CONDITION
Agency Approvals (pending)	• UL/CSA 62368-1 (USA/Canada) • IEC 62368-1 (Europe/International) • CB Certificate & Report, IEC 62368-1 (Report to include all country national deviations)) • CE – Low Voltage Directive 2006/95/EC (Europe) • GB4943 – CNCA Certification (China) • BSMI Certification (Taiwan)
Leakage Current	Max. 0.875 mA at 264 VAC, 60 Hz

13 ENVIRONMENTAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Ambient Temperature	Operating	-5		+55	°C
	Non-Operating	-40		+70	
Humidity	Operating, relative (non-condensing)	5		85	%
	Non-Operating, relative (non-condensing)	5		95	
Altitude	Operating, T_A = 45°C max.	0		5 000	ft
	Non-Operating	0		15 200	ft
Mechanical Shock (non-operating)	50 G Trapezoidal Wave, Velocity change = 170 in. / sec Three drops in each of six directions are applied to each of the samples.				
Vibration (non-operating) sinusoidal	1.5G, pk-pk, 10 Hz-500 Hz–10 Hz, 0.5 octave/min; 2 sweeps per axis. Three mutually perpendicular axes.				
Vibration (non-operating) random	2 Grms, 10 Hz-500 Hz, 60 mins per axis Three mutually perpendicular axes.				
Thermal Shock (non-operating)	50 cycles, 30°C /min. ≧ transition time ≧ 15°C /min duration of exposure to temperature extremes for each half cycle shall be 30 minutes.	-40		+70	°C
Audible Noise	@ 100% rated DC load and inlet T_A = 25°C,			80	dB

14 RELIABILITY

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Mean time between failures (MTBF)	T_A = 25°C, 100% load, according Telcordia SR-332	200 000			h

15 MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions (W x H x L)			73.5 x 40.0 x 265 2.89 x 1.57 x 10.43		mm in
Weight			1330		g

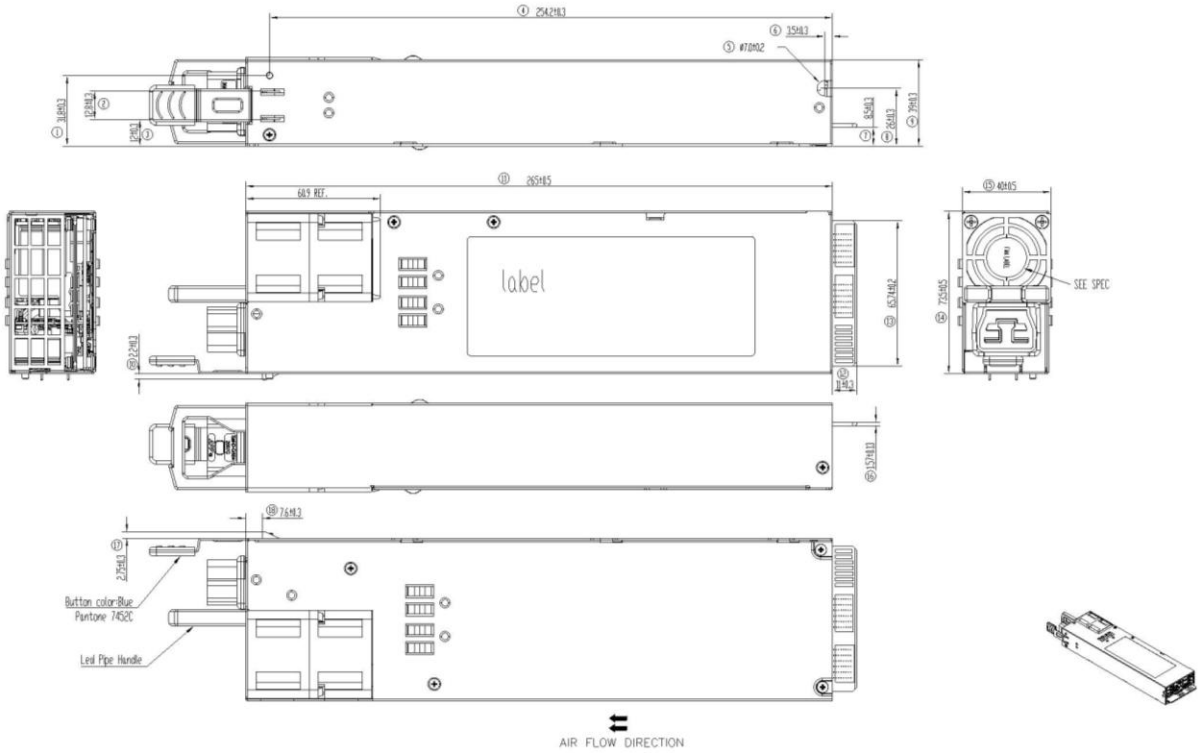

Figure 25. Mechanical Drawing of Standard Product

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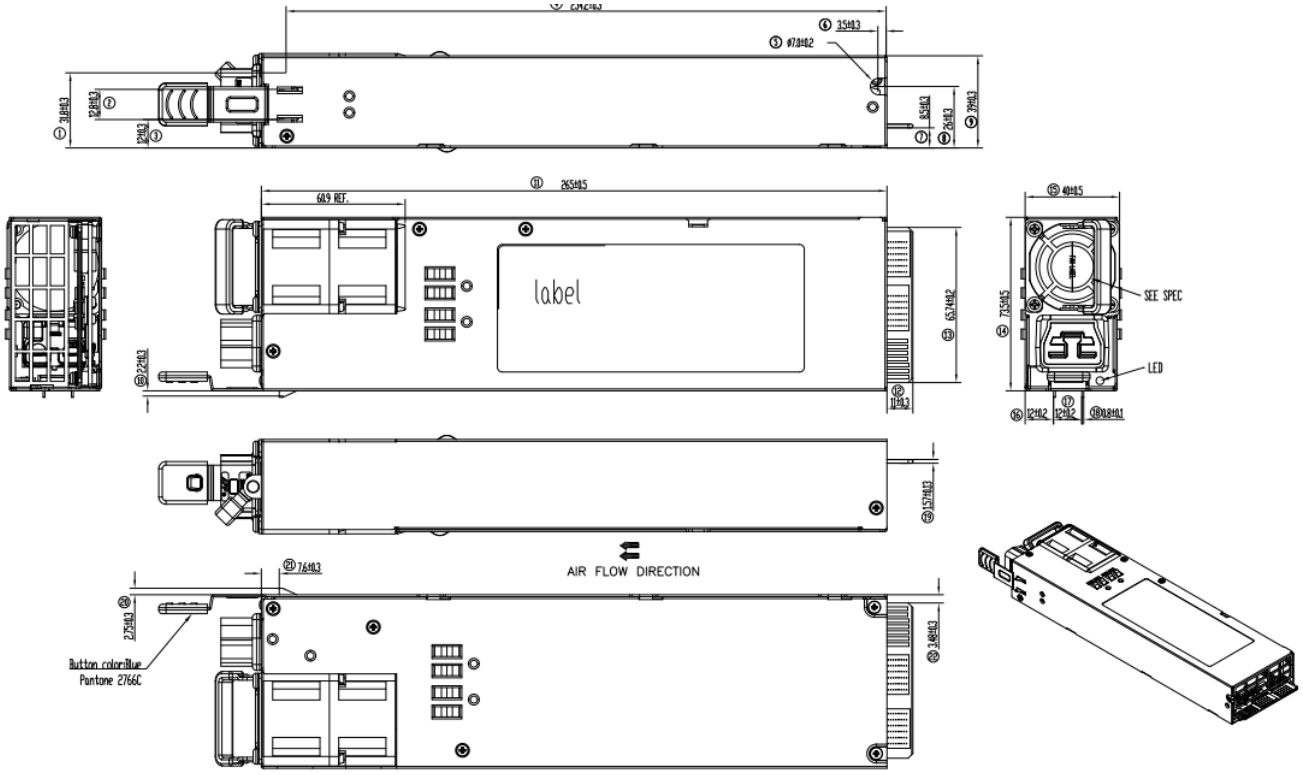

Figure 26. Mechanical Drawing of Custom Product G1S653

15.1 AIRFLOW DIRECTION

The normal airflow direction (NA) is from the card edge connector side to the AC inlet side of the power supply.

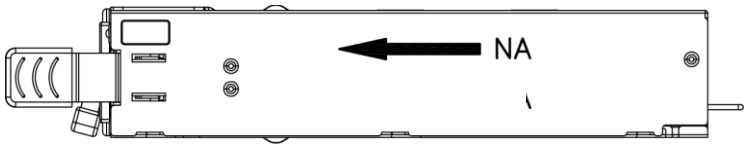

Figure 27. Airflow Direction

15.2 HANDLE RETENTION

The power supply has a handle to assist extraction. The module can be inserted and extracted without the assistance of tools. The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.
The handle protects the operator from any burn hazard through the use of the Customer Corporation Industrial designed plastic handle.

15.3 LED MARKING AND IDENTIFICATION

The power supply has a single bi-colored LED for indication of the power supply status Green & Amber.
The below table showing the LED states for each power supply operating state.

POWER SUPPLY CONDITION	LED STATE
Output ON and OK	GREEN
No AC power to all power supplies	OFF
PSU standby state AC present / Only 12 VSB on	1 Hz Blink GREEN
Power supply is cold standby state or always standby state as defined in the Cold Redundancy section of the CRPS Common Requirements Specification	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	RED
Power supply critical event causing a shutdown; failure, over current, short circuit, over voltage, fan failure.	RED
Power supply warning events where the power supply continues to operate; high temp, high power, high current.	1 Hz Blink RED
Power supply FW updating	2 Hz Blink GREEN

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16 CONNECTORS

16.1 AC INLET CONNECTOR

The AC input receptacle is Anderson 2007G1S-BK 400V Ultra short receptacles (in the footprint of an IEC 320 C14 type connector system), maximum carrying current 30 A at 400 VAC / VDC rating. This connector is located at the front side of power supply. There is a retainer to fix the line cord to avoid accident disconnection.

16.2 DC OUTPUT CONNECTOR PIN LOCATIONS

The power supply has a card edge output that interfaces with 2*25 card edge connector in the system.
The Matting connector at system side is OUPIIN (9305-4P12S14B7SAA01)

PIN-OUT	DEFINITION	PIN-OUT	DEFINITION
A1	GND	B1	NC
A2-8	GND	B2-8	GND
A9	NC	B9	NC
A10	+54V	B10	NC
A11-17	+54V	B11-17	+54V
A18	NC	B18	NC
A19	Power Management Bus SDA	B19	A0 (SMBus address)
A20	Power Management Bus SCL	B20	A1 (SMBus address)
A21	PSON#	B21	+12V stby
A22	SMBAlert#	B22	Cold Redundancy
A23	Return Sense (Remote sense-)	B23	+54V Load share bus
A24	+54V remote Sense (Remote sense+)	B24	PRESENT#
A25	PWOK	B25	VINOK

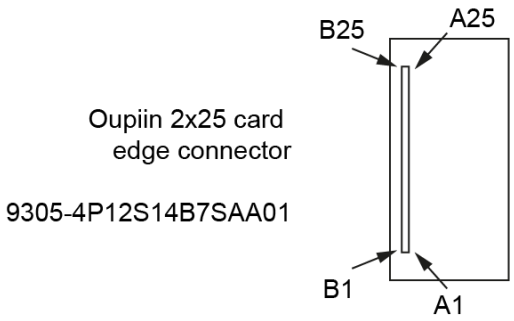

Figure 28. Back DC output golden finger port

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.