TEC2000-12-074xA

AC-DC CRPS Front-End Power Supply



TEC2000-12-074xA is a 2000 Watt, CRPS AC to DC power supply module with a +12.2 V main DC output and a +12.2 V standby output. The power supply operates as a single supply, or N+1 parallel configuration.
TEC2000-12-074xA utilizes full digital control architecture for greater efficiency, control and functionality.
This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- 80 PLUS Titanium Efficiency
- Input Voltage Range 90 – 140 / 180 – 264 VAC; 180 – 300 VDC
- Output Voltage 12.2 VDC
- +12.2 VSB (3 A) Standby Output
- Output Power up to 2000 W
- Intel Standard CRPS Form Factor
- Dimensions: 185 x 73.5 x 40 mm (7.28 x 2.89 x 1.57 in)
- High Power Density
- UL/CSA 62368-1, EN/IEC 62368-1 Certified
- Supports N+1 Redundancy, SMART_ON Redundancy, Internal ORing
- Black Box Recorder, Bootloader
- Clockwise and Counter-Clockwise Fan Rotation
- Supports Power Management Bus Communication Protocol

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

Please read our datasheet & drawing disclaimer here.

1 ORDERING INFORMATION

TEC	2000	-	12	-	074	x	A
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
TEC Front-Ends	2000 W		12 V		73.5 mm	N: Normal R: Reverse	A: AC

2 INPUT

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Input Voltage Ranges	Low Line Voltage AC Range (1000 W)	90	100-127	140	V_{RMS}
	Start-up (V_{BROWN_IN})	80	84	88	VAC
	Power Off (V_{BROWN_OUT})	70	74	79	VAC
	High Line Voltage AC Range (2000 W)	180	200-240	264	V_{RMS}
	Start-up (V_{BROWN_IN})	171	175	179	VAC
	Power Off (V_{BROWN_OUT})	159	164	169	VAC
	AC Input Voltage Protection (V_{IN_OVP})	301		318	VAC
	HVDC (2000 W)	180	240	300	VDC
	Start-up (V_{BROWN_IN})	167		175	VDC
	Power Off (V_{BROWN_OUT})	155		165	VDC
	DC Input Voltage Protection (V_{IN_OVP})	330		345	VDC
Input Current	AC Low Line (Nominal) AC High Line (Nominal) at 200~220 VAC (1800 W) at 220~240 VAC (2000 W) HVDC (Nominal)			13 10 10 10	A
AC Line Inrush Current	@ 240 VAC, cold start, duration 1-1200 ms (2000 W)			25	A_{pk}
Leakage Current	@ 264 VAC, 63 Hz			875	µA
Input Frequency		47	50/60	63	Hz
Power Factor	230 / 240 VAC and 50/60 Hz, 10% load	0.90			
	230 / 240 VAC and 50/60 Hz, 20% load	0.96			
	230 / 240 VAC and 50/60 Hz, 50% load	0.98			
	230 / 240 VAC and 50/60 Hz, 100% load	0.99			
Current iTHD (Total Harmonic Distortion)	200 to 240 VAC and 50/60 Hz, > 10% & < 20% load			15	%
	200 to 240 VAC and 50/60 Hz, ≥ 20% load			10	
	200 to 240 VAC and 50/60 Hz, ≥ 40% load			8	
	200 to 240 VAC and 50/60 Hz, ≥ 50% load			5	
Efficiency	230 VAC / 60 Hz, 10% load	90			%
	230 VAC / 60 Hz, 20% load	94			%
	230 VAC / 60 Hz, 50% load	96			%
	230 VAC / 60 Hz, 100% load	91			%
Hold-up Time	70% of rated load	10			ms
$12V_{SB}$ Hold-up Time	@ 100% load	70			ms
AC Line Sag	0 to 1/2 AC cycle (nom AC voltage ranges, 50/60 Hz) No loss of function or performance.		95		%
	> 1 AC cycle (nom AC voltage ranges, 50/60 Hz) Loss of function acceptable, self-recoverable	30			%
AC Line Surge	Continuous (nom AC voltage ranges, 50/60 Hz) No loss of function or performance		10		%
	0 to 1/2 AC cycle (mid-point of nom VAC ranges, 50/60 Hz) No loss of function or performance		30		%
AC Line Isolation	Primary to secondary; reinforced insulation	3000 4242			VAC VDC

NOTES:
1. The standby output may continue to operate when input voltage below V_{BROWN_OUT} range.
2. Brown-in / Brown-Out can be used 100% of rated load only above 1V/s variation of input voltage, otherwise should become 80% of rated load for low slope of Vin.
3. The Iin is specified when the Vin is at nominal condition.
4. The AC voltage considering CF = 1.1, 1.6 should meet the turn on/off point as above.
   Due to many waveforms having the same C.F result, so the all C.F settings in this specification is based on Chroma instrument setting.
5. Either Line or Neutral could be the positive polarity of 240 VDC application.
6. The power supply shall not be damaged when the input voltage is in the range of 265 VAC ~ 300 VAC for a long time.

3 OUTPUT

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Output Voltage			12.2		VDC
Voltage Regulation Limits	± 5 %	+11.59	+12.2	+12.81	V_{RMS}
Max Continuous Output Power				2000	W
Output Current	@ 100 – 127 VAC @ 200 – 220 VAC / 200 – 220 VDC @ 220 – 264 VAC / 220 – 300 VDC	0 0 0		82 148 164	A
Overshoot / Undershoot			± 5		%
Transient Load	Δ Step Load Size, 60% of Load Max, 2200 µF			2.5	A/µs
Capacitive Loading		2200		70000	µF
Output Ripple & Noise	20 MHz BW			120	mVpp
+12 V_{SB} OUTPUT					
+12 V_{SB} Output Voltage			+ 12.2		V_{SB}
Voltage Regulation Limits	± 5 %	+11.59	+12.2	+12.81	V_{RMS}
+12 V_{SB} Output Current		0		3	A
Overshoot / Undershoot			± 5		%
Transient Load	Δ Step Load Size = 1 A, 100 µF			0.5	A/µs
Capacitive Loading		100		3100	µF
Output Ripple & Noise	10 Hz to 20 MHz BW			120	mVpp

3.1 CRPS LOAD REQUIREMENTS

Output	Input Voltage	Output Power (W)	Max. Current Rating (A)	CLST Peak 20 s duration [2] (A)	Pmax. app Peak 10 ms duration [3] (A)	Pmax Peak 100 µs duration [4] (A)	Voltage Regulation
12 V main	100 – 127 VAC	1000	82	Rated + 10 A	Rated + 72 A	Rated + 105 A	Static: 11.8 - 12.6 V Dynamic: 11.6 - 12.8 V
12 V main	200 – 220 VAC 200 – 220 VDC	1800	148	Rated + 10 A	Rated + 72 A	Rated + 105 A	
12 V main	220 – 264 VAC 220 – 300 VDC	2000	164	Rated + 10 A	Rated + 72 A	Rated + 105 A	
12V_{SB} [1]	–	–	3	3.5	NA	NA	12.20 V ± 5%

NOTES:
1. 12Vstby must provide 6.0 A with two power supplies in parallel. The Fan may work when stby current >1.5 A.
2. Close Loop System Throttling (CLST) Peak load duration is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20 seconds without asserting the SMBAlert# signal at maximum operating temperature.
3. Pmax.app peak duty cycle shall be 25%; 4 ms at Pmax.app peak / 12 ms at CLST Peak. Applying a Pmax.app peak load must not trip the SMBAlert# signal. The maximum length of time the Pmax.app peak must be supported is based on the SMBAlert# signal asserting. The PSU must support this peak load for 5 ms after SMBAlert# asserts.
4. Pmax peak must be supported by the PSU based on PMAX Protection requirements that included added system 12V capacitors.

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5 C14 Inlet current de-rating may exceed during low line Peak Current condition.
6 The low line condition max output power should not exceed 1000W.
7 Pmax.app Peak 10 ms 72 A and Pmax Peak 100 µs 105 A is the max current; The Pmax.app Peak and Pmax Peak test allows for an external maximum of 8800 uF ordinary aluminum electrolytic capacitors.

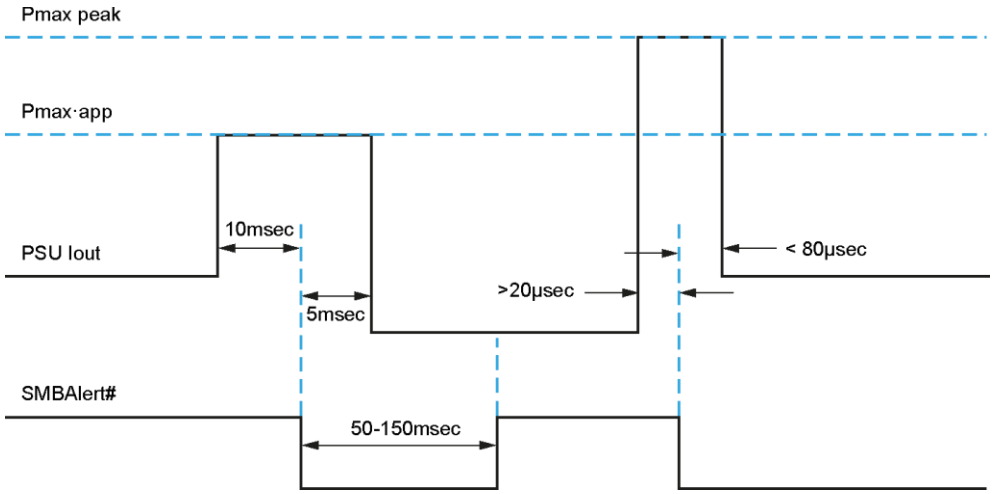

Figure 1. PSU Peak Power Timing

3.2 LOAD SHARE SIGNAL CHARACTERISTICS

The load share signal is only for the load function. The load share signal characteristics can be defined by bel. The delay from output voltages in regulation to load share active with maximum load of one power supply and other power supply in parallel is 100 ms maximum.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
V_{SHARE}; I_{OUT} = Max	Voltage of load share bus at specified maximum output current	7.76	8.0	8.24	V
$\triangle V_{SHARE} / \triangle I_{OUT}$; I_{OUT} > 1 A	Slope of load share bus voltage with changing load		8.00 / I_{MAX} V/A		
I_{SHARE} sink; V_{SHARE} = 4.00 V	Amount of current the load share bus output from each power supply sources.			0.5	mA
I_{SHARE} source V_{SHARE} = 4.00 V	Amount of current the load share bus output from each power supply sinks.	4			mA

4 PROTECTION

4.1 CURRENT LIMIT AND OVER CURRENT PROTECTION (OPP & OCP)

The power supply has a current limit to prevent the outputs from exceeding the values shown in the table below. If the current limits are exceeded the power supply shuts down, the power supply will not be damaged from repeated power cycling in this condition

		THRESHOLDS		TIMING	
PARAMETER	DESCRIPTION	MIN	MAX	MIN	MAX
OPP / Fast OCP [1,4]	Over power protection (voltage foldback then latch after MIN timing)	Rating + 82 A	Rating + 92 A	100 µs	
Slow OCP	Slow over current protection (shutdown and latch after MIN/MAX timing)	Rating + 20 A	Rating + 30 A	20 ms	100 ms
Fast OCW [2]	Fast over current warning (SMBAlert#)	Rating + 72 A	Rating + 82 A	400 µs	800 µs
Slow OCW [3]	Slow over current warning (SMBAlert#)	Rating + 10 A	Rating + 20 A	10 ms	15 ms
OCPstby	Stby over current protection (shutdown, hiccup mode)	3.6 A	4.5 A	1 ms	100 ms

NOTES:

[1] Over power protection mode shall be held for at least 100 µs before OCP shuts down the PSU.

[2] Fast OCW threshold must be set below the OPP / Fast OCP threshold. Fast OCW shall hold the SMBAlert# signal asserted for 50 ms to 150 ms; then de-assert. Fast OCW meet high line AC range is 220 VAC ~ 264 VAC and output power is 2000 W.

[3] Slow OCW threshold must be set below the Slow OCP threshold.

[4] OPP feature is not needed if fast V-mode is present and enabled in the platform. Instead, the PSU shall use this threshold as an Over Current Protection level and shutdown to protect itself.

4.2 OVER AND UNDER VOLTAGE PROTECTION (OVP / UVP)

PARAMETER	DESCRIPTION / CONDITION	PROTECTION MODE	MIN	MAX	UNIT
Over Voltage Protection (OVP)	12 V_{OUT}	Latch-off	13.5	14.5	V
	12 V_{SB}	Recovery	13.5	15.0	V
Under Voltage Protection (UVP)	12 V_{OUT}	Latch-off	10	10.9	V
	12 V_{SB}	Recovery	-	-	V

4.3 OVER TEMPERATURE PROTECTION (OTP)

The power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the 12 V_{SB} remains always on. The OTP circuit has a built-in hysteresis, so that the power supply does not oscillate on and off due to temperature recovering condition. The OTP trip level is a minimum of 5 °C of ambient temperature hysteresis.

PARAMETER	MODEL	TRIGGER POINT	TOLERANCE	UNIT
Over Temperature Warning (OTW)	TEC2000-12-074NA	62	3	°C
Over Temperature Protection (OTP)		65	3	°C
Over Temperature Warning (OTW)	TEC2000-12-074RA	58	3	°C
Over Temperature Protection (OTP)		60	3	°C

NOTES:

1. Internal fan speed control algorithm shall ramp up the fan speed to the maximum prior to the SMBAlert# insertion;
2. The 3°C is Ambient temperature RT1 sensor and Power Management Bus reading tolerance.

4.4 SHORT CIRCUIT PROTECTION (SCP)

A short circuit is considered to be resistance of 50 mΩ or less, applied to any output during start-up or while running will not cause any damage to the power supply (connectors, components, PCB traces, etc.). The power supply shuts down and latches off for short on main outputs but recovers upon PS_ON toggled or AC re-applied.
When the Standby output VSB is shorted the output may go into “hiccup mode”, and all outputs shut down upon a short circuit of the VSB. When the short is removed on VSB, the power supply will recover automatically.

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5 CONTROL

The below table is a TTL signals summary, which presents all the pull-high resistance and pull-up location.

PIN NO.	PIN NAME	PIN TYPE (I/O/A)	ACTIVE	PULL-UP RES. OF PSU (kΩ)	PULL-UP VOL. (V)
A19	SDA	I / O	--	10k/0603	3.3
A20	SCL	I / O	--	10k/0603	3.3
A21	PSON#	I	Low	10	3.3
A22	SMBAlert#	O	Low	10	3.3
A25	PWOK	O	High	0.02	3.3
B19	A0	I	--	10	3.3
B20	A1	I	--	10	3.3
B22	SMART_ON	I / O	High	--	--
B23	12VOUT Load Share Bus	A	--	--	--
B24	PRESENT#	Input	Low	0.1	GND
B25	Vin_good	O	High	2	3.3

5.1 PSON#

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turn on the main power rails. When this signal is not pulled low by the system, or left open, the outputs turn off. The power supply provides an internal pull-up resistor to high. The power supply also provides de-bounce circuitry on PSON# to prevent it from oscillating On/Off at startup when activated by mechanical switch. Provisions for de-bouncing will be included in the PSON# circuitry to prevent the power supply from oscillating on/off at startup

SIGNAL TYPE	PULL-UP TO 3.3 VSB LOCATED IN POWER SUPPLY.	
PSON# = Low	PSU ON	
PSON# = High or Open	PSU OFF	
	MIN	MAX
Logic level low (PSU ON)	0 V	1.0 V
Logic level high (PSU OFF)	2.0 V	3.46 V
Sink current, $V_{PSON\#}$ = low		4 mA

PSON# signal should be logic level low (PSU ON) when the voltage is between 0 V ~ 1 V and becomes logic level high (PSU OFF) when the voltage is between 2.0 V ~ 3.46 V. So, the signal may become logic level low when the voltage is a little higher than 1V and becomes logic level high when the voltage is a little smaller than 2.0V.

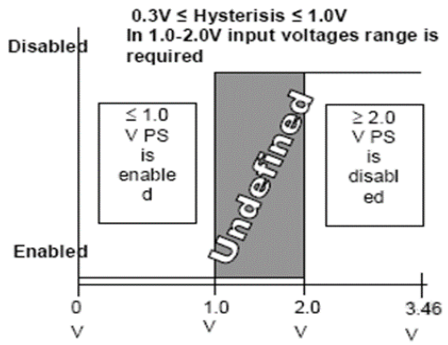

Figure 2. PSON#

5.2 POWER GOOD (PWOK or P_GOOD)

This signal should be asserted high by the power supply to indicate that all outputs are within the regulation. Conversely, this signal should be de-asserted to a low state when any of the DC outputs voltage falls below its under voltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation cannot be guaranteed.

This signal has an internal pull-up resistor to internal 3.3 V sources.

SIGNAL TYPE	PULL-UP TO 3.3 VSB LOCATED IN THE POWER SUPPLY.	
PWOK or P_Good = High	DC Outputs O.K.	
PWOK or P_Good = Low	DC Outputs N.G.	
	MIN	MAX
Logic level low, I_{SINK} = 400 µA	0 V	0.4 V
Logic level high, I_{SOURCE} = 200 µA	2.4 V	3.46 V
Sink current, PWOK = low		400 µA
Source current, PWOK = high		500 µA
PWOK delay: T_{PWOK_ON}	100 ms	500 ms
Power down delay: T_{PWOK_OFF}	1 ms	
PWOK or P_Good rise and fall time		100 µs

5.3 PRESENT#

This pin is tied to Standby return through a resistor. System side should have a pull-up resistor which limits the max current 4mA to go through from this signal pin to the power supply, the pull-down resistor shall be 0 ohm with 1206/0805 package or short PRESENT# to ground directly.

5.4 12V_{OUT} LOAD SHARE BUS

This input / output allows two or more power supplies to share output current between them. If one of the supplies fail the remaining supplies must pick up the entire load without any of the outputs dropping out of regulation. A defective supply that is connected to the output voltage bus will not have an adverse effect on the operation of the remaining function supplies.

TOTAL LOAD	NUMBER OF SUPPLIES	V_{LS} (V) MINIMUM	V_{LS} (V) NOMINAL	V_{LS} (V) MAXIMUM
100%	2	3.8	4	4.2
50%	2	1.8	2	2.2
20%	2	0.64	0.8	0.96
100%	1	7.76	8	8.24
50%	1	3.8	4	4.2
20%	1	1.4	1.6	1.8
0%	1	0	0	0.3

5.5 SHARING ACCURACY

The 12V main has an active load sharing. The failure of a power supply should not affect the load sharing or output voltages of the other supplies and does not cause these outputs to go out of regulation in the system.

SYSTEM LOAD	SHARING ACCURACY
100%	± 3%
50%	± 8%
20%	± 15%

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5.6 SMBAlert#

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal will activate in the case of critical component temperature reached a warning threshold such as OCW / OTW / OCP / OTP. For SMB Alert trigger condition please refer FW Spec in detail. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

SIGNAL TYPE	PULL-UP TO INTERNAL 3.3 V LOCATED IN THE POWER SUPPLY	
SMBAlert# = High	OK	
SMBAlert# = Low	Power Alert to system	
	MIN	MAX
Logical Level Low, ISINK = 4 mA	0 V	0.4 V
Logical Level High, ISOURCE = 50 µA	2.4 V	3.46 V
Sink current, Alert# = low		4 mA
Source current, Alert# = high		50 µA
Alert# fall time		100 µs

5.7 ADDRESS_A0 / A1

This signal is defined by the end user system for Power Management Bus communication, to allocate address of power supply unit in particular slot location. This signal has an internal resistor to internal 3.3 V located in power supply. The address of the power supply unit must be set by user system for Power Management Bus communication reliability.

SIGNAL TYPE	PULL-UP TO INTERNAL 3.3 V LOCATED IN POWER SUPPLY	
	MIN	MAX
Logical Level Low	0 V	0.4 V
Logical Level High	2.4 V	3.46 V

5.8 POWER MANAGEMENT BUS CLOCK_SCL & DATA_SDA

SCL is the SMBus clock input to the supply, SDA is the bi-directional SMBus data path to /from the supply. Both signals have a pull-up resistor to 3.3 V internal located in power supply. The pull-up must be diode isolated to prevent an unpowered/ faulted supply from loading the signal. It must be designed to not glitch bus during hot plug and unplugging. The Power Management Bus operation frequency is 100 kHz. It shall conform to SMBus V2.0 signaling protocol standards. And this specification is based on the Power Management Bus specification parts I and II, revision 1.2. The hardware setting in SDA and SCL is:

Inner Pulled up Resistor to internal 3.3V = 10k ohm / 0603.

Inner Filter MAX capacitor less than 68pF.

Inner serial Resistor (Rs) = 10 ohm / 0603.

NOTE: Once the internal communication between primary and second DSP/MCU fault is detected, the Fan speed shall be run at full speed until the fault is removed.

5.9 REMOTE SENSE + / REMOTE SENSE –

These signals are analog Input / Output $12V_{OUT}$ Main Voltage Sense. Both are analog input / output voltage sense lines to compensate for power path voltage drop. These low level analog signals should be isolated from digital circuit noise. When one or more remote sense lines are opened, regulation measured at the power supply output connector must be maintained within regulation defined, plus or minus an additional 200 mV but no more than 300 mV.

5.10 Vin_good

This signal is an output to indicate AC power is existence and is within operation range. It should act from high to low level within 4 mS only for Vin drops out to zero and input voltage brown-out events. The 4 ms timing is defined as Vin = 0 to V_{in_good} signal low level.

SIGNAL TYPE	PULL-UP 2KΩ TO INTERNAL 3.3 V LOCATED IN POWER SUPPLY	
Vin_good = High	Input voltage is in operating range	
Vin_good = Low	Input voltage is out of operating range	
	MIN	MAX
Logical Level Low, I_{SINK} = 4 mA	0 V	0.4 V
Logical Level High, I_{SOURCE} = 50 µA	2.4 V	3.46 V
Sink current, Vin_good = low		4 mA
Source current, Vin_good = high		50 µA
Vin_good rise and fall time		400 µs

5.11 SMART_ON

This signal is connected to the system board for smart redundant function.
The pin is used in the SMART_ON Redundancy mode control which all of SMART_ON Redundancy Bus signals should be tied together. When the pin is HIGH in the SMART_ON Redundancy mode, the slave power supply will enter the SMART_ON Standby mode sleep mode (sleep mode, +12VDC keeps the voltage and stops the power out); and when the pin is LOW, the SMART_ON Standby mode power supplies will in normal redundancy mode.
SMART_ON Redundancy feature supports 1+1, 2+1, 3+1 and 2+2 redundant configurations. It uses the Power Management Bus manufacturer specific command area to define Power Management Bus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.

5.12 STANDBY TURN-OFF

Following removal of AC power, the Standby output will remain at its steady state value until such time as it begins to decrease in voltage. The decrease will be monotonic in nature dropping to 0.5 V or less. There will be no other perturbations of this voltage at, or following, removal of AC power.

5.13 FAN SPEED CONTROL

The power supply incorporates a 40 x 28 mm^2 fan for cooling the power supply when installed in the system. The airflow direction is from the card edge connector side to the AC inlet side of the power supply (DC->AC) or opposite direction (AC->DC). The Fan speed control must have a close loop algorithm based on both the critical component temperature and the ambient temperature (Inlet temperature). Thus ensure the PSU Fan will always ramp to maximum speed under any condition to protect the power supply from overheating. These conditions include high ambient temperatures, loading, AC input, and airflow impedance.
Under any steady state operating condition (steady state power output level and steady state inlet air temperature), fan oscillation shall be controlled such that associated sound power level variation falls within roughly 10% mean speed.
This condition may be treated as steady state fan speed condition. After the new load and/or cooling condition steady state is established, transition to the steady state fan speed shall take place within 60 seconds.

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5.14 LED INDICATORS

The power supply has a single bi-color (Green-Amber) configuration, the below table shows the behavior of LED states.

POWER SUPPLY CONDITION	LED STATE
12V Output is normal	GREEN
No AC power to all power supplies	OFF
AC present / Only VSB on (PS off)	1 Hz Blink GREEN
Slave PSU is set as active standby mode (SMART_ON Redundant)	1 Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply critical event causing a shutdown; failure, OCP, SCP, OVP, Fan Fail and OTP	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current and slow FAN.	1 Hz Blink AMBER
Power supply FW updating	2 Hz Blink GREEN

5.15 TIMING

These are the timing requirements for the power supply operation. All outputs must rise monotonically. The table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON# held low and the PSON# signal, with the AC input applied.

ITEM	DESCRIPT ION	MIN	MAX
$T_{AC_OFF_Vin_good}$	The time interval between AC Drop to zero to Vin_good signal gets asserted	--	4
$T_{Vin_good_PWOK}$	Vin_good shall be get asserted 1ms prior to PWOK during ac loss event.	1	--
T_{VSB_RISE}	Standby voltage rise time for V_{SB}	5	70
$T_{VSB_ON_DELAY}$	Delay from AC being applied to 12V_{SB} being within regulation.	--	1500
T_{12VOUT_RISE}	Output voltage rises time for 12V_{OUT}	5	70
$T_{AC_ON_DELAY}$	Delay from AC being applied to 12V_{OUT} output voltage being within regulation.	--	3000
T_{12VOUT_HOLDUP}	Time 12V_{OUT} output voltage stays within regulation after loss of AC with specified load on section 3.	11	--
T_{PWOK_HOLDUP}	Delay from loss of AC to de-assertion of PWOK with specified load on section 3.	10	--
$T_{PSON\#_ON_DELAY}$	Delay from PSON# active to output voltages within regulation limits.	5	400
$T_{PSON\#_PWOK}$	Delay from PSON# deactivate to PWOK being de- asserted.	--	5
T_{PWOK_ON}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500
T_{PWOK_OFF}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1	--
T_{PWOK_LOW}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON# signal.	100	--
T_{VSB_12VOUT}	Delay from VSB being in regulation to 12V_{OUT} output voltage being in regulation at AC turn on.	50	1000
T_{VSB_HOLDUP}	Time the V_{SB} standby voltage stays within regulation after loss of AC.	70	--

Units in ms.

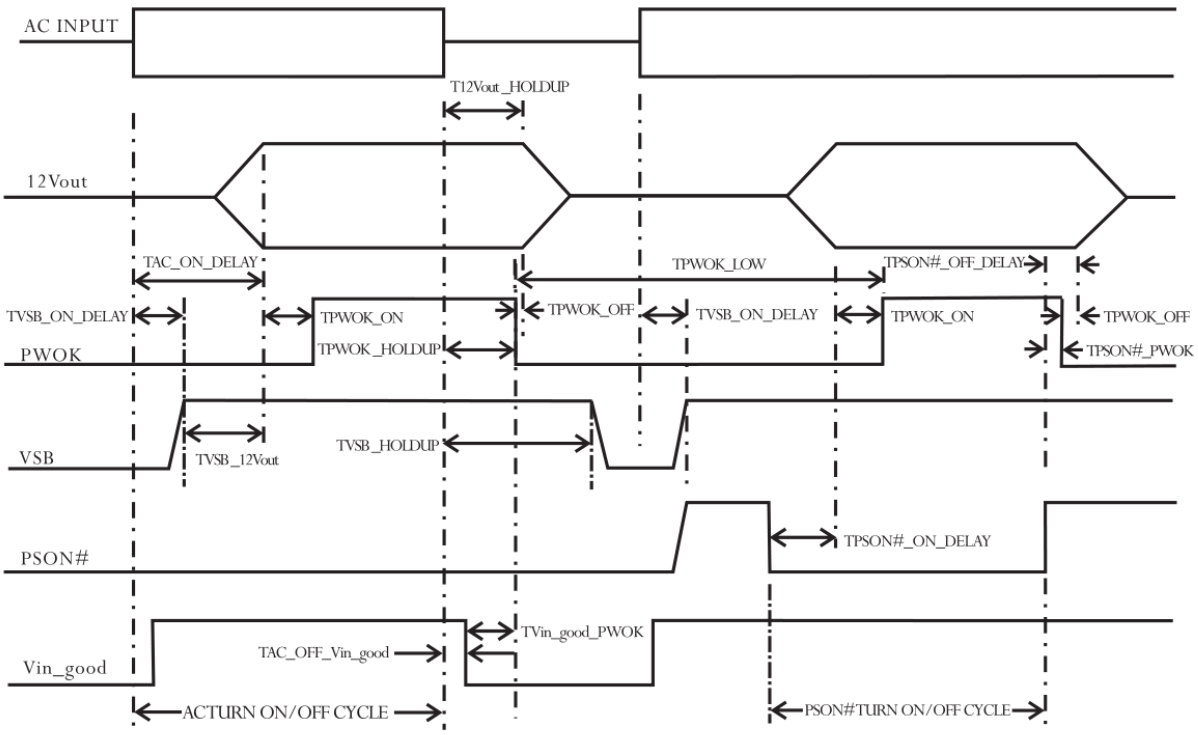

Figure 3. Timing

6 ADDITIONAL REQUIREMENTS

6.1 OTP

The power supply shall incorporate a thermal shutdown feature that turns off all outputs when an over temperature condition occurs, the power supply will not be damaged and will automatically restart when the over temp condition no longer exists. Hysteresis shall be employed to prevent frequent toggling on and off of the outputs, and the hysteresis of OTP shall be greater than 5 Deg-C at least.
The location of the OTP sensor should be on the component(s) most likely to overheat in the event of an abnormal ambient temperature or a blockage of airflow.
In normal operation the OTP cannot activate when the power supply is operated in any of the specified operating conditions of sections 2 and 3.
The OTP must be driven low before or while PWOK is driven low. PWOK must be low for at least 1ms before the main outputs go out of regulation.

6.2 FAN FAIL

The fan(s) is (are) running or the supply is in Standby mode, if there is a fan fault event, the PSU is off and the PWOK must be low for at least 1mS before the main outputs go out of regulation. The main output shall latch-off due to loss fan. When the fan fault occurs under standby mode, and the load is greater than 2.5 A, the standby shall be protection itself due to thermal concern.

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7 FRU REQUIREMENTS

7.1 FRU DATA

For identification of the power supply an internal 256x8 bit EEPROM with Power Management Bus interface is used. The information in the EEPROM follows the IPMI (Platform Management FRU Information Storage Definition) guidelines Document Revision 1.1 from November 15, 1999.

7.2 COMMUNICATION ADDRESS

Four pins will be allocated for the FRU and Power Management Bus information on the Power Supply connector.

One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Two pins are for address lines A0-A1 to indicate the power supply's EEPROM and MCU. which position the power supply is located in the system. The SCL and SDA signals are pulled up by system, the address lines are also pulled up by system.

A1 LOGICAL VOLTAGE	A0 LOGICAL VOLTAGE	PSU ADDRESS	FRU ADDRESS
0	0	0xB0	0xA0
0	1	0xB2	0xA2
1	0	0xB4	0xA4
1	1	0xB6	0xA6

8 POWER MANAGEMENT BUS

8.1 COMMANDS TABLE

The following table shows mandatory Power Management Bus commands to be supported by the PSU.

COMMAND CODE	COMMAND NAME	SMBUS TRANSACTION TYPE:		NUMBER OF DATA BYTES	COMMENT
		Writing Data	Reading Data		
00h	PAGE	Write Byte	Read Byte	1	
01h	OPERATION	Write Byte	Read Byte	1	0x80 ON; 0x00 OFF Default: 0x80
02h	ON_OFF_CONFIG	Write Byte	Read Byte	1	0x1D
03h	CLEAR_FAULTS	Send Byte	N/A	0	
05h	PAGE_PLUS_WRITE	Block Write	N/A	Variable	
06h	PAGE_PLUS_READ	N/A	Block Write – Block Read	Variable	
19h	CAPABILITY	N/A	Read Byte	1	0xB0
1Ah	QUERY	N/A	Block Write – Block Read	1	
1Bh	SMBALERT_MASK	Write Word	Block Write – Block Read	2	
20h	VOUT_MODE		Read Byte	1	0x17 (n=-9)
21h	VOUT_COMMAND	Write Word	Read Word	2	
30h	COEFFICIENTS	N/A	Block Write – Block Read	5	Use for Ein/Eout
31h	POUT_MAX	N/A	Read Word	2	
3Ah	FAN_CONFIG_1_2	Write Byte	Read Byte	1	Default is Duty
3Bh	FAN_COMMAND_1	Write Word	Read Word	2	
4Ah	IOUT_OC_WARN_LIMIT		Read Word	2	
51h	OT_WARN_LIMIT		Read Word	2	
5Dh	IIN_OC_WARN_LIMIT		Read Word	2	
6Ah	POUT_OP_WARN_LIMIT		Read Word	2	
6Bh	PIN_OP_WARN_LIMIT		Read Word	2	
78h	STATUS_BYTE	Write Byte	Read Byte	1	
Bit 6	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC				
Bit 3	VIN_UV				
Bit 2	TEMPERATURE				
Bit 1	CML				
Bit 0	NON OF THE ABOVE				
79h	STATUS_WORD	Write Word	Read Word	2	
Bit 7(H)	VOUT				
Bit 6	IOUT/POUT				
Bit 5	INPUT				
Bit 3	POWER_GOOD#				
Bit 2	FANS				
Bit 6(L)	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC_FAULT				
Bit 3	VIN_UV_FAULT				
Bit 2	TEMPERATURE				
Bit 1	CML				
Bit 0	NON OF THE ABOVE				
7Ah	STATUS_VOUT	Write Byte	Read Byte	1	
Bit 7	VOUT_OV_FAULT				

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Bit 4	VOUT_UV_FAULT				
7Bh	STATUS_IOUT	Write Byte	Read Byte	1	
Bit 7	Iout OC fault				
Bit 5	Iout OC warning				
Bit 1	Pout OP fault				
Bit 0	Pout OP warning				
7Ch	STATUS_INPUT	Write Byte	Read Byte	1	
Bit 5	Vin UV warning				
Bit 4	Vin UV fault				
Bit 3	Unit off for insufficient input				
Bit 1	Iin over current warning				
Bit 0	Pin over power warning				
7Dh	STATUS_TEMPERATURE	Write Byte	Read Byte	1	
Bit 7	OT fault				
Bit 6	OT warning				
7Eh	STATUS_CML	Write Byte	Read Byte	1	
Bit 7	Invalid COMMAND				
Bit 6	Invalid DATA				
Bit 5	PEC Failed				
81h	STATUS_FANS_1_2	Write Byte	Read Byte	1	
Bit 7	Fan 1 fault				
Bit 5	Fan 1 warning				
Bit 3	Fan1 speed overridden				
86h	READ_EIN	N/A	Block Read	6	DIRECT Data Format
87h	READ_EOUT	N/A	Block Read	6	DIRECT Data Format
88h	READ_VIN	N/A	Read Word	2	Linear
89h	READ_IIN	N/A	Read Word	2	Linear
8Bh	READ_VOUT	N/A	Read Word	2	Linear16
8Ch	READ_IOUT	N/A	Read Word	2	Linear
8Dh	READ_TEMPERATURE_1	N/A	Read Word	2	Ambient
8Eh	READ_TEMPERATURE_2	N/A	Read Word	2	SR Hotspot
8Fh	READ_TEMPERATURE_3	N/A	Read Word	2	PFC Hotspot
90h	READ_FAN_SPEED_1	N/A	Read Word	2	In RPM
96h	READ_POUT	N/A	Read Word	2	Linear
97h	READ_PIN	N/A	Read Word	2	Linear
98h	PMBUS_REVISION	N/A	Read Byte	1	1.2
99h	MFR_ID	Block Write	Block Read	Variable (3)	"bel"
9Ah	MFR_MODEL	Block Write	Block Read	Variable (16)	"TEC2000-12-074xA"
9Bh	MFR_REVISION	Block Write	Block Read	Variable (3)	"VXX"
9Ch	MFR_LOCATION	Block Write	Block Read	Variable (8)	"DONGGUAN"
9Dh	MFR_DATE	Block Write	Block Read	Variable (8)	"YYYYMMDD"
9Eh	MFR_SERIAL	Block Write	Block Read	Variable (19)	Serial Number
9Fh	APP_PROFILE_SUPPORT	N/A	Block Read	Variable (2)	PMBus 1.2
A0h	MFR_VIN_MIN	N/A	Read Word	2	90V
A1h	MFR_VIN_MAX	N/A	Read Word	2	264V
A2h	MFR_IIN_MAX	N/A	Read Word	2	
A3h	MFR_PIN_MAX	N/A	Read Word	2	
A4h	MFR_VOUT_MIN	N/A	Read Word	2	11.6V
A5h	MFR_VOUT_MAX	N/A	Read Word	2	12.8V
A6h	MFR_IOUT_MAX	N/A	Read Word	2	
A7h	MFR_POUT_MAX	N/A	Read Word	2	
A8h	MFR_TAMBIENT_MAX	N/A	Read Word	2	
A9h	MFR_TAMBIENT_MIN	N/A	Read Word	2	

AAh	MFR_EFFICIENCY_LL	N/A	Block Read	14	At 20%/50%/100%
ABh	MFR_EFFICIENCY_HL	N/A	Block Read	14	At 20%/50%/100%
B0h	PMBUS_MFR_ CALIBRATION_0xB0	Block Write	Block Read	Variable	
C0h	MFR_MAX_TEMP_1	N/A	Read Word	2	
C1h	MFR_MAX_TEMP_2	N/A	Read Word	2	
C2h	MFR_MAX_TEMP_3	N/A	Read Word	2	
D0h	MFR_SMART_ON_ REDUNDANCY_CONFIG	Write Byte	Read Byte	1	
D4h	MFR_HW_COMPATIBILITY	N/A	Read Word	2	
D5h	MFR_FWUPLOAD_CAPABILITY	N/A	Read Byte	1	
D6h	MFR_FWUPLOAD_MODE	Write Byte	Read Byte	1	
D7h	MFR_FWUPLOAD	Block Write	N/A		
D8h	MFR_FWUPLOAD_STATUS	N/A	Read Word	21	
D9h	MFR_FW_REVISION	N/A	Block Read	3	
DCh	MFR_BLACK_BOX	N/A	Block Read	237	
DDh	MFR_REAL_TIME	Block Write	Block Read	4	
DEh	MFR_SYSTEM_BLACK_BOX	Block Write	Block Read	40	
DFh	MFR_BLACKBOX_CONFIG	Write Byte	Read Byte	1	
E0h	MFR_CLEAR_BLACKBOX	Send Byte	N/A	1	

Note: Write protocol must include PEC (Packet Error Checking).

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8.2 STATUS COMMANDS

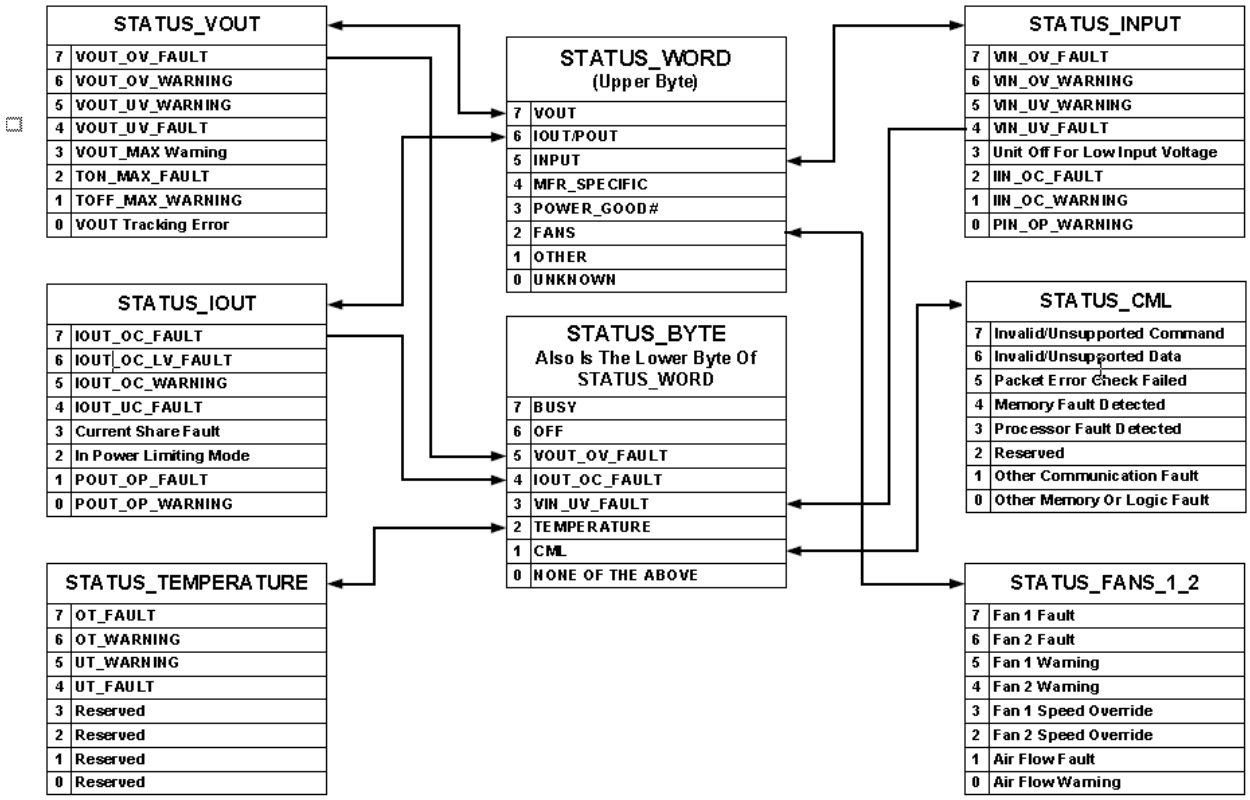

Figure 4. Summary of The Status Registers

The following Power Management Bus STATUS commands shall be supported. All STATUS commands stated in Table 1 Supporting PAGE instances shall support the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_ PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared

The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_W RITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBAlert# signal. The new SMBALERT_MASK command is used to define which status event control the SMBAlert# signal. Default values for these mask bits are shown in the table below.

POWER MANAGEMENT BUS COMMAND	BIT LOCATION	PSU STATE WHEN BIT IS ASSERTED ('1')	INSTANCES NO PAGE'ING2 PAGE 00H = BMC PAGE 01H = ME	SMBALERT_MASK DEFAULTS FOR EACH OF THE THREE INSTANCES (NO PAGE, PAGE 00H, PAGE 01H) 0 = CAUSES ASSERTION OF SMBALERT# 1 = DOES NOT CAUSE ASSERTION OF SMBALERT#
STATUS_WORD			No PAGE, 00h, 01h	
OFF	6 (lower)	OFF		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
CML	1 (lower)	ON		NA
VOUT	7 (upper)	Refer to STATUS_VOUT		NA
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		NA
INPUT	5 (upper)	Refer to STATUS_INPUT		NA
FANS	2 (upper)	Refer to STATUS_FANS		NA
STATUS_VOUT			No PAGE'ing	
VOUT_OV_FAULT	7	OFF		1, 1, 1
VOUT_UV_FAULT	4	OFF		1, 1, 1
STATUS_IOUT			No PAGE'ing, 00h,01h	
IOUT_OC_FAULT	7	OFF		1, 1, 1
IOUT_OC_WARNING	5	ON		1, 1, 0
POUT_OP_FAULT	1	OFF		1, 1, 1
POUT_OP_WARNING	0	ON		1, 1, 1
STATUS_INPUT			No PAGE'ing, 00h,01h	
VIN_UV_WARNING	5	ON		1, 1, 1
VIN_UV_FAULT [1]	4	OFF		1, 1, 0
Unit off for low input voltage	3	OFF		1, 1, 1
IIN_OC_WARNING	1	ON		1, 1, 1
PIN_OP_WARNING	0	ON		1, 1, 1
STATUS_TEMPERATURE			No PAGE'ing, 00h,01h	
OT_FAULT	7	OFF		1, 1, 1
OT_WARNING	6	ON		1, 1, 0
STATUS_FANS_1_2			No PAGE'ing	
Fan 1 fault [3]	7	OFF		1, 1, 1
Fan 1 warning [3]	5	ON		1, 1, 1

Table 1. Power Management Bus STATUS Commands Summary

1 The Vin Fault bit in STATUS_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time; even if the PSU continues to operate normally through a momentary input dropout event.

2 'No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.

3 All fans in the PSU shall be OR'ed into a single fan status bit for fault and warning conditions.

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8.3 POWER MANAGEMENT BUS TEMPERATURE READ COMMANDS

The following temperature read commands as documented by the PMBus specification Part II version 1.2 should be supported.
READ_TEMPERATURE_1(8Dh), should provide the PSU inlet temperature.
READ_TEMPERATURE_2(8Eh), should provide the temperature of the SR heat sink in the PSU.
READ_TEMPERATURE_3(8Fh), should provide the temperature of the PFC heat sink in the PSU.

8.4 PAGE (00h)

Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command.

8.5 OPERATION (01h)

The OPERTION command is used to configure the operational state of the converter, in conjunction with input from the CONTROL pin. The OPERATION command is used to turn the PMBus device output on and off.
Bit [7] controls whether the PMBus device output is on or off.
If Bit [7] is cleared (equals 0) then the output is off. If Bit [7] is set (equals 1), then the output is on.

8.6 ON_OFF_CONFIG (02h)

ON_OFF_CONFIG command Default value is 0x1Dh.

SETTING TYPE	BIT 7~5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DATA VALUE	DESCRIPTION	SUPPORTED
1	000	0	X	X	X	1	0x01	If AC ok, turn-on	YES
2	000	1	0	1	0	1	0x15	HW + LO	YES
3	000	1	1	0	X	1	0x19	SW	YES
4	000	1	1	1	0	1	0x1D	HW + LO + SW	YES

Table 2. ON_OFF_CONFIG

X = don't care HW = turn-on/off by control pin HI = control pin active high turn-on power
LO = control pin active low turn-on power SW = turn-on/off by operation command.

8.7 CLEAR_FAULTS COMMAND (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT# signal output if the device is asserting the SMBALERT# signal.

8.8 PAGE_PLUS_WRITE / PAGE_PLUS_READ COMMANDS (05h/06h)

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_VOUT, and

STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

Reading STATUS commands with PAGE_PLUS_READ Reading STATUS_WORD

Block Write – Block Read Process Call with PEC

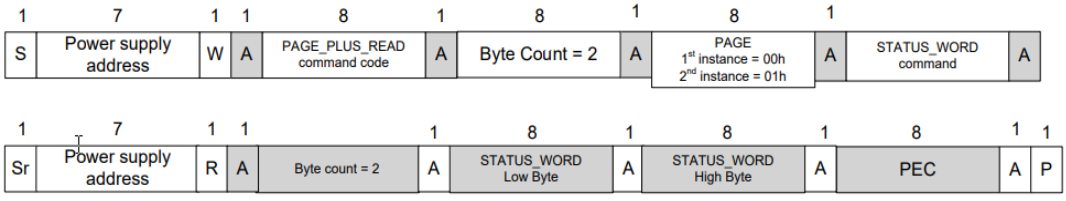

Figure 5. Reading STATUS commands with PAGE_PLUS_READ

Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write – Block Read Process Call with PEC

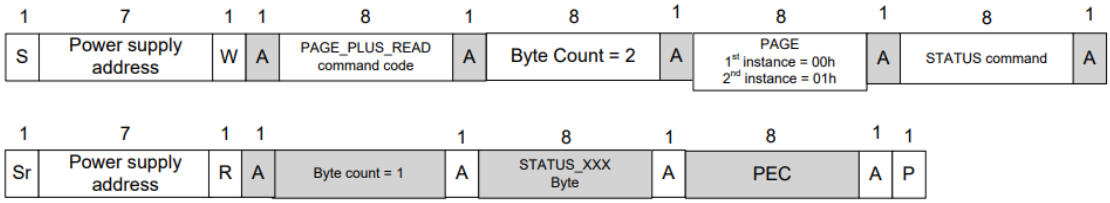

Figure 6. Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML

Clearing STATUS commands (write '1' to clear a bit) STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write with PEC

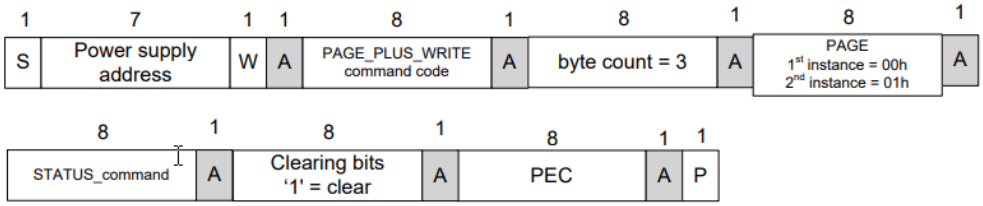

Figure 7. Clearing STATUS commands using PAGE_PLUS_WRITE

8.9 CAPABILITY (19h)

This command provides a way for a host system to determine some key capabilities of a Power Management Bus device. There is one data byte formatted as shown in table below. This command is read only.

BITS	DESCRIPTION	VALUE	MEANING
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
		01	Maximum supported bus speed is 400 kHz
		10	Reserved
		11	Reserved
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol
		1	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol
3:0	Reserved	X	Reserved

Table 3. CAPABILITY COMMAND Data Byte Format

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8.10 QUERY (1Ah)

The QUERY command is used to ask a Power Management Bus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write-Block Read Process Call described in the SMBus specification.

BITS	VALUE	MEANING
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write
	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read
4:2	000	Linear Data Format used
	001	16 bit signed number
	010	Reserved
	011	Direct Mode Format used
	100	8 bit unsigned number
	101	VID Mode Format used
	110	Manufacturer specific format used
	111	Command does not return numeric data. This is also used for commands that return blocks of data.
1:0	XX	Reserved for future use

Table 4. QUERY Command Returned Data Byte Format

If bit [7] is zero, then the rest of the bits are “don’t care”.

8.11 SMBALERT_MASK (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a ‘1’ to the associated STATUS bits. The SMBALERT_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. It is not supported for masking the Non-PAGE’d STATUS_ commands. Below are the protocols.

Reading mask values using PAGE_PLUS
Block Write – Block Read Process Call with PEC

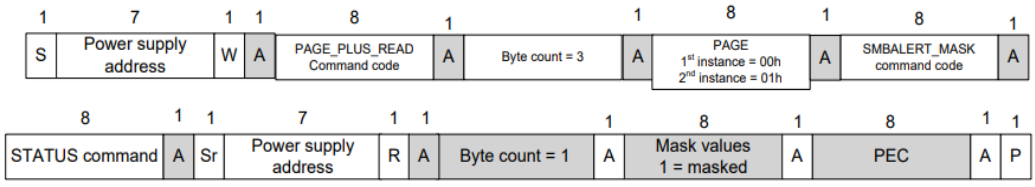
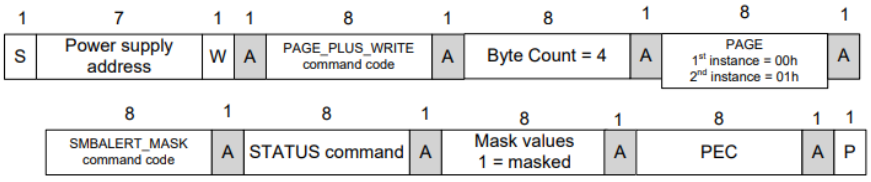


Figure 8. PAGE_PLUS_READ command.

Writing mask values using PAGE_PLUS
Block Write with PEC



STATUS_WORD is not used with SMBALERT_MASK. Only the ‘root’ event bits are used to control the SMBAlert signal

Figure 9. PAGE_PLUS_WRITE command.

8.12 COEFFICIENT (30h)

The power supply shall support the Power Management Bus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN and READ_EOUT accumulated power values.

COMMAND	COEFFICIENTS SUPPORT	M	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h

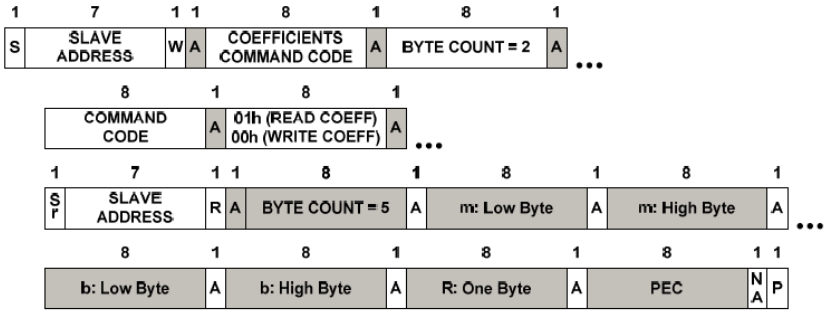


Figure 10. Retrieving Coefficients Using PEC

8.13 FAN_CONFIG_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

The first of the configuration tells the Power Management Bus device whether or not a fan associated with position 1 (or 2) is installed. Any combination of fan installation is permitted.

The second part of the configuration tells the device whether the fan speed commands are in RPM or PWM duty cycle (in percent). These settings do not have to be the same for Fan 1 and Fan 2.

The third part of the configuration data tells the Power Management Bus device the number of tachometer pulses per revolution each fan provides. This information is needed for commanding and reporting fan speed in RPM. Two bits are provided for each fan. These settings do not have to be the same for Fan 1 and Fan 2. The binary values of these bits map to pulses per revolution as follows:

- 00b = 1 pulse per revolution,
- 01b = 2 pulses per revolution,
- 10b = 3 pulses per revolution,
- 11b = 4 pulses per revolution.

This command has one data byte formatted as follows:

BITS	VALUE	MEANING
7	1	Fan in position 1
6	0	Fan 1 commanded in Duty Cycle
	1	Fan 1 commanded in RPM
5:4	00b-11b	Fan 1 Tachometer Pulses Per Revolution
3	0	No fan in position 2
2	Not used	
1:0	Not used	

Table 5. FAN_CONFIG_1_2 Command

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8.14 FAN_COMMAND_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN_COMMAND_1 command. This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU minimum speed of the thermal requirement.

The default control mode of fan is duty (0 ~ 100%).

8.15 READ_FAN_SPEED_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the Power Management Bus linear format.

8.16 POWER MANAGEMENT BUS_REVISION (98h)

This is a correction to the table in the Power Management Bus part II specification regarding the POWER MANAGEMENT BUS_REVISION command.

BITS [7:4]	PART I REVISION	BITS [3:0]	PART II REVISION
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2
0011	1.3	0011	1.3

Table 6. POWER MANAGEMENT BUS_REVISION Command

8.17 MFR-EFFIENCY_LL (AAh)

The MFR_EFFICIENCY_LL command sets or retrieves information about the efficiency of the device while operating at a low line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred to as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power are specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

BYTE NUMBER	BYTE ORDER	DESCRIPTION
0	Low Byte	The input voltage, in volts, at which the low line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power, in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percentage, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer.
13	High Byte	

Table 7. MFR_EFFICIENCY_LL

8.18 MFR-EFFIENCY_HL (ABh)

The MFR_EFFICIENCY_HL command sets or retrieves information about the efficiency of the device while operating at a high line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred to as low, medium and high output power and are transmitted in that order. For example, the low, medium, and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power are specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

BYTE NUMBER	BYTE ORDER	DESCRIPTION
0	Low Byte	The input voltage, in volts, at which the high line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percentage, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer.
13	High Byte	

Table 8. MFR_EFFICIENCY_HL

8.19 READ EIN (86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

	MIN	MAX	DESCRIPTION
Format	Power Management Bus Direct format m = 01h, R = 00h, b = 00h		Power Management Bus data format; refer to Power Management Bus specification for details.
Psample averaging period	4 AC cycles		Period instantaneous input power is averaged over to calculate Psample.
READ_EIN update period	80/66.7 ms (50/60 Hz)		Period at which the power accumulator and sample counter are updated
Range of System polling period	1 sec	100 ms	The PSU shall be polled over this range of rates while testing accuracy.

IMPORTANT:

The PSU READ_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).

Table 9. READ_EIN Requirements Summary

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8.20 READ EOUT (87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

	MIN	MAX	DESCRIPTION
Format	Power Management Bus Direct format m = 01h, R = 00h, b = 00h		Power Management Bus data format; refer to Power Management Bus specification for details.
Psample averaging period	Nominal 50 ms		Period instantaneous input power is averaged over to calculate Psample.
Sampling period	Nominal 50 ms		Period at which the power accumulator and sample counter are updated
System polling rate	1 sample /s	10 samples /s	The PSU shall be polled over this range of rates while testing accuracy.

Table 10. READ_EOUT Requirements Summary

8.21 READ_EIN & READ_EOUT FORMATS

The READ_EIN and READ_EOUT commands shall use the Power Management Bus direct format to report an accumulated power value and the sample count. The Power Management Bus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the Power Management Bus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

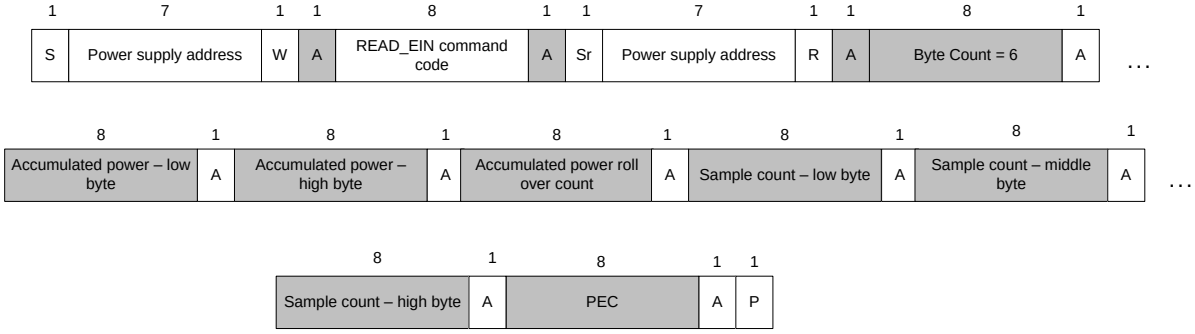

Figure 11. READ_EIN Command

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached (> 7FFFh). The sample count should be incremented to 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

IMPORTANT NOTE:

When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always align with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.

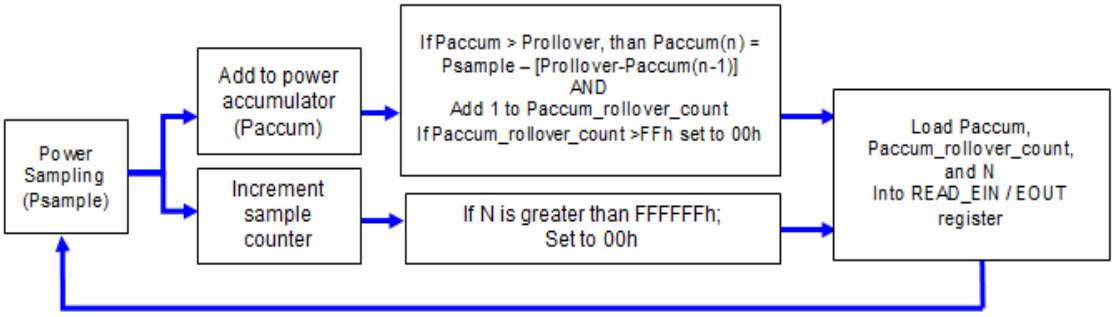

Figure 12. READ_EIN PSU Functional Diagram

VALUE	DESCRIPTION
Psample:	The sampled power value in linear or direct format
Paccum:	2 bytes in Power Management Bus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n)
N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

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8.22 POWER SUPPLY ACCURACY

The following Power Management Bus commands shall be supported for the purpose of monitoring current, voltage, and power. All sensors shall continue providing real time data as long as the Power Management Bus device is powered. This means in standby mode the main output(s) of the PSU shall be zero amps and zero volts. Sensors shall meet requirements at nominal input voltage; maximum deviation for the ambient temperature is +/- 3°C.

	10% ~ <20% Load	≥ 20% ~ 50% Load	> 50% ~ 100% Load
P_{IN}/E_{IN}	± 15 W or ± 5%	± 15 W or ± 5%	± 3%
V_{IN}		± 3%	
I_{IN}	± 0.2 A or ± 5%	± 0.2 A or ± 5%	± 3%
FAN		±500 rpm	
$12V_{OUT}$		± 3%	
I_{OUT}	± 1 A or ± 5%	± 5%	± 3%
P_{OUT}	± 10 W or ± 5%	± 5%	± 3%
AMB Temperature		± 3°C	

Table 11. Power Management Bus Accuracy for AC-DC Models

Note.1: The spec is based on input voltage 115 VAC, 230 VAC and 240 VDC measurement, the Max. output may be different between low and high line, the load definition where is taken Max. value.

Note.2: In 240 VDC application, no matter the input polarity is positive or negative, the PSU could operate normally, but Accuracy shall be measured when positive polarity on Neutral. If a customer may apply positive polarity on either one, please inform bel early.

Note.3: For light load reporting requirement, in the normal redundant application, PSU shall report below value to system once the below condition is set, which is not included the PSU that in SMART_ON redundant mode and set as slave. For system power calculation requirement, the reporting performance shall make sure the Pin > Pout situation,

Note.4: The accuracy of AMB temperature is defined as the temperature around the temperature sensor inside of PSU, thereby this accuracy performance shall measure the closest point on the inlet chassis to internal temperature sensor.

8.23 LINEAR DATA FORMAT

The Linear Data Format is typically used for commanding and reporting the parameters such as (but not only) the following:

- Output Current,
- Input Voltage,
- Input Current,
- Operating Temperatures,
- Time (durations), and Energy Storage Capacitor Voltage.

The Linear Data Format is a two byte value with:

- An 11 bit, two's complement mantissa and,
- A 5 bit, two's complement exponent (scaling factor),

The format of the two data bytes is illustrated in Figure as show below.

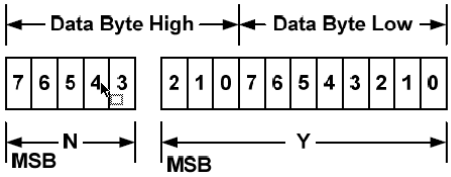

Figure 13. Linear Data Format Data Bytes

The relation between *Y*, *N* and the "real world" value is:
$X = Y \cdot 2^N$

Where, as described above:
X is the "real world" value;
Y is an 11 bit, two's complement integer; and
N is a 5 bit, two's complement integer.

Devices that use the linear format must accept and be able to process any value of *N*.

8.24 VOUT_MODE (20h)

The data byte for the VOUT_MODE command is one byte that consists of a three-bit Mode and a five-bit exponent. The three-bit Mode shall be set to indicate the LINEAR mode for output voltage related commands. The five-bit Exponent shall be set to indicate the value of the five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

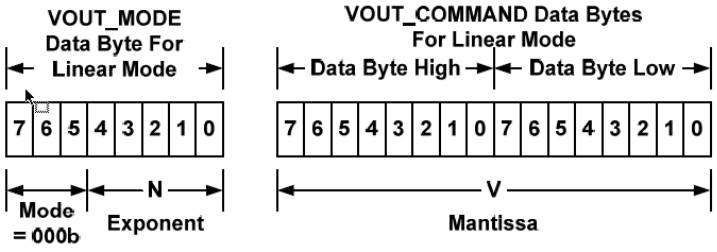

Figure 14. Linear Format Data Bytes

The voltage, in volts, is calculated from the equation Voltage = $V \cdot 2^N$, where:

- V is a 16 bit unsigned binary integer
- N is a 5 bit two's complement binary integer

Sending the VOUT_MODE command with the address set for writing is not supported. If the system sends a VOUT_MODE command for a write, the power supply shall reject the command, and set the Invalid/Unsupported Data bit in the STATUS_CML register.

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9 SMART_ON REDUNDANCY

9.1 OVERVIEW

Below is a block diagram showing the SMART_ON Redundancy architecture. When the power subsystem is in SMART_ON Redundant mode; only the needed power supply to support the best power delivery efficiency are ON. Any additional power supplies, including the redundant power supply, is in SMART_ON Standby state.

Each power supply has an additional signal that is dedicated to supporting SMART_ON Redundancy; SMART_ON_BUS. This signal is a common bus between all power supplies in the system. SMART_ON_BUS is asserted (pulled low) when there is a fault in any power supply OR the power supplies output voltage falls below the Vfault threshold. Asserting the SMART_ON_BUS signal causes all power supplies in SMART_ON Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a Power Management Bus command.

Whenever there is no SMART_ON Redundant active power supply on the SMART_ON Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined SMART_ON Redundant roll (active or SMART_ON Standby). This guarantees that incorrect programming of the SMART_ON Redundancy states of the power supply will never cause the power subsystem to shut down or become overloaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in SMART_ON Redundant Active state or Standard Redundant state to allow the SMART_ON Standby state power supplies to go into SMART_ON Standby state.

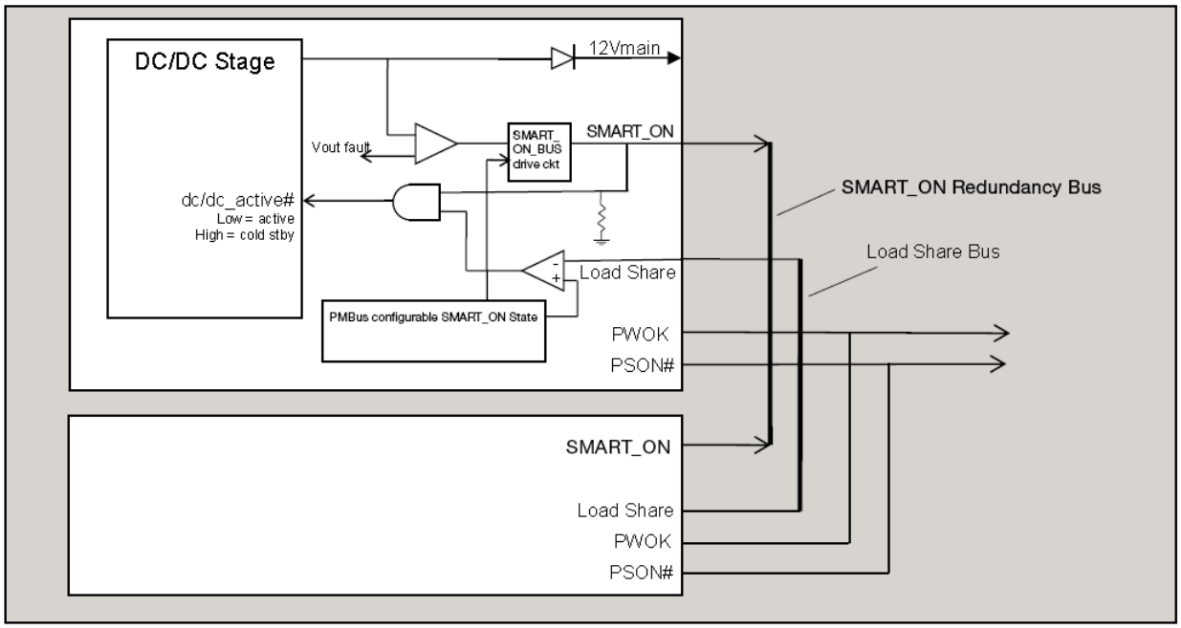

Figure 15. SMART_ON Redundancy 1+1 Functional Block Diagram

SMART_ON_BUS	LOAD SHARE	DC/DC_ACTIVE#	SMART_ON STANDBY POWER SUPPLY STATE(S)
High	< V_{SMART_ON}	High	SMART_ON Standby
Low	< V_{SMART_ON}	Low	Active
High	> V_{SMART_ON}	Low	Active
Low	> V_{SMART_ON}	Low	Active

Table 12. Logic Matrix for SMART_ON Standby Power Supplies

9.2 POWERING ON SMART_ON STANDBY SUPPLIES TO MAINTAIN BEST EFFICIENCY

Power supplies in SMART_ON Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the SMART_ON standby configuration; will slightly change the load share threshold that the power supply shall power on at.

	Enable Threshold for VSMART_ON_EN	Disable Threshold for VSMART_ON_DIS	SMART_ON_BUS De-asserted / Asserted States
Standard Redundancy	N/A; Ignore dc/dc_ active# signal; power supply is always ON		OK = Tri-state Fault = Low
SMART_ON Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
SMART_ON Standby 1 (02h)	3.2 V (40% of max)	90% x (3.2V x 1/2) = 1.44 V	OK = Tri-state Fault = Low
SMART_ON Standby 2 (03h)	5.0 V (62% of max)	90% x (5.0V x 2/3) = 3.01 V	OK = Tri-state Fault = Low
SMART_ON Standby 3 (04h)	6.7 V (84% of max)	90% x (6.7V x 3/4) = 4.52 V	OK = Tri-state Fault = Low

Table 13. Example Load Share Threshold for Activating Supplies

Notes:
Maximum load share voltage = 8.0 V at 100% of rated output power
These are example load share bus threshold; for any power supply these shall be customized to maintain the best efficiency curve that specific model.

9.3 POWERING ON SMART_ON STANDBY SUPPLIES DURING A FAULT OR OVER CURRENT CONDITION

When an active power supply asserts its SMART_ON_BUS signal (pulling it low), all parallel power supplies in SMART_ON standby mode shall power on within 100 µsec.

9.4 SMART_ON REDUNDANCY SMBUS COMMANDS

The Power Management Bus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to SMART_ON redundancy. We will call the command SMART_ON_Redundancy_Config (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

VALUE	STATE	DESCRIPTION
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's SMART_ON_BUS signal shall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in SMART_ON Standby state.
01h	SMART_ON Redundant Active	Defines this power supply to be the one that is always ON in a SMART_ON redundancy configuration.
02h	SMART_ON Standby 1 1	Defines the power supply that is first to turn on in a SMART_ON redundant configuration as the load increases.
03h	SMART_ON Standby 2 1	Defines the power supply that is second to turn on in a SMART_ON redundant configuration as the load increases.
04h	SMART_ON Standby 3 1	Defines the power supply that is third to turn on in a SMART_ON redundant configuration as the load increases.
05h	Always Standby [1]	Defines this power supply to be always in SMART_ON redundant configuration no matter what the load condition.

[1] When the SMART_ON_BUS transitions from a high to a low state; each PSU programmed to be in SMART_ON Standby state shall be put into Standard Redundancy mode (SMART_ON_redundancy_Config = 00h). For the power supplies to enter SMART_ON Redundancy mode the system must re-program the power supplies using the SMART_ON_Redundancy_Config command.

Table 14. SMART_ON_Redundancy_Config (D0h)

9.5 SMART_ON REDUNDANT SIGNALS

There is an additional signal defined supporting SMART_ON Redundancy. This is connected to a bus shared between the power supplies; the SMART_ON_BUS.

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10 BLACK BOX

10.1 BLACK BOX FUNCTION DESCRIPTION

This specification defines the requirements for power supplies with Power Management Bus capability to store Power Management Bus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shutdown. The data can be accessed via the Power Management Bus interface by applying power to the 12Vstby pins. No AC power need to be applied to the power supply.

10.2 WHEN IS DATA SAVED TO THE BLACK BOX?

Data is saved to the Black Box for the following fault events:

- General fault
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

10.3 BLACK BOX EVENTS

There are two types of data saved in the black box:

1) System Tracking Data.
2) Power supply event data.

System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

10.4 BLACK BOX PROCESS

- System writes system tracking data to the power supply RAM at power ON.
- System writes the real time clock data to the PSU RAM once every ~5 minutes.
- Power supply tracks the number of PSON# and AC power cycles in EEPROM.
- Power supply tracks ON time in EEPROM
- Power supply loads warning and fault event counter data from EEPROM into RAM
- Upon a warning event, the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM
- Upon a fault event that causes the PSU to shut down all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON# power cycles, PSU ON time, warning event counters and fault event counters.

10.5 RELATED COMMAND OF BLACK BOX

The following command set will be used for Black Box function via the Host System. The commands and protocol used by the Host System and shall be implemented by the microcontroller are defined by this document.

COMMAND CODE	COMMAND NAME	SMBUS TRANSACTION TYPE	NUMBER OF DATA BYTES	REMARK
DCh	MFR_BLACK_BOX	Read only (7)	237	Read the data of the Black box.
DDh	MFR_REAL_TIME	Read/Write (6/7)	4	Read/Write the data of MFR real time.
DEh	MFR_SYSTEM_BLACK_BOX	Read/Write (6/7)	40	Read/Write the data of MFR system black box.
DFh	MFR_BLACKBOX_CONFIG	Read/Write (2/3)	1	Read/Write the data of MFR black box configure.
E0h	MFR_CLEAR_BLACKBOX	Write only (1)	1	Send one byte to clear all data of black box.

1) Command Name: MFR_BLACKBOX

Format: Read Block with PEC (237 bytes)

Code: DCh

	ITEM	NUMBER OF BYTES	DESCRIPTION
System Tracking Data	System top assembly number	10	The system will write its Intel part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCII characters.
	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCII characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON# asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON# power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these time and power cycle counters in RAM. When a black box event occurs, the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System (reserved for future use)	4	This time stamp does not need to be generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON# power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply.
Power Management Bus			The power supply shall save these Power Management Bus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the Power Management Bus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	

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	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. These values shall be saved to the black box when a black box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	
	Input voltage warning; no shutdown	Lower ½	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
Power supply event data (N-1)		38	
Power supply event data (N-2)		38	
Power supply event data (N-3)		38	
Power supply event data (N-4)		38	

2) Name: MFR_REAL_TIME_BLACK_BOX

Format: Write/Read Block with PEC (4 bytes)

Code: DDh

The system shall use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSIC.

3) Name: MFR_SYSTEM_BLACK_BOX

Format: Write/Read Block with PEC (40 bytes). Low byte first.

Code: DEh

The system uses this command to write the following data to the PSU.

Item	Bytes	
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

1)

4) Name: MFR_BLACKBOX_CONFIG

Format: Read/Write Byte with PEC

Code: DFh

BIT	VALUE	DESCRIPTION
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. Intel shall receive the power supply with the black box function enabled; bit 0 = '1'.
1-7		Reserved

5) Name: MFR_CLEAR_BLACKBOX

Format: Send Byte with PEC

Code: E0h

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously.

This command is write only. There is no data byte for this command.

10.6 HARDWARE REQUIREMENTS

The SMBus interface shall be used to access the Black Box data. It may be accessed when the power supply is ON or in standby mode. It also may be accessed when no AC power is applied, and power is only applied at the standby output pins by an external source (12Vstby).

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11 BOOTLOADER

11.1 FUNCTION DESCRIPTION

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). It is desired that any other microcontroller in the power supply also be able to be updated with this same process (example: primary side microcontroller); however, this is not a requirement at this time.

11.2 FW IMAGE MAPPING

The power supply firmware image shall be made up of two parts; 1) Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1) Boot Loader:
This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling, and protections (UV, OV, OC).

2) Main Program:
This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

11.3 POWER SUPPLY OPERATING MODE DURING AND AFTER FIRMWARE UPDATE

1) Firmware update mode in ON state with no power cycle needed:
Power supply may be able to support FW upload in the ON state. The new FW will take effect once it is taken out of FW upload load.

2）Bad image after firmware update:
The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

11.4 TEC2000-12-074NA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	T	Model Name 13 bytes
Byte 12	E	
Byte 13	C	
Byte 14	2	
Byte 15	0	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	N	
Byte 22	A	
Byte 23		
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes, in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

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11.5 TEC2000-12-074RA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	T	Model Name 13 bytes
Byte 12	E	
Byte 13	C	
Byte 14	2	
Byte 15	0	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	R	
Byte 22	A	
Byte 23		
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes, in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

11.6 FIRMWARE UPDATE PROCESS

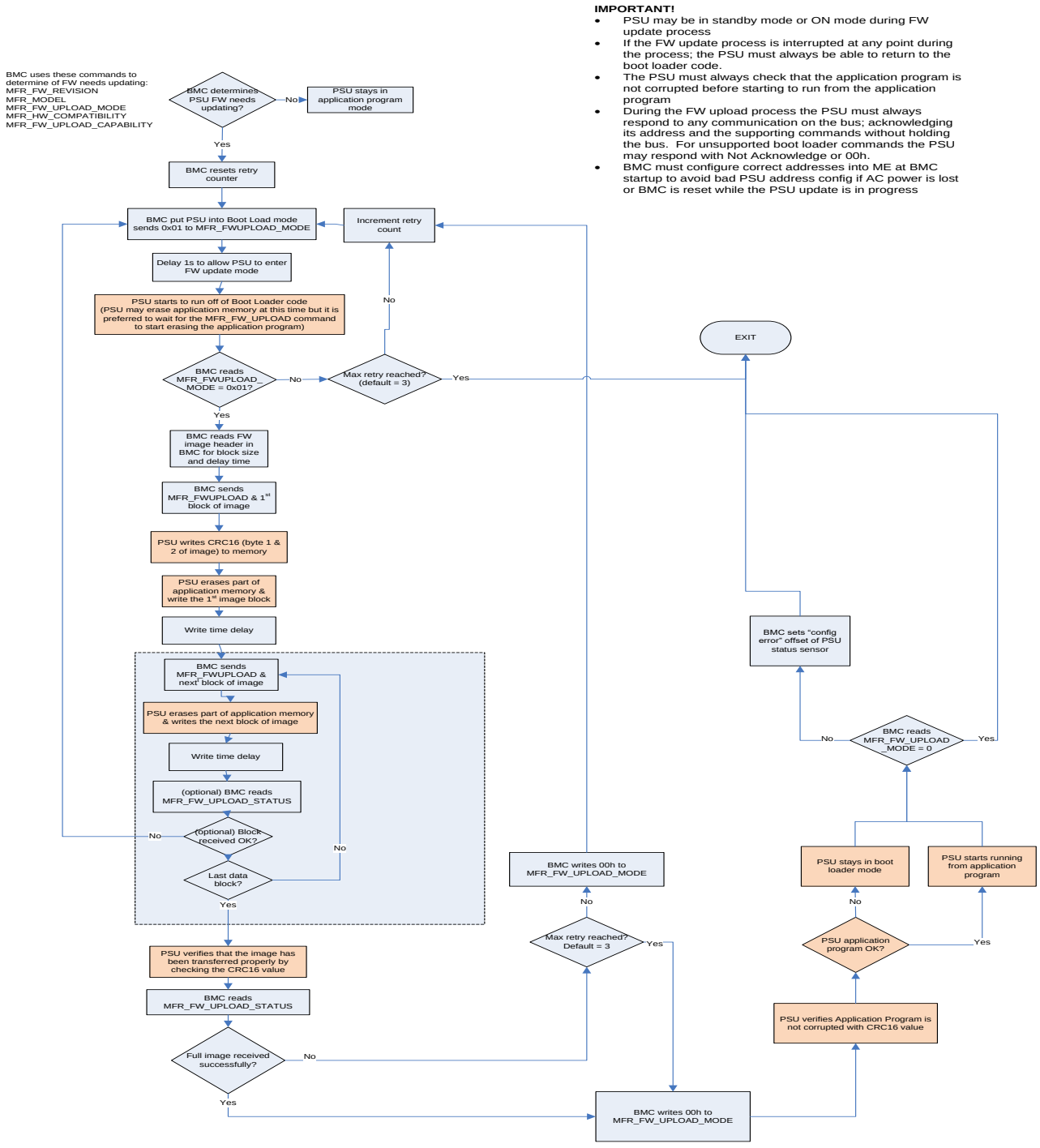

Figure 16. PSU Upload Process

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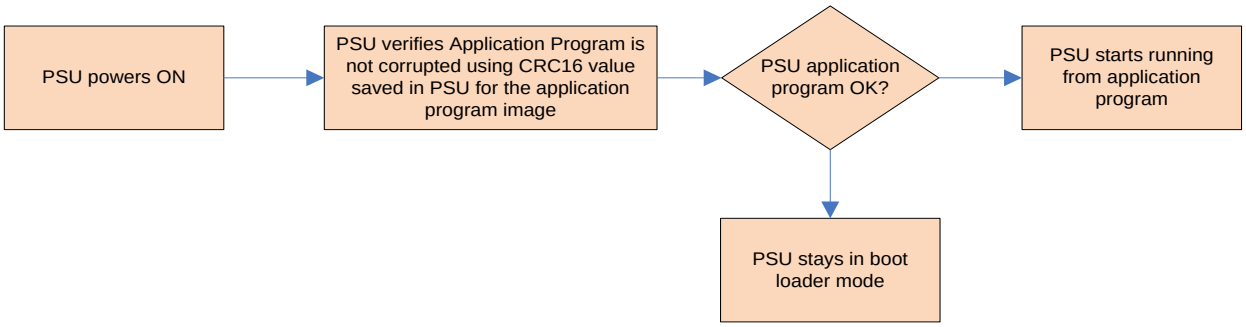

Figure 17. PSU flow during powering ON

11.7 RELATED COMMAND OF BOOTLOADER

1) Name: MFR_HW_COMPATIBILITY

Format: Read Word

Code: D4h

BYTES	VALUE	DESCRIPTION
low	ASCII code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCII code for second letter/number of the PSU HW compatibility.	

2) Name: MFR_FWUPLOAD_CAPABILITY

Format: Read Byte

Code: D5h

The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

BIT	VALUE	DESCRIPTION
0 (for future use)	1 = PSU support FW uploading in standby mode only	For future use
1 (for future use)	1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON#.	For future use
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

3) Name: MFR_FWUPLOAD_MODE

Format: Read/Write Byte

Code: D6h

BIT	VALUE	DESCRIPTION
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7		Reserved

4) Name: MFR_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

Code: D7h

BYTES	VALUE	DESCRIPTION
Block size defined in header	Image header & image data	Command used to send each block of the FW image. Header should follow the format described in section 11.4 (NA) and 11.5 (RA). The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

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5) Name: MFR_FWUPLOAD_STATUS

Format: Read Word

Code: D8h

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.
Reset: all bits get reset to '0' when the power supply enters FW upload mode.

BIT	DESCRIPTION
0	1 = Full image received successfully
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3 (for future use)	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.
4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5 – 15	Reserved

6) Name: MFR_FW_REVISION

Format: Block Read, 3 bytes

Code: D9h

BYTE	VALUE	DESCRIPTION
0	0 - 255	Minor revision; secondary
1	0 - 255	Minor revision; primary
2	0 - 255	Bit 7: 1-> Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed but recommended to follow. 0→ No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision

7) MFR_MODEL (existing Power Management Bus command)

Code: 9Ah

Maximum of 12 byte value; ending in terminator character.

8) MFR_REVISION (existing Power Management Bus command)

Code: 9Bh

12 ELECTROMAGNETIC COMPATIBILITY

12.1 IMMUNITY

The power supply complies with the limits defined in EN 55024.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Electrostatic Discharge	IEC / EN 61000-4-2; 15 kV air discharge, 8 kV Contact discharge	A
Radiated Immunity	IEC / EN 61000-4-3; 80 ~1000 MHz, 10V/m	A
Fast Transient / Burst	IEC / EN 61000-4-4; AC Power Port: 1 kV 2 kV	A B
Surge Immunity	IEC / EN 61000-4-5; 2 kV line to ground and 2 kV line to line	A
Conducted Susceptibility	IEC / EN 61000-4-6; 0.15 ~ 80 MHz, 10 Vrms	A
Power Frequency Magnetic Immunity	IEC / EN 61000-4-8; 50 Hz or 60 Hz, 1 A/m	A
Voltage Dips and Interruptions	IEC / EN 61000-4-11 ; >95% reduction for 0.5 period, 30% reduction for 25 period, >95% reduction for 250 period	B

12.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted & Radiated Emissions	EN 55032 / CISPR32 (at 100 - 120, 200 – 240 VAC / 50 Hz)	Class A 6 dB margin
Power Harmonics	EN 61000-3-2	Class A
Voltage Fluctuation and Flicker	EN 61000-3-3	Class A

13 SAFETY / APPROVALS

PARAMETER	DESCRIPTION / CONDITION	STATUS
Agency Approvals	• UL / CSA 62368-1 (USA / Canada) • EN / IEC 62368-1 (Europe / International) • CB Certificate & Report, IEC 62368-1 (Report includes all country national deviations)) • CE – Low Voltage Directive 2006/95/EC (Europe) • Nordics – EMKO-TSE (74-SEC) 207/94 • GB4943.1 – CNCA Certification (China)	
Leakage Current	875 µA @ 264 VAC, 63 Hz	

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14 ENVIRONMENTAL

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
Ambient Temperature	Operating	TEC2000-12-074NA TEC2000-12-074RA	-5 -5		+50 +50	°C
	Non-Operating		-40		+85	
Humidity	Operating, relative (non-condensing)		5		85	%
	Non-Operating, relative (non-condensing)				95	
Altitude [1]	Operating		-50		5 000	m
	Non-Operating		-50		50 000	ft
Mechanical Shock (non-operating)	50 G Trapezoidal Wave, Velocity change = 170 in. / sec					
Vibration (non-operating) sine sweep	5 Hz to 500 Hz at 0.5 g RMS at 0.5 octave/min. dwell 15 min. at each of 3 resonant points					
Vibration (non-operating) random	5Hz at 0.01g²/Hz to 20 Hz at 0.02g²/Hz (slope up). 20 Hz to 500 Hz at 0.02g²/Hz (flat) Input acceleration = 3.13gRMS; 10 min. per axis for 3 axes on all samples					
Thermal Shock (non-operating)	Transition time not to exceed 5 minutes. Duration of exposure to temperature extremes will be 20 min.		-40		+70	°C
Acoustic Noise	@ 100% rated DC load and inlet T_A = 25°C				70	dB

[1] The system ambient supports at 950 m (3000 feet) altitude. Maximum operating temperature is de-rated 1°C per 125 m above 950 m.

15 RELIABILITY

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
CMTBF	T_A = 50°C, 80% load	200			kh

16 MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions (W x H x L)			73.5 x 40.0 x 185 2.89 x 1.57 x 7.28		mm in
Weight			740		g

16.1 AIRFLOW DIRECTION

The normal airflow direction (NA): intake from DC connector side and exhaust from the AC connector side of the power supply
The reverse airflow direction (RA): intake from the AC connector side and exhaust from the DC connector side of the power supply.

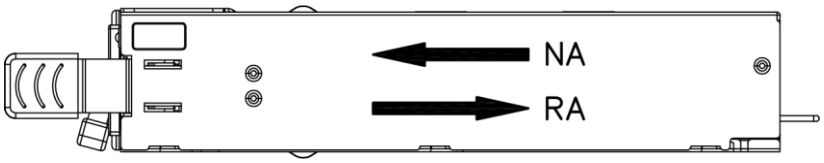

Figure 18. Airflow Direction

16.2 HANDLE RETENTION

The power supply has a handle to assist extraction. The module can be inserted and extracted without the assistance of tools.
The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is plugged into the power supply.
The handle shall protect the operator from any burn hazard and be designed as a plastic handle or equivalent material.

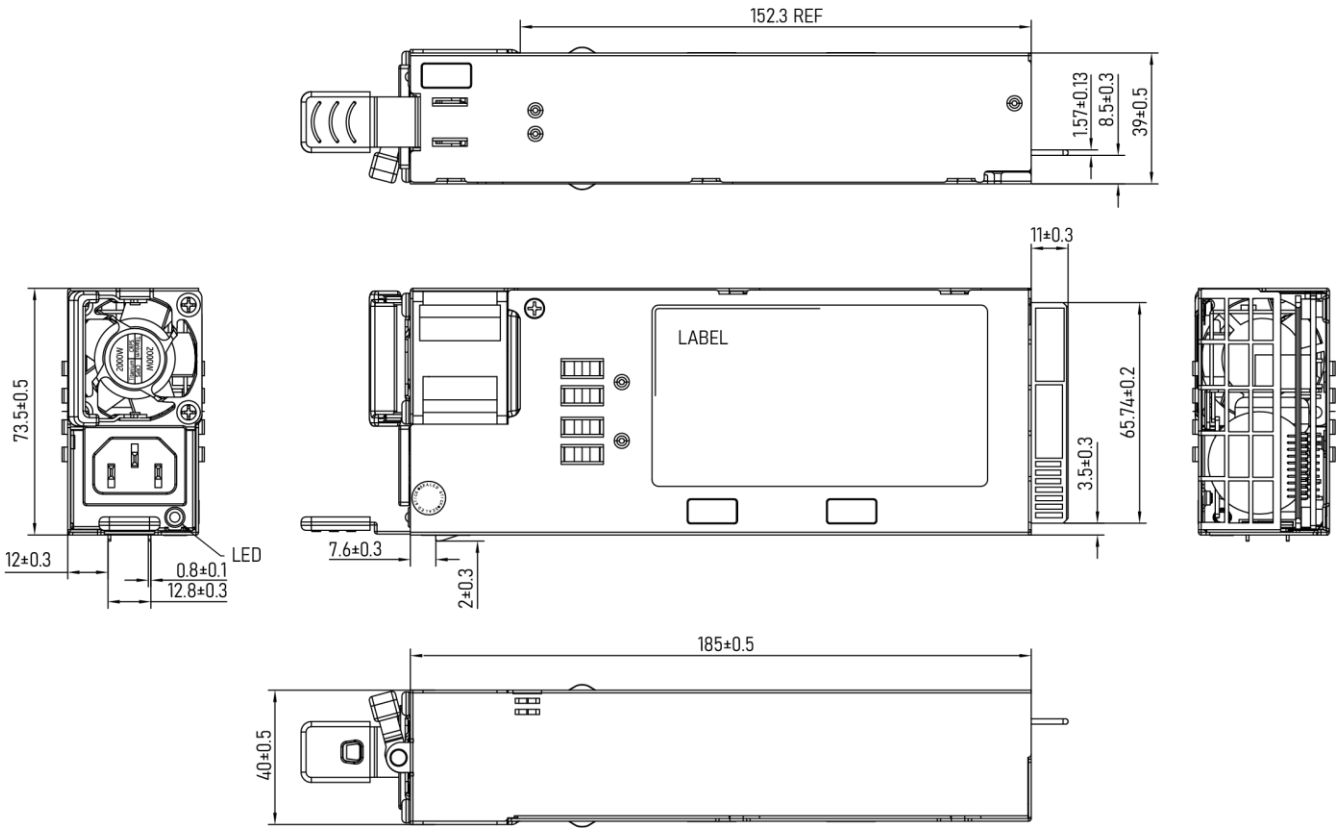

Figure 19. Mechanical Drawing

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17 CONNECTORS

17.1 AC INPUT CONNECTOR

The AC input receptacle is an IEC-320 type C14 capable of at least 10 A at 120 VAC rating and 10 A at 250 VAC rating.

17.2 DC OUTPUT CONNECTOR PIN LOCATIONS

The power supply uses a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the FCI power card connector 10035388-102LF or OUPIIN power card connector 9393-F4P50N11ACB30DA.

PIN NO.	PIN NAME	PIN TYPE	PIN LENGTH	DESCRIPTION
A1~A9 B1~B9	GND	12 V_{OUT} main & V_{SB} Return	Long	12V_{OUT} main & VSB Return
A10~A18 B10~B18	12V_{OUT}	12 V_{OUT} main output	Standard	12V_{OUT} main output
A19	SDA	I / O	Short	SMBus / Power Management Bus Data
A20	SCL	I / O	Short	SMBus / Power Management Bus Clock
A21	PSON#	Input	Short	Active low; 12V_{OUT} main output on/off control
A22	SMBAlert#	Output	Short	Active low; I2C alert signal (interrupt)
A23	RETURN Sense	Analog Input	Standard	12V_{OUT} main output Remote Sense -
A24	12V_{OUT} Remote Sense	Analog Input	Standard	12V_{OUT} main output remote sense +
A25	PWOK	Output	Standard	Active high; indicate 12V_{OUT} main is valid
B19	A0	Input	Standard	Power Management Bus address 0
B20	A1	Input	Standard	Power Management Bus address 1
B21	12V Standby VSB	Aux Power	Standard	Standby voltage
B22	SMART_ON	I / O	Standard	SMART_ON Redundancy Bus
B23	12VOUT Load Share Bus	Analog Output	Standard	12VOUT main output load current sharing
B24	PRESENT#	Input	Short	Power Supply Present
B25	Vin_good	Output	Short	Indicate the status of input voltage

18 FRU DATA

18.1 TEC2000-12-074NA FRU DATA

ITEM	1	BYTE VALUE		DESCRIPTION	BLOCK TITLE
		DEC	HEX		
1	0000H	1	01	COMMON HEADER FORMAT VERSION	COMMON HEADER
2	0001H	0	00	INTERNAL USE AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present	
3	0002H	0	00	CHASSIS INFO AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present.	
4	0003H	0	00	BOARD AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present.	
5	0004H	1	01	PRODUCT INFO AREA STARTING OFFSET (In Multiples Of 8 Bytes).	
6	0005H	11	0B	MULTIRECORD AREA STARTING OFFSET (In Multiples Of 8 Bytes).	
7	0006H	0	00	PAD, Write As 00H	
8	0007H	243	F3	COMMON HEADER CHECKSUM (ZERO CHECKSUM)	
1	0008H	1	01	PRODUCT AREA FORMAT VERSION 7:4 - Reserved, Write As 0000B 3:0 - Format Version Number = 1H	PRODUCT INFORMATION AREA
2	0009H	10	0A	PRODUCT AREA LENGTH (In multiples of 8 bytes)	
3	000AH	25	19	LANGUAGE CODE (ENGLISH)Z	
4	000BH	200	C8	MANUFACTURER NAME TYPE / LENGTH (C8H) 7:6 - Type Code 5:0 - Number Of Data Bytes.	
5	000CH	98	62	b	
6	000DH	101	65	e	
7	000EH	108	6C	l	
8	000FH	32	20		
9	0010H	32	20		
10	0011H	32	20		
11	0012H	32	20		
12	0013H	32	20		
13	0014H	208	D0	PRODUCT NAME Type/Length (CEh) 7:6 - Type Code 5:0 - Number Of Data Bytes.	MANUFACTURER'S MODEL NUMBER
14	0015H	84	54	T	
15	0016H	69	45	E	
16	0017H	67	43	C	
17	0018H	50	32	2	
18	0019H	48	30	0	
19	001AH	48	30	0	
20	001BH	48	30	0	
21	001CH	45	2D	-	
22	001DH	49	31	1	
23	001EH	50	32	2	
24	001FH	45	2D	-	
25	0020H	48	30	0	
26	0021H	55	37	7	
27	0022H	52	34	4	
28	0023H	78	4E	N	
29	0024H	65	41	A	
30	0025H	212	D4	PRODUCT PART/MODEL NUMBER Type/Length (D4h)	CUSTOMER PART NUMBER
31	0026H	67	43	C	
32	0027H	82	52	R	
33	0028H	80	50	P	
34	0029H	83	53	S	
35	002AH	50	32	2	
36	002BH	48	30	0	

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37	002CH	48	30	0	
38	002DH	48	30	0	
39	002EH	45	2D	-	
40	002FH	65	41	A	
41	0030H	72	48	H	
42	0031H	32	20		
43	0032H	32	20		
44	0033H	32	20		
45	0034H	32	20		
46	0035H	32	20		
47	0036H	32	20		
48	0037H	32	20		
49	0038H	32	20		
50	0039H	32	20		
51	003AH	195	C3	PRODUCT VERSION NUMBER Type/Length (C3h)	CUSTOMER CURRENT REVISION
52	003BH	86	56	V	To be updated
53	003CH	48	30	0	To be updated
54	003DH	48	30	0	To be updated
55	003EH	211	D3	PRODUCT SERIAL NUMBER type/length byte (D3)	
56	003FH	84	54	T	To be updated
57	0040H	69	45	E	To be updated
58	0041H	67	43	C	To be updated
59	0042H	50	32	2	To be updated
60	0043H	48	30	0	To be updated
61	0044H	48	30	0	To be updated
62	0045H	48	30	0	To be updated
63	0046H	78	4E	N	To be updated
64	0047H	65	41	A	To be updated
65	0048H	89	59	Y	To be updated
66	0049H	89	59	Y	To be updated
67	004AH	77	4D	M	To be updated
68	004BH	77	4D	M	To be updated
69	004CH	88	58	X	To be updated
70	004DH	88	58	X	To be updated
71	004EH	88	58	X	To be updated
72	004FH	88	58	X	To be updated
73	0050H	88	58	X	To be updated
74	0051H	0	00		To be updated
75	0052H	192	C0	FRU FILE ID Type/Length Byte	Not used, code is zero length byte
76	0053H	192	C0	FRU FILE ID Type/Length Byte	Not required
77	0054H	193	C1	ENCODED TO INDICATE NO MORE INFO FIELDS	
78	0055H	0	00	PAD (Always Zero)	
79	0056H	0	00	PAD (Always Zero)	
80	0057H	138	8A	CHECKSUM (100H-(LOWER BYTE(SUM OF BYTES)))	To be updated
1	0058H	0	00	RECORD TYPE ID 0x00 =POWER SUPPLY INFORMATION	MULTI RECORD AREA
2	0059H	2	02	7:7 END OF LIST ,6:4=000B, 3:0 RECORD FORMAT VERSION=2	
3	005AH	24	18	RECORD LENGTH OF MULTIRECORD	
4	005BH	65	41	RECORD CHECKSUM (ZERO CHECKSUM)	
5	005CH	165	A5	HEADER CHECKSUM (ZERO CHECKSUM)	
1	005DH	208	D0	15-12:RESERVED,WRITE AS 0000B	2000W
2	005EH	7	07	11-0:OVERALL CAPACITY(WATTS)	
3	005FH	96	60	PEAK VALUE	

4	0060H	9	09	LSB FIRST	2400W
5	0061H	25	19	INRUSH CURRENT ,FFH IF NOT SPECIFIED	25A
6	0062H	5	05	INRUSH INTERVAL IN MS.	5mS
7	0063H	16	10	LOW END INPUT VOLTAGE RANGE 1 100V=2710H	100V
8	0064H	39	27		
9	0065H	156	9C	HIGH END INPUT VOLTAGE RANGE 1 127V=319CH	127V
10	0066H	49	31		
11	0067H	32	20	LOW END INPUT VOLTAGE RANGE 2 200V=4E20H	200V
12	0068H	78	4E		
13	0069H	192	C0	HIGH END INPUT VOLTAGE RANGE 2 240V=5DC0H	240V
14	006AH	93	5D		
15	006BH	50	32	LOW END INPUT FREQUENCY RANGE 50HZ=32H	50Hz
16	006CH	60	3C	HIGH END INPUT FREQUENCY RANGE 60HZ=3CH	60Hz
17	006DH	10	0A	A/C DROPOUT TOLERANCE IN mS 10mS=0AH	10mS
18	006EH	30	1E	7-5:RESERVED,WRITE AS 000B 4:TACHOMETER PULSES PER POTATION/PREDICTIVE FALL POLARITY YES=1(FAIL=1,PASS=0) 3:HOT SWAP/REDUNDANCY SUPPORT YES=1 2:AUTOSWITCH YES=1 1:POWER FACTOR CORRECTION YES=1 0:PREDICTIVE FALL SUPPLY YES=1	
19	006FH	52	34	PEAK WATTAGE 15-12:HOLD UP TIME IN SECONDS 1S=1H	
20	0070H	248	F8	11-0 PEAK CAPACITY (WATTS)(LSB FIRST) 2100W=0834H	15S
21	0071H	0	00	COMMBINED WATTAGE 7-4:Voltage 1 3-0:Voltage 2=00H	
22	0072H	0	00	BYTE 2:3 TOTAL COMBINED WATTAGE (LSB FIRST) W=0000H	0
23	0073H	0	00	BYTE 2:3 TOTAL COMBINED WATTAGE (LSB FIRST) W=0000H	
24	0074H	16	10	PREDICTIVE FAIL TACHOMETER LOWER THRESHOLD(PRM/60)1000/60=16	
1	0075H	10	0A	RECORD TYPE ID 0X01 =DC OUTPUT Record	MULTIRECORD
2	0076H	2	02	7:7 END OF LIST 6:4=000 3:0 RECORD FORMAT VERSION=2	HEADER
3	0077H	13	0D	RECORD LENGTH OF MULTIRECORD	
4	0078H	212	D4	RECORD CHECKSUM	
5	0079H	19	13	HEADER CHECKSUM	
1	007AH	1	01	+12V 7:STANDBY=0,6-4:RESERVED 000B , 3-0:OUTPUT UMBER=0001B	+12V
2	007BH	196	C4	NOMINAL VOLTAGE(10mV)1220=04C4H	12.2V
3	007CH	4	04		
4	007DH	135	87	MAXIMUM NEGATIVE VOLTAGE DEVIATION(10mV) 1159=0487H	11.59V
5	007EH	4	04		
6	007FH	1	01	MAXIMUM POSITIVE VOLTAGE DEVIATION(10mV) 1281=0501H	12.81V
7	0080H	5	05		
8	0081H	120	78	RIPPLE AND NOISE PK-PK 10Hz TO 20MHz(mV) 120mV=0078H	120mV
9	0082H	0	00		
10	0083H	10	0A	MINIMUM CURRENT DRAW(10mA)	0.1A
11	0084H	0	00		
12	0085H	16	10	MAXIMUM CURRENT DRAW(10mA)	164A
13	0086H	64	40		
1	0087H	1	01	RECORD TYPE ID 0X01 =DC OUTPUT Record	MULTIRECORD

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2	0088H	130	82	7:7 END OF LIST 6:4=000 3:0 RECORD FORMAT VERSION=2	HEADER
3	0089H	13	0D	RECORD LENGTH OF MULTIRECORD	
4	008AH	184	B8	RECORD CHECKSUM	
5	008BH	184	B8	HEADER CHECKSUM	
1	008CH	130	82	+12vSB 7:STANDBY=1,6-4:RESERVED 000B , 3-0:OUTPUT UMBER=0010B	+12VSB
2	008DH	196	C4	NOMINAL VOLTAGE(10mV)1220=04C4H	12.2V
3	008EH	4	04		
4	008FH	135	87	MAXIMUM NEGATIVE VOLTAGE DEVIATION(10mV)	11.59V
5	0090H	4	04		
6	0091H	1	01	MAXIMUM POSITIVE VOLTAGE DEVIATION(10mV)	12.81V
7	0092H	5	05		
8	0093H	120	78	RIPPLE AND NOISE PK-PK 10Hz TO 20MHz(mV) 120mV=0078H	120mV
9	0094H	0	00		
10	0095H	50	32	MINIMUM CURRENT DRAW(mA) 50mA=0032H	0.05A
11	0096H	0	00		
12	0097H	184	B8	MAXIMUM CURRENT DRAW(mA) 3000mA=0BB8H	3.0A
13	0098H	11	0B		
1	0099H	0	00	Unused Area	
2	009AH	0	00	Unused Area	
3	009BH	0	00	Unused Area	
4	009CH	0	00	Unused Area	
5	009DH	0	00	Unused Area	
6	009EH	0	00	Unused Area	
7	009FH	0	00	Unused Area	
8	00A0H	0	00	Unused Area	
9	00A1H	0	00	Unused Area	
10	00A2H	0	00	Unused Area	
11	00A3H	0	00	Unused Area	
12	00A4H	0	00	Unused Area	
13	00A5H	0	00	Unused Area	
14	00A6H	0	00	Unused Area	
15	00A7H	0	00	Unused Area	
16	00A8H	0	00	Unused Area	
17	00A9H	0	00	Unused Area	
18	00AAH	0	00	Unused Area	
19	00ABH	0	00	Unused Area	
20	00ACH	0	00	Unused Area	
21	00ADH	0	00	Unused Area	
22	00AEH	0	00	Unused Area	
23	00AFH	0	00	Unused Area	
24	00B0H	0	00	Unused Area	
25	00B1H	0	00	Unused Area	
26	00B2H	0	00	Unused Area	
27	00B3H	0	00	Unused Area	
28	00B4H	0	00	Unused Area	
29	00B5H	0	00	Unused Area	
30	00B6H	0	00	Unused Area	
31	00B7H	0	00	Unused Area	
32	00B8H	0	00	Unused Area	
33	00B9H	0	00	Unused Area	

34	00BAH	0	00	Unused Area	
35	00BBH	0	00	Unused Area	
36	00BCH	0	00	Unused Area	
37	00BDH	0	00	Unused Area	
38	00BEH	0	00	Unused Area	
39	00BFH	0	00	Unused Area	
40	00C0H	0	00	Unused Area	
41	00C1H	0	00	Unused Area	
42	00C2H	0	00	Unused Area	
43	00C3H	0	00	Unused Area	
44	00C4H	0	00	Unused Area	
45	00C5H	0	00	Unused Area	
46	00C6H	0	00	Unused Area	
47	00C7H	0	00	Unused Area	
48	00C8H	0	00	Unused Area	
49	00C9H	0	00	Unused Area	
50	00CAH	0	00	Unused Area	
51	00CBH	0	00	Unused Area	
52	00CCH	0	00	Unused Area	
53	00CDH	0	00	Unused Area	
54	00CEH	0	00	Unused Area	
55	00CFH	0	00	Unused Area	
56	00D0H	0	00	Unused Area	
57	00D1H	0	00	Unused Area	
58	00D2H	0	00	Unused Area	
59	00D3H	0	00	Unused Area	
60	00D4H	0	00	Unused Area	
61	00D5H	0	00	Unused Area	
62	00D6H	0	00	Unused Area	
63	00D7H	0	00	Unused Area	
64	00D8H	0	00	Unused Area	
65	00D9H	0	00	Unused Area	
66	00DAH	0	00	Unused Area	
67	00DBH	0	00	Unused Area	
68	00DCH	0	00	Unused Area	
69	00DDH	0	00	Unused Area	
70	00DEH	0	00	Unused Area	
71	00DFH	0	00	Unused Area	
72	00E0H	0	00	Unused Area	
73	00E1H	0	00	Unused Area	
74	00E2H	0	00	Unused Area	
75	00E3H	0	00	Unused Area	
76	00E4H	0	00	Unused Area	
77	00E5H	0	00	Unused Area	
78	00E6H	0	00	Unused Area	
79	00E7H	0	00	Unused Area	
80	00E8H	0	00	Unused Area	
81	00E9H	0	00	Unused Area	
82	00EAH	0	00	Unused Area	
83	00EBH	0	00	Unused Area	
84	00ECH	0	00	Unused Area	
85	00EDH	0	00	Unused Area	
86	00EEH	0	00	Unused Area	

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87	00EFH	0	00	Unused Area	
88	00F0H	0	00	Unused Area	
89	00F1H	0	00	Unused Area	
90	00F2H	0	00	Unused Area	
91	00F3H	0	00	Unused Area	
92	00F4H	0	00	Unused Area	
93	00F5H	0	00	Unused Area	
94	00F6H	0	00	Unused Area	
95	00F7H	0	00	Unused Area	
96	00F8H	0	00	Unused Area	
97	00F9H	0	00	Unused Area	
98	00FAH	0	00	Unused Area	
99	00FBH	0	00	Unused Area	
100	00FCH	0	00	Unused Area	
101	00FDH	0	00	Unused Area	
102	00FEH	0	00	Unused Area	
103	00FFH	0	00	Unused Area	

Table showing TEC2000-12-074NA HEX Information

Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	01	00	00	00	01	0B	00	F3	01	0A	19	C8	62	65	6C	20
10	20	20	20	20	D0	54	45	43	32	30	30	30	2D	31	32	2D
20	30	37	34	4E	41	D4	43	52	50	53	32	30	30	30	2D	41
30	48	20	20	20	20	20	20	20	20	20	C3	56	30	30	D3	54
40	45	43	32	30	30	30	4E	41	59	59	4D	4D	58	58	58	58
50	58	00	C0	C0	C1	00	00	8A	00	02	18	41	A5	D0	07	60
60	09	19	05	10	27	9C	31	20	4E	C0	5D	32	3C	0A	1E	34
70	F8	00	00	00	10	0A	02	0D	D4	13	01	C4	04	87	04	01
80	05	78	00	0A	00	10	40	01	82	0D	B8	B8	82	C4	04	87
90	04	01	05	78	00	32	00	B8	0B	00	00	00	00	00	00	00
A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

18.2 TEC2000-12-074RA FRU DATA

ITEM	01	BYTE VALUE		DESCRIPTION	BLOCK TITLE
		DEC	HEX		
1	0000H	1	01	COMMON HEADER FORMAT VERSION	COMMON HEADER
2	0001H	0	00	INTERNAL USE AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present	
3	0002H	0	00	CHASSIS INFO AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present.	
4	0003H	0	00	BOARD AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present.	
5	0004H	1	01	PRODUCT INFO AREA STARTING OFFSET (In Multiples Of 8 Bytes).	
6	0005H	11	0B	MULTIRECORD AREA STARTING OFFSET (In Multiples Of 8 Bytes).	
7	0006H	0	00	PAD, Write As 00H	
8	0007H	243	F3	COMMON HEADER CHECKSUM (ZERO CHECKSUM)	
1	0008H	1	01	PRODUCT AREA FORMAT VERSION 7:4 - Reserved, Write As 0000B 3:0 - Format Version Number = 1H	PRODUCT INFORMATION AREA
2	0009H	10	0A	PRODUCT AREA LENGTH (In multiples of 8 bytes)	
3	000AH	25	19	LANGUAGE CODE (ENGLISH)Z	
4	000BH	200	C8	MANUFACTURER NAME TYPE / LENGTH (C8H) 7:6 - Type Code 5:0 - Number Of Data Bytes.	
5	000CH	98	62	b	
6	000DH	101	65	e	
7	000EH	108	6C	l	
8	000FH	32	20		
9	0010H	32	20		
10	0011H	32	20		
11	0012H	32	20		
12	0013H	32	20		
13	0014H	208	D0	PRODUCT NAME Type/Length (CEh) 7:6 - Type Code 5:0 - Number Of Data Bytes.	MANUFACTURER'S MODEL NUMBER
14	0015H	84	54	T	
15	0016H	69	45	E	
16	0017H	67	43	C	
17	0018H	50	32	2	
18	0019H	48	30	0	
19	001AH	48	30	0	
20	001BH	48	30	0	
21	001CH	45	2D	-	
22	001DH	49	31	1	
23	001EH	50	32	2	
24	001FH	45	2D	-	
25	0020H	48	30	0	
26	0021H	55	37	7	
27	0022H	52	34	4	
28	0023H	82	52	R	
29	0024H	65	41	A	
30	0025H	212	D4	PRODUCT PART/MODEL NUMBER Type/Length (D4h)	CUSTOMER PART NUMBER
31	0026H	67	43	C	
32	0027H	82	52	R	
33	0028H	80	50	P	
34	0029H	83	53	S	
35	002AH	50	32	2	
36	002BH	48	30	0	
37	002CH	48	30	0	

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38	002DH	48	30	0	
39	002EH	45	2D	-	
40	002FH	65	41	A	
41	0030H	72	48	H	
42	0031H	32	20		
43	0032H	32	20		
44	0033H	32	20		
45	0034H	32	20		
46	0035H	32	20		
47	0036H	32	20		
48	0037H	32	20		
49	0038H	32	20		
50	0039H	32	20		
51	003AH	195	C3	PRODUCT VERSION NUMBER Type/Length (C3h)	CUSTOMER CURRENT REVISION
52	003BH	86	56	V	To be updated
53	003CH	48	30	0	To be updated
54	003DH	48	30	0	To be updated
55	003EH	211	D3	PRODUCT SERIAL NUMBER type/length byte (D3)	
56	003FH	84	54	T	To be updated
57	0040H	69	45	E	To be updated
58	0041H	67	43	C	To be updated
59	0042H	50	32	2	To be updated
60	0043H	48	30	0	To be updated
61	0044H	48	30	0	To be updated
62	0045H	48	30	0	To be updated
63	0046H	82	52	R	To be updated
64	0047H	65	41	A	To be updated
65	0048H	89	59	Y	To be updated
66	0049H	89	59	Y	To be updated
67	004AH	77	4D	M	To be updated
68	004BH	77	4D	M	To be updated
69	004CH	88	58	X	To be updated
70	004DH	88	58	X	To be updated
71	004EH	88	58	X	To be updated
72	004FH	88	58	X	To be updated
73	0050H	88	58	X	To be updated
74	0051H	0	00		To be updated
75	0052H	192	C0	FRU FILE ID Type/Length Byte	Not used, code is zero length byte
76	0053H	192	C0	FRU FILE ID Type/Length Byte	Not required
77	0054H	193	C1	ENCODED TO INDICATE NO MORE INFO FIELDS	
78	0055H	0	00	PAD (Always Zero)	
79	0056H	0	00	PAD (Always Zero)	
80	0057H	130	82	CHECKSUM (100H-(LOWER BYTE(SUM OF BYTES)))	To be updated
1	0058H	0	00	RECORD TYPE ID 0x00 =POWER SUPPLY INFORMATION	MULTI RECORD AREA
2	0059H	2	02	7:7 END OF LIST ,6:4=000B, 3:0 RECORD FORMAT VERSION=2	
3	005AH	24	18	RECORD LENGTH OF MULTIRECORD	
4	005BH	65	41	RECORD CHECKSUM (ZERO CHECKSUM)	
5	005CH	165	A5	HEADER CHECKSUM (ZERO CHECKSUM)	
1	005DH	208	D0	15-12:RESERVED,WRITE AS 0000B	
2	005EH	7	07	11-0:OVERALL CAPACITY(WATTS)	2000W
3	005FH	96	60	PEAK VALUE	
4	0060H	9	09	LSB FIRST	2400W
5	0061H	25	19	INRUSH CURRENT, FFH IF NOT SPECIFIED	25A

6	0062H	5	05	INRUSH INTERVAL IN MS.	5mS
7	0063H	16	10	LOW END INPUT VOLTAGE RANGE 1 100V=2710H	100V
8	0064H	39	27		
9	0065H	156	9C	HIGH END INPUT VOLTAGE RANGE 1 127V=319CH	127V
10	0066H	49	31		
11	0067H	32	20	LOW END INPUT VOLTAGE RANGE 2 200V=4E20H	200V
12	0068H	78	4E		
13	0069H	192	C0	HIGH END INPUT VOLTAGE RANGE 2 240V=5DC0H	240V
14	006AH	93	5D		
15	006BH	50	32	LOW END INPUT FREQUENCY RANGE 50HZ=32H	50Hz
16	006CH	60	3C	HIGH END INPUT FREQUENCY RANGE 60HZ=3CH	60Hz
17	006DH	10	0A	A/C DROPOUT TOLERANCE IN mS 10mS=0AH	10mS
18	006EH	30	1E	7-5:RESERVED,WRITE AS 000B 4:TACHOMETER PULSES PER POTATION/PREDICTIVE FALL POLARITY YES=1(FAIL=1,PASS=0) 3:HOT SWAP/REDUNDANCY SUPPORT YES=1 2:AUTOSWITCH YES=1 1:POWER FACTOR CORRECTION YES=1 0:PREDICTIVE FALL SUPPLY YES=1	
19	006FH	52	34	PEAK WATTAGE 15-12:HOLD UP TIME IN SECONDS 1S=1H	
20	0070H	248	F8	11-0 PEAK CAPACITY (WATTS)(LSB FIRST) 2100W=0834H	15S
21	0071H	0	00	COMMBINED WATTAGE 7-4:Voltage 1 3-0:Voltage 2=00H	
22	0072H	0	00	BYTE 2:3 TOTAL COMBINED WATTAGE (LSB FIRST) W=0000H	0
23	0073H	0	00	BYTE 2:3 TOTAL COMBINED WATTAGE (LSB FIRST) W=0000H	
24	0074H	16	10	PREDICTIVE FAIL TACHOMETER LOWER THRESHOLD(PRM/60)1000/60=16	
1	0075H	10	0A	RECORD TYPE ID 0X01 =DC OUTPUT Record	MULTIRECORD
2	0076H	2	02	7:7 END OF LIST 6:4=000 3:0 RECORD FORMAT VERSION=2	HEADER
3	0077H	13	0D	RECORD LENGTH OF MULTIRECORD	
4	0078H	212	D4	RECORD CHECKSUM	
5	0079H	19	13	HEADER CHECKSUM	
1	007AH	1	01	+12V 7:STANDBY=0,6-4:RESERVED 000B , 3-0:OUTPUT UMBER=0001B	+12V
2	007BH	196	C4	NOMINAL VOLTAGE(10mV)1220=04C4H	12.2V
3	007CH	4	04		
4	007DH	135	87	MAXIMUM NEGATIVE VOLTAGE DEVIATION(10mV) 1159=0487H	11.59V
5	007EH	4	04		
6	007FH	1	01	MAXIMUM POSITIVE VOLTAGE DEVIATION(10mV) 1281=0501H	12.81V
7	0080H	5	05		
8	0081H	120	78	RIPPLE AND NOISE PK-PK 10Hz TO 20MHz(mV) 120mV=0078H	120mV
9	0082H	0	00		
10	0083H	10	0A	MINIMUM CURRENT DRAW(10mA)	0.1A
11	0084H	0	00		
12	0085H	16	10	MAXIMUM CURRENT DRAW(10mA)	164A
13	0086H	64	40		
1	0087H	1	01	RECORD TYPE ID 0X01 =DC OUTPUT Record	MULTIRECORD
2	0088H	130	82	7:7 END OF LIST 6:4=000 3:0 RECORD FORMAT VERSION=2	HEADER

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3	0089H	13	0D	RECORD LENGTH OF MULTIRECORD	
4	008AH	184	B8	RECORD CHECKSUM	
5	008BH	184	B8	HEADER CHECKSUM	
1	008CH	130	82	+12vSB 7:STANDBY=1,6-4:RESERVED 000B , 3-0:OUTPUT UMBER=0010B	+12VSB
2	008DH	196	C4	NOMINAL VOLTAGE(10mV)1220=04C4H	12.2V
3	008EH	4	04		
4	008FH	135	87	MAXIMUM NEGATIVE VOLTAGE DEVIATION(10mV)	11.59V
5	0090H	4	04		
6	0091H	1	01	MAXIMUM POSITIVE VOLTAGE DEVIATION (10mV)	12.81V
7	0092H	5	05		
8	0093H	120	78	RIPPLE AND NOISE PK-PK 10Hz TO 20MHz (mV) 120mV=0078H	120mV
9	0094H	0	00		
10	0095H	50	32	MINIMUM CURRENT DRAW (mA) 50mA=0032H	0.05A
11	0096H	0	00		
12	0097H	184	B8	MAXIMUM CURRENT DRAW (mA) 3000mA=0BB8H	3.0A
13	0098H	11	0B		
1	0099H	0	00	Unused Area	
2	009AH	0	00	Unused Area	
3	009BH	0	00	Unused Area	
4	009CH	0	00	Unused Area	
5	009DH	0	00	Unused Area	
6	009EH	0	00	Unused Area	
7	009FH	0	00	Unused Area	
8	00A0H	0	00	Unused Area	
9	00A1H	0	00	Unused Area	
10	00A2H	0	00	Unused Area	
11	00A3H	0	00	Unused Area	
12	00A4H	0	00	Unused Area	
13	00A5H	0	00	Unused Area	
14	00A6H	0	00	Unused Area	
15	00A7H	0	00	Unused Area	
16	00A8H	0	00	Unused Area	
17	00A9H	0	00	Unused Area	
18	00AAH	0	00	Unused Area	
19	00ABH	0	00	Unused Area	
20	00ACH	0	00	Unused Area	
21	00ADH	0	00	Unused Area	
22	00AEH	0	00	Unused Area	
23	00AFH	0	00	Unused Area	
24	00B0H	0	00	Unused Area	
25	00B1H	0	00	Unused Area	
26	00B2H	0	00	Unused Area	
27	00B3H	0	00	Unused Area	
28	00B4H	0	00	Unused Area	
29	00B5H	0	00	Unused Area	
30	00B6H	0	00	Unused Area	
31	00B7H	0	00	Unused Area	
32	00B8H	0	00	Unused Area	
33	00B9H	0	00	Unused Area	
34	00BAH	0	00	Unused Area	
35	00BBH	0	00	Unused Area	

36	00BCH	0	00	Unused Area	
37	00BDH	0	00	Unused Area	
38	00BEH	0	00	Unused Area	
39	00BFH	0	00	Unused Area	
40	00C0H	0	00	Unused Area	
41	00C1H	0	00	Unused Area	
42	00C2H	0	00	Unused Area	
43	00C3H	0	00	Unused Area	
44	00C4H	0	00	Unused Area	
45	00C5H	0	00	Unused Area	
46	00C6H	0	00	Unused Area	
47	00C7H	0	00	Unused Area	
48	00C8H	0	00	Unused Area	
49	00C9H	0	00	Unused Area	
50	00CAH	0	00	Unused Area	
51	00CBH	0	00	Unused Area	
52	00CCH	0	00	Unused Area	
53	00CDH	0	00	Unused Area	
54	00CEH	0	00	Unused Area	
55	00CFH	0	00	Unused Area	
56	00D0H	0	00	Unused Area	
57	00D1H	0	00	Unused Area	
58	00D2H	0	00	Unused Area	
59	00D3H	0	00	Unused Area	
60	00D4H	0	00	Unused Area	
61	00D5H	0	00	Unused Area	
62	00D6H	0	00	Unused Area	
63	00D7H	0	00	Unused Area	
64	00D8H	0	00	Unused Area	
65	00D9H	0	00	Unused Area	
66	00DAH	0	00	Unused Area	
67	00DBH	0	00	Unused Area	
68	00DCH	0	00	Unused Area	
69	00DDH	0	00	Unused Area	
70	00DEH	0	00	Unused Area	
71	00DFH	0	00	Unused Area	
72	00E0H	0	00	Unused Area	
73	00E1H	0	00	Unused Area	
74	00E2H	0	00	Unused Area	
75	00E3H	0	00	Unused Area	
76	00E4H	0	00	Unused Area	
77	00E5H	0	00	Unused Area	
78	00E6H	0	00	Unused Area	
79	00E7H	0	00	Unused Area	
80	00E8H	0	00	Unused Area	
81	00E9H	0	00	Unused Area	
82	00EAH	0	00	Unused Area	
83	00EBH	0	00	Unused Area	
84	00ECH	0	00	Unused Area	
85	00EDH	0	00	Unused Area	
86	00EEH	0	00	Unused Area	
87	00EFH	0	00	Unused Area	
88	00F0H	0	00	Unused Area	

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89	00F1H	0	00	Unused Area	
90	00F2H	0	00	Unused Area	
91	00F3H	0	00	Unused Area	
92	00F4H	0	00	Unused Area	
93	00F5H	0	00	Unused Area	
94	00F6H	0	00	Unused Area	
95	00F7H	0	00	Unused Area	
96	00F8H	0	00	Unused Area	
97	00F9H	0	00	Unused Area	
98	00FAH	0	00	Unused Area	
99	00FBH	0	00	Unused Area	
100	00FCH	0	00	Unused Area	
101	00FDH	0	00	Unused Area	
102	00FEH	0	00	Unused Area	
103	00FFH	0	00	Unused Area	

Table showing TEC2000-12-074RA HEX Information

Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	01	00	00	00	01	0B	00	F3	01	0A	19	C8	62	65	6C	20
10	20	20	20	20	D0	54	45	43	32	30	30	30	2D	31	32	2D
20	30	37	34	52	41	D4	43	52	50	53	32	30	30	30	2D	41
30	48	20	20	20	20	20	20	20	20	20	C3	56	30	30	D3	54
40	45	43	32	30	30	30	52	41	59	59	4D	4D	58	58	58	58
50	58	00	C0	C0	C1	00	00	82	00	02	18	41	A5	D0	07	60
60	09	19	05	10	27	9C	31	20	4E	C0	5D	32	3C	0A	1E	34
70	F8	00	00	00	10	0A	02	0D	D4	13	01	C4	04	87	04	01
80	05	78	00	0A	00	10	40	01	82	0D	B8	B8	82	C4	04	87
90	04	01	05	78	00	32	00	B8	0B	00	00	00	00	00	00	00
A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

For more information on these products consult: tech.support@psbel.com

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