PLS1600-12-080xA

AC-DC Front-End Power Supply

The PLS1600-12-080xA is a 1600 Watt AC to DC, power-factor-corrected (PFC) power supply that converts standard AC power into a main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PLS1600-12-080xA utilizes full digital control architecture for greater efficiency, control, and functionality.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- High Efficiency, meet 80 plus “Platinum” efficiency requirement
- Universal input voltage range: 90-264 VAC
- AC input with active power factor correction
- High voltage DC input: 180-300 VDC
- 1600 W continuous output power capability for both low line and high line
- Always-on 12 VSB / 3 A standby output
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- High power density design: 42 W/in^3
- Small form factor: 80(W) x 40(H) x 195(L) mm
- Power Management Bus communication interface for control, programming, and monitoring
- Status LED with fault signaling

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

Please read our datasheet & drawing disclaimer here.

1. ORDERING INFORMATION

PLS	1600	-	12	-	080	x	A
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PLS Front-End	1600 W		12 V		80 mm	N: Normal[1)] R: Reverse[2)]	A: AC

[1)] Normal airflow from rear to front (from output connector to input AC socket)
[2)] Reverse airflow from front to rear (from input AC socket to output connector)

2. OVERVIEW

The PLS1600-12-080xA AC/DC power supply is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonance-soft-switching technology to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range, the PLS1600-12-080xA maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.
The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range. The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.
Status information is provided with a front-panel bicolor LED. In addition, the power supply can be controlled and the fan speed set via the I^2C bus. The I^2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I^2C bus.

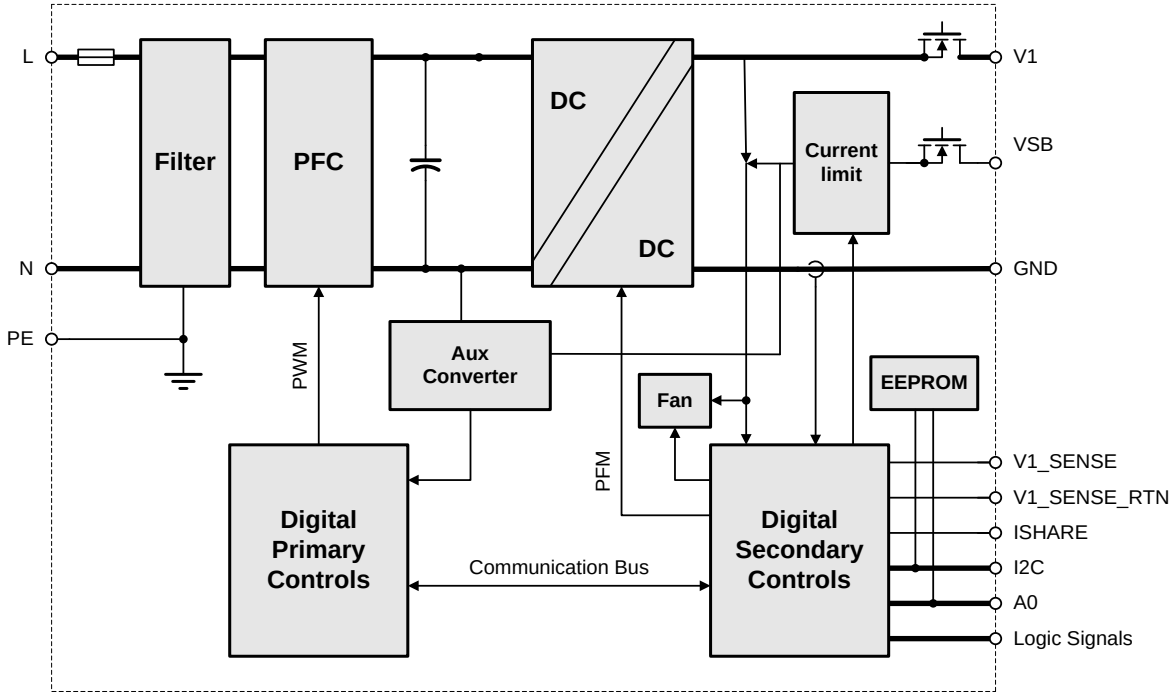

Figure 1. PLS1600-12-080xA Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
$V_{i\,max}$	Maximum AC Input Voltage	Continuous		264	VAC

4. INPUT

General Condition: T_A = 0… 55 °C, unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	AC Nominal Input Voltage	Rated AC Input Voltage	100		240	VAC
V_i	AC Input Voltage Range	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	90		264	VAC
$V_{i\,nom\,DC}$	DC Nominal Input Voltage	Rated HVDC		240		VDC
$V_{i\,DC}$	DC Input Voltage Range	Normal operating ($V_{i\,minDC}$ to $V_{i\,maxDC}$)	180		300	VDC
$I_{i\,max}$	Maximum Input Current	V_{IN} = 100 VAC, I_1=133.3 A, I_{SB} =3 A			20	A_{RMS}
		V_{IN} = 200 VAC, I_1=133.3 A, I_{SB} =3 A			10	A_{RMS}
$I_{i\,inrush}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, T_{NTC} = 25°C (see Section 4.2 and Figure 2)			30	A_p
f_i	Input Frequency		47	50/60	63	Hz
$V_{i\,on}$	Turn-on Input Voltage[1)]	Ramping up	80		88	VAC
$V_{i\,off}$	Turn-off Input Voltage[1)]	Ramping down	75		85	VAC
		Vi = 230 VAC, 50 Hz and 60 Hz, Vi = 115 VAC,60 Hz				
		10% Load	0.85			W/VA
PF	Power Factor	20% Load	0.95			W/VA
		50% Load	0.97			W/VA
		100% Load	0.97			W/VA
		V_{IN} = 230 VAC, 10% load	82			%
		V_{IN} = 230 VAC, 20% load	90	93.5		%
η	Efficiency[2)]	V_{IN} = 230 VAC, 50% load	94	94.5		%
		V_{IN} = 230 VAC, 100% load	91	93.5		%
$T_{Ride\text{-}through}$	Ride through time	V_{IN}= 90 VAC, I_1=133.3 A, I_{SB} =3 A	12			ms
$T_{V1\,holdup}$	Hold-up Time V_1	V_{IN}= 230 VAC, I_1=133.3 A, I_{SB} =3 A	12			ms
$T_{VSB\,holdup}$	Hold-up Time V_{SB}	12V_{SB}, full load	100			ms

[1)] The Front-End is provided with a typical hysteresis of 4 VAC during turn-on and turn-off within the ranges
[2)] Efficiency measured without fan power

Table 1. Input conditions

4.1 INPUT FUSE

Quick-acting (fast blow) type, 25 A input fuse (5.93 x 21.75 mm max.) in series with the L-line inside the power supply protects against severe defects. The fuse is not accessible from the outside and is therefore not a serviceable part.

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4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 2.18 µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through a NTC which will limit the inrush current.

NOTE: Do not repeat plug-in / out operations below 5 sec interval time at maximum input, high temperature condition, or else the internal in-rush current limiting device PTC may not sufficiently cool down and excessive inrush current or component failure(s) may result.

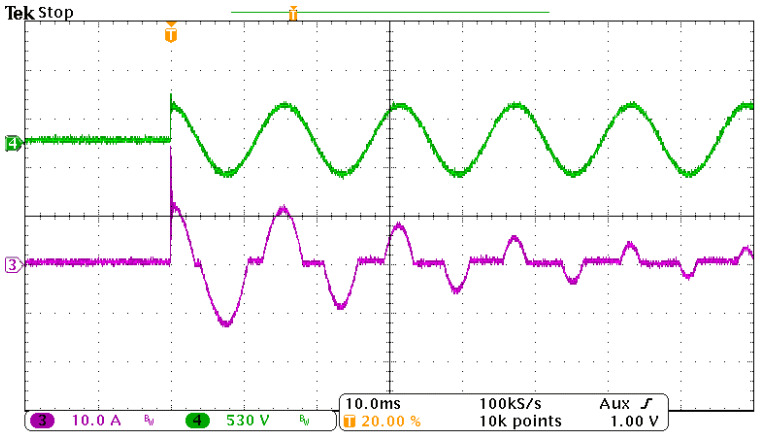

Figure 2. Inrush current, Vin = 264Vac, 90°, CH3: Iin (10A/div), CH4: Vin (530V/div)

4.3 INPUT UNDER-VOLTAGE

If the AC input voltage stays below the input under-voltage lockout threshold *Vi on*, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again**.**

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform.

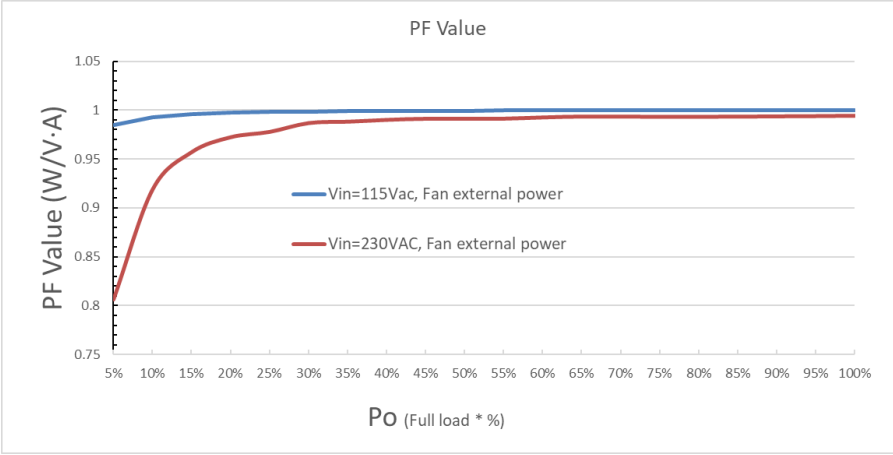

Figure 3. Power Factor vs. Output Power

4.5 EFFICIENCY

High efficiency (see Figure 4*)* is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

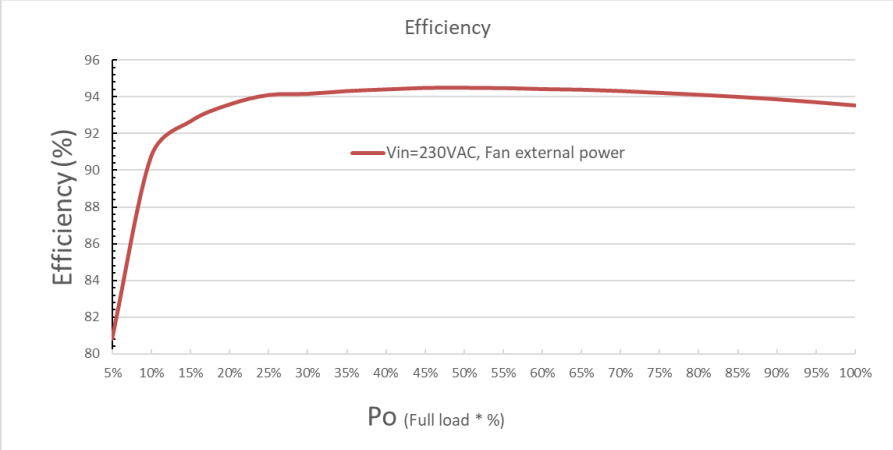

Figure 4. Efficiency vs. Output Power

5. OUTPUT

General condition: T_A = 0…55 °C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy		-0.5		+0.5	%$V_{1\ nom}$
$dV_{1\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, Ta_{min} *to* Ta_{max}	-5		+5	%$V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		1600		W
$I_{1\ nom}$	Output Current	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$		133.3		ADC
$V_{1\ pp}$	Output Ripple Voltage[1)]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, 20MHz Bandwidth			120	mVpp
$dI_{1\ share}$	Current Sharing	(I_x - I_y) / I_{tot}, I > 10%	-5		+5	% $I_{1\ nom}$
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ nom}$		8		VDC
$dV_{1\ dyn}$	Dynamic Load Regulation[2)]	Test frequency between 50Hz and 5KHz at duty cycles from 10% to 90%, ΔI1 = 50% $I1_{nom}$, I1 = 5% $I1_{nom}$ … 100% $I1_{nom}$, dI1/dt =1A/µs, recovery within 1% of $V1_{nom}$	11.40		12.60	VDC
t_{rec}	Recovery Time				2	ms
$t_{V1\ rise}$	Output Voltage Rise Time	V_1 = 10…90% $V_{1\ nom}$	1		20	ms
$t_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom\ HL}$, 0 to 100% $I_{1\ nom}$			0.6	V
$C_{V1\ load}$	Capacitive Loading				10,000	µF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	0.5·$I_{SB\ nom}$, T_A = 25°C		12.0		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-0.5		+0.5	%$V_{SB\ nom}$
$dV_{sb\ load}$	Load Regulation	0 to 100% $I_{SB\ nom}$			600	mV
$dV_{sb\ line}$	Line Regulation	$V_{i\ min\ LL}$ to $V_{i\ max\ HL}$			120	mV

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$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$	-5		+5	%$V_{SB\ nom}$
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		36		W
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$		3		ADC
$V_{SB\ pp}$	Output Ripple Voltage [3]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, 20 MHz bandwidth			120	mVpp
dV_{SB}	Droop	10% - 100 % $I_{SB\ nom}$		350		mV
$dV_{SB\ dyn}$	Dynamic Load Regulation[4]	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 0 … 100% $I_{SB\ nom}$,	11.40		12.60	VDC
t_{rec}	Recovery Time	dI_{SB}/dt = 1A/µs, recovery within 1% of $V_{SB\ nom}$			2	ms
$t_{VSB\ rise}$	Output Voltage Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$,	5		20	ms
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom\ HL}$, 0 to 100% $I_{SB\ nom}$			0.6	V
$C_{VSB\ load}$	Capacitive Loading				1000	µF

[1), 2), 3), 4)] Ripple noise and dynamic load measured with a 10µF low ESR capacitor in parallel with a 0.1µF ceramic capacitor at the point of measurement. See section 5.9

Table 2. Output spec

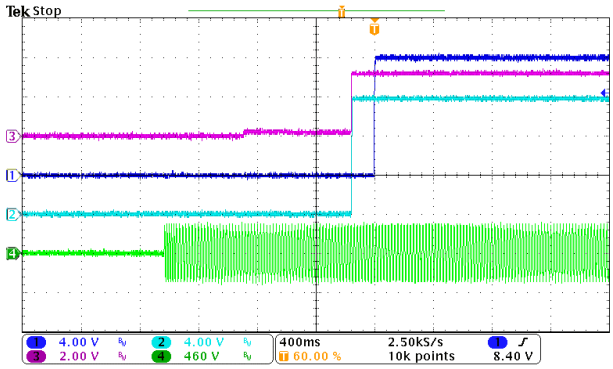

Figure 5. Turn-On AC Line 230VAC, full load (400ms/div)
CH1: V1 (4V/div) CH2: V_{SB} (4V/div)
CH3: VIN_OK_H (2V/div) CH4: V_i (460V/div)

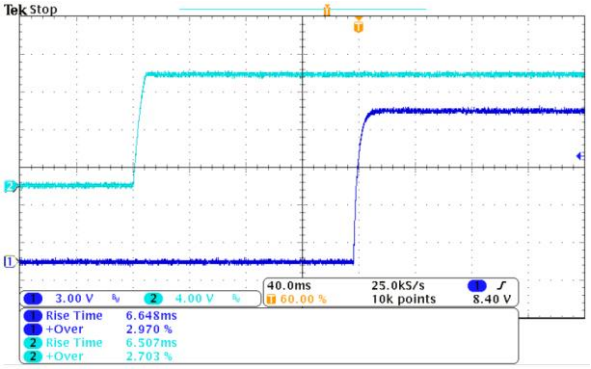

Figure 6. Turn-On AC Line 230VAC, no load (40ms/div)
CH1: V1 (3V/div) CH2: V_{SB} (4V/div)

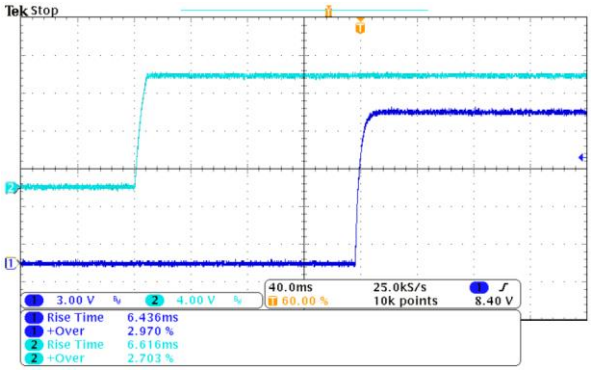

Figure 7. Turn-On AC Line 230VAC, full load (40ms/div)
CH1: V1 (3V/div) CH2: V_{SB} (4V/div)

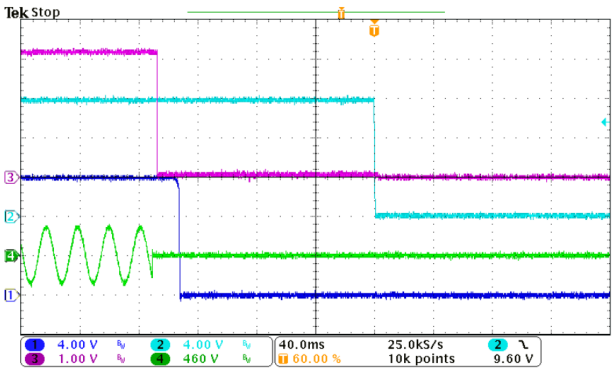

Figure 8. Turn-Off AC Line 230VAC, full load (40ms/div)
CH1: V1 (4V/div) CH2: V_{SB} (4V/div)
CH3: VIN_OK_H (1V/div) CH4: V_i (460V/div)

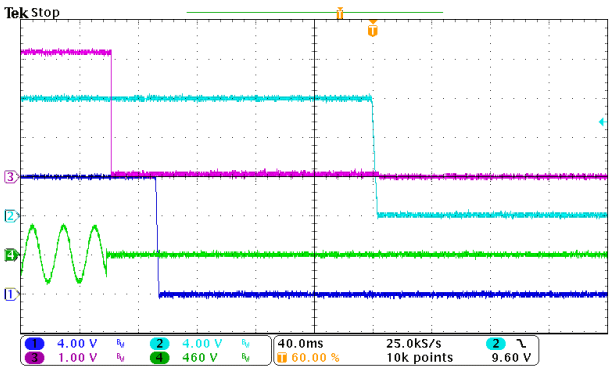

Figure 9. Turn-Off AC Line 230VAC, half load (40ms/div)
CH1: V1 (4V/div) CH2: V_{SB} (4V/div)
CH3: VIN_OK_H (1V/div) CH4: V_i (460V/div)

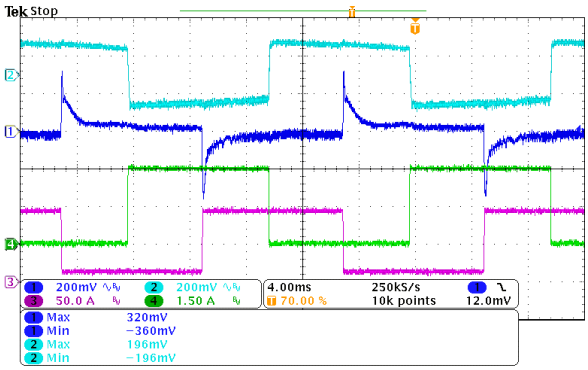

Figure 10. Load transient V_1, V_{SB} .0 to 50% full load (4ms/div)
CH1: V1 (200mV~/div) CH2: V_{SB} (200mV~/div)
CH3: I1 (50A/div) CH4: I_{SB} (1.5A/div)

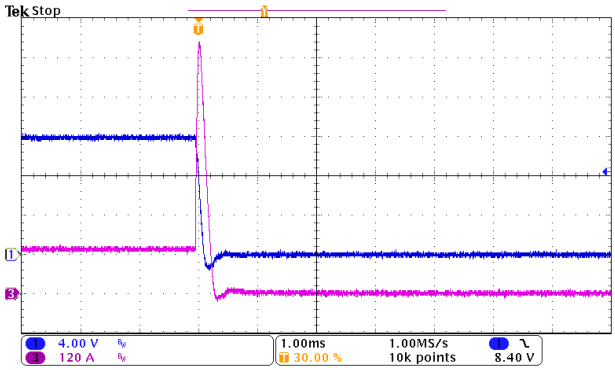

Figure 11. Short circuit on V1 (1ms/Div)
CH1: V1 (4V/div) CH3: I_{SC} (120A/div)

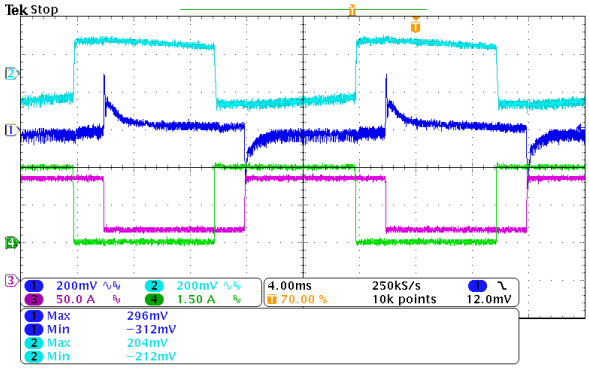

Figure 12. Load transient V_1, V_{SB} .50 to 100% full load (4ms/div)
CH1: V1 (200mV~/div) CH2: V_{SB} (200mV~/div)
CH3: I1 (50A/div) CH4: I_{SB} (1.5A/div)

5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in Figure 13. Alternatively, separated ground signals can be used as shown in Figure 14. In this case the two ground planes should be connected together at the power supplies ground pins.

NOTE:
Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal on the AC inlet. Therefore, it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

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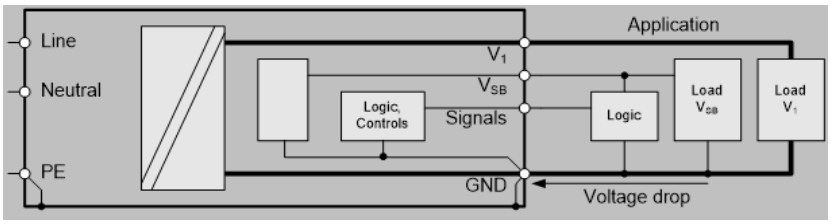

Figure 13. Common Low Impedance Ground Plane

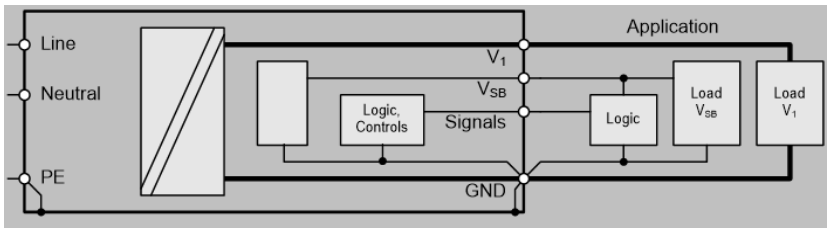

Figure 14. Separated Power and Signal Ground

5.2 CLOSED LOOP STABILITY

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of 45 degrees phase margin and -10dB gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at 20%, 50% and 100% loads as applicable, 0% load is just for reference.

5.3 RESIDUAL VOLTAGE IMMUNITY IN STANDBY MODE

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON_L signal is de-asserted.

5.4 COMMON MODE NOISE

The common mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz.

The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure), the test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

5.5 SOFT STARTING

The Power Supply contains control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

5.6 ZERO LOAD STABILITY REQUIREMENTS

When the power subsystem operates in a no-load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.7 HOT SWAP REQUIREMENTS

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process, the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the input power cord is inserted into the power supply.

5.8 FORCED LOAD SHARING

The PLS front-ends have an active current share scheme implemented for main output V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The output will share within 10% at full load.

The 12VSB output uses the droop method current sharing. The output current must share within 0.7A for loads greater than 10%. The 12VSB output shall have 350mV ±10% typical droop voltage from 10% load to full load and voltage set point of +12V at 1.5A (half of the max output current). The Standby 12VSB output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause outputs to go out of regulation in the system.

5.9 RIPPLE / NOISE

Ripple and noise shall be measured by using the following methods:

a) Outputs bypassed at the point of measurement with a parallel combination of 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitors, referring the setup in Figure 15

b) The ripple voltage is measured with 20 MHz bandwidth

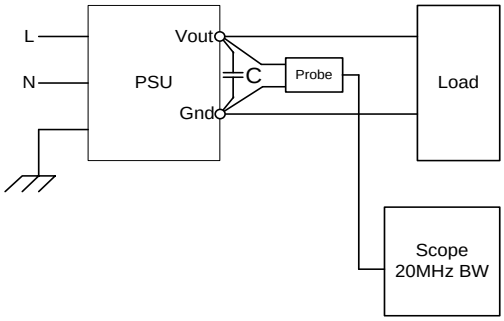

Figure 15. Differential Noise Test Setup

6. PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)	Not use accessible, quick-acting (fast blow)		25		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type	13.6	14.2	15.0	VDC
$V_{VSB\ OV}$	OV Threshold V_{SB}	Over Voltage V_1 Protection, Automatic recovery Type	13.6	14.2	15.0	VDC

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$V_{1\ UV}$	UV Threshold V_1	Under Voltage V_1 Protection. Protection behavior, see section 6.4		10.8		VDC
$V_{VSB\ UV}$	UV Threshold V_{SB}	Under Voltage V_1 Protection, Automatic recovery Type		10.8		VDC
$I_{V1\ OC}$	OC Limit V_1	Over Current Limitation, $V_{i\ min\ HL}$ to $V_{i\ max\ HL}$. Protection behavior, see section 6.5	147	170	186	ADC
$I_{VSB\ OC}$	OC Limit V_{SB}	Over Current Limitation, Automatic recovery Type	3.5	3.9	4.8	A
T_{SD}	Over Temperature On Critical Points	Automatic shut-down		Refer to Table 12		°C

Table 3. Protections

6.1 PROTECTION CIRCUITS

Protection circuits inside the power supply shall cause only the power supply's main output to shut down. If the power supply latches off due to a protection circuit tripping, an input AC or DC cycle OFF for 15sec and a PSON_L cycle HIGH for 1sec shall be able to reset the power supply.

6.2 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature.
In an OTP condition, the PSU will shut down, when the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on, the OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition, the OTP trip temperature level shall be at least 5°C higher than over temperature warning threshold level.
See section 10 and Table 12 for OTP trip temperature.

6.3 OVER VOLTAGE PROTECTION

The PLS1600-12-080xA front-end provides a fixed threshold overvoltage (OV) protection implemented for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. 12VSB will be auto recovered after removing OVP limit.

6.4 UNDER VOLTAGE DETECTION

12V main should shut down for 10s then retry automatically, if fault is still valid after 10s then 12V main should latch off until an AC power recycled or by toggling the PSON_L input (or remote on/off).
When 12V main output is in OVP mode, the 12VSB shall remain on. When the 12VSB is in OVP mode, both 12V Main and 12VSB should shut down

6.5 OVER CURRENT LIMIT & OVER-POWER PROTECTION (OCP & OPP)

The power supply shall have a current limit to prevent the main output from exceeding the over current limit value. 12V main should shut down for 10s then retry automatically, if fault is still valid after 10s then 12V main should latch off until an AC power recycled or by toggling the PSON_L input (or remote on/off).
When 12V main output is in OCP mode, the 12V standby shall remain on. Over current protection for 12V standby shall be a hiccup mode and during that time 12V main output shall be turned off.

6.6 PEAK POWER

The power supply shall be able to support higher peak power levels for up to 100µs. Below table is Peak Power testing conditions.

PEAK POWER	PEAK CURRENT	PEAK LOAD DURATION	VOLTAGE UNDERSHOOT
2280W	190A	100µs	5%

Table 4. Peak Power

7. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to Section 9 and document of PLS1600-12-080xA Power Management Bus Communication Manual. Below are accuracy specs:

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,mon}$	Input RMS Voltage		-3		+3	%
$I_{i\,mon}$	Input RMS Current	I_1 < 10% $I_{1\,nom}$ (For information only)	-1		+1	A
		10% $I_{1\,nom}$ < I_1 < 20% $I_{1\,nom}$	-10		+10	%
		I_1 > 20% $I_{1\,nom}$	-5		+5	%
$P_{i\,mon}$	True Input Power	I_1 < 10% $I_{1\,nom}$ (For information only)	-14		+14	W
		10% $I_{1\,nom}$ < I_1 < 20% $I_{1\,nom}$	-10		+10	%
		I_1 > 20% $I_{1\,nom}$	-5		+5	%
$V_{1\,mon}$	V_1 Voltage		-2		+2	%
$V_{SB\,mon}$	V_{SB} Voltage		-2		+2	%
$I_{1\,mon}$	V_1 Current	I_1 < 10% $I_{1\,nom}$ (For information only)	-1		+1	ADC
		10% $I_{1\,nom}$ < I_1 < 20% $I_{1\,nom}$	-10		+10	%
		I_1 > 20% $I_{1\,nom}$	-5		+5	%
$I_{SB\,mon}$	V_{SB} Current	I_{SB} < 10% $I_{SB\,nom}$ (For information only)	-1		+1	ADC
		10% $I_{SB\,nom}$ < I_{SB} < 20% $I_{SB\,nom}$	-10		+10	%
		I_{SB} > 20% $I_{SB\,nom}$	-5		+5	%
P_{nom}	Total Output Power	I_1 < 10% $I_{1\,nom}$ (For information only)	-13		+13	W
		10% $I_{1\,nom}$ < I_1 < 20% $I_{1\,nom}$	-10		+10	%
		I_1 > 20% $I_{1\,nom}$	-5		+5	%
T_{Inlet}	Air Inlet (Ambient) Temperature	-5°C ≤ T_{amb} ≤ 65°C	-3		+3	°C
T_{Outlet}	Air Outlet Temperature		-5		+5	°C

Table 5. Input, Output, Temperature Power Management Bus accuracy

8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PSON_L						
V_{IL}	Input Low Level Voltage	PSON_L: Main output enabled	-0.2		0.5	V
V_{IH}	Input High Level Voltage	PSON_L: Main output disabled	2		5.25	V
$I_{IL,H}$	Maximum Source Current	V_I = -0.2V to +3.5V			4	mA
$R_{pull\,up}$	Pull-up to 3.3V Located in Power Supply			1		kΩ
PSKILL						
V_{IL}	Input Low Level Voltage	PSKILL: Main and 12VSB output enabled	-0.2		0.5	V
V_{IH}	Input High Level Voltage	PSKILL: Main and 12VSB output disabled	2		5.25	V
$I_{IL,H}$	Maximum Source Current	V_I = -0.2V to +3.5V			4	mA

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$R_{pull\ up}$	Pull-up to 3.3V Located in Power Supply			4.7		kΩ
PWOK_H						
V_{OL}	Output Low Level Voltage	$Vi < V_{i\ min\ LL}$, I_{sink}=400µA	0		0.4	V
V_{OH}	Output High Level Voltage	$Vi > V_{i\ min\ LL}$, I_{source}=200µA	2.4		3.46	V
I_S	Maximum Sink Current Maximum Source Current	PWOK_H = low PWOK_H = high			400 2	µA mA
SMB_ALERT_L						
V_{ext}	Maximum External Pull up Voltage				3.46	V
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4mA	0		0.4	V
$R_{pull\ up}$	Pull-up to 3.3V Located in Power Supply			None		
I_S	Sink Current	SMB_ALERT_L = low SMB_ALERT_L= high			4 50	mA µA
VIN_OK_H						
V_{ext}	Maximum External Pull up Voltage				3.46	V
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4mA	0		0.4	V
$R_{pull\ up}$	Pull-up to 3.3V Located in Power Supply			1		kΩ
I_S	Sink Current	VIN_OK_H = low			4	mA

Table 6. Signals

8.1 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PSON_L can be either controlled by an open collector device or by a voltage source.

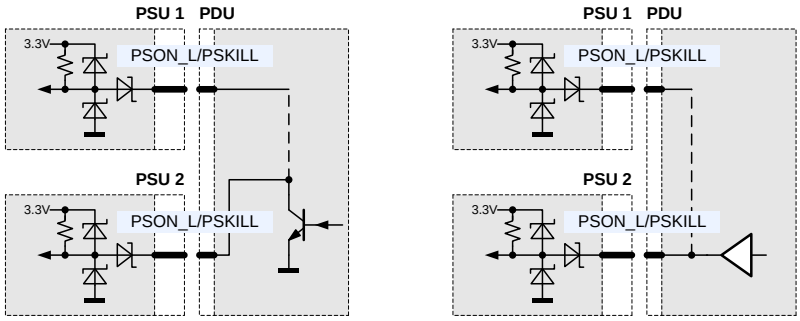

Figure 16. PSON_L/ PSKILL connection

8.2 PSKILL INPUT

Shuts off power supply both 12V Main output V1 and 12V Standby outputs. High = OFF, Low = ON (short pin refer to mechanical drawing for the correct distance from the edge) Prevents partially installed supply from outputting a voltage. This pin is intended to be grounded on system. This signal should have a series diode before going to the connector side after the pull up resistor

8.3 PWOK_H (DCOK_H) OUTPUT

PWOK_H is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK_H will be de-asserted to a LOW state. The start of the PWOK_H delay time shall inhibit as long as any power supply output is in current limit.

The PWOK_H and I2C bus of PSU are connected together on the redundant system. The below block diagram was shown the wiring on the system. The internal PWOK_H circuit of power supply is designed so that the PWOK_H bus is the wire-ORed function of the individual PWOK_H signals of all the power supply in parallel. Suggest system Pull-up to 3.3V and pull-up resistance is 10K. The PWOK_H signal also can be separated for each PSU design in system side to indicate each PSU output state.

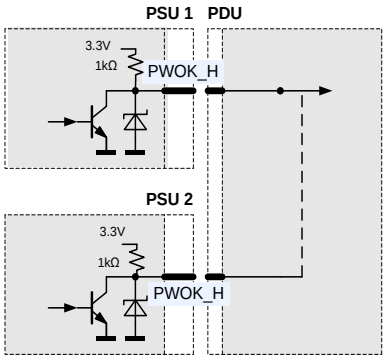

Figure 17. PWOK_H connection

8.4 SMB_ALERT_L (INTERRUPT_L) OUTPUT

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning blinking Amber (warning triggered) or solid Amber (protection triggered).

The inlet temperature warning threshold must be set at 60°C, preventing exhaust air and cord temperatures temperature exceeding safety ratings. The warning gets de-asserted once inlet air temperature returns into specified operating temperature range.

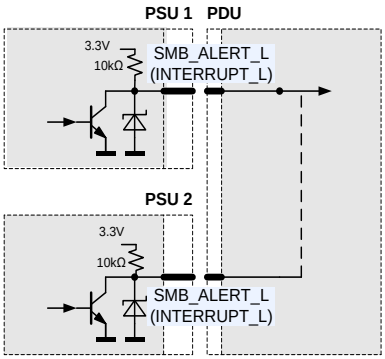

Figure 18. SMB_ALERT_L (INTERRUPT_L) Connection

8.5 VIN_OK_H (ACOK_H) OUTPUT

The VIN_OK_H is an internal pull-up to 3.3V via 1kOhm resistor. VIN_OK_H signal is active-high that indicates the input voltage is within the range that the power supply can use and turn on. VIN_OK_H is low level indicates the input voltage is out of operation input range.

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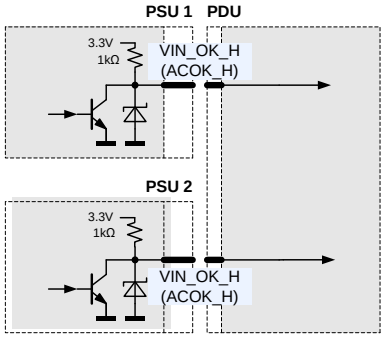

Figure 19. VIN_OK_H (ACOK_H) Connection

8.6 PRESENT_L OUTPUT

The PRESENT_L pin is wired through a 0 Ohm/0603 resistor to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low level voltage if power supply is seated.

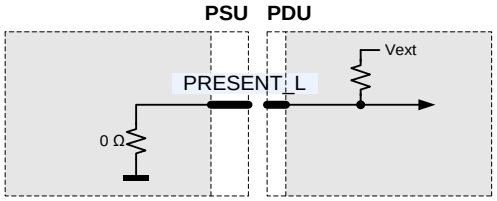

Figure 20. PRESENT_L Connection

8.7 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.
With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.8 TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 1 to 20ms. For 12VSB, The rise time is allowed to from 5ms to 20ms. All outputs must rise monotonically. Table 7 shows the timing requirements for the power supply being turned on and off two ways; 1) via the AC input with PSON_L held low; 2) via the PSON_L signal with the AC input applied. The PSU needs to remain off for 1 second minimum after PWOK_H is de-asserted.

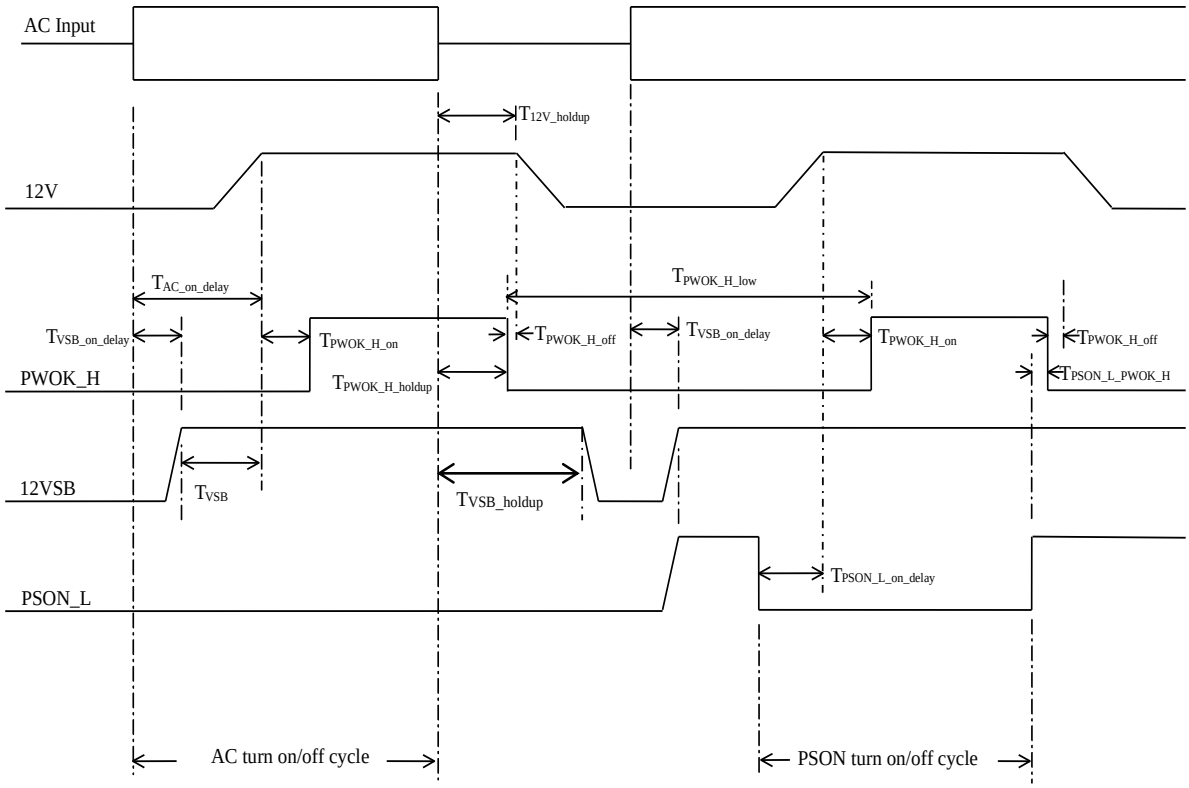

Figure 21. Turn On/Off Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_{12V_rise}	12V main output voltage rise time	1		20	ms
T_{12VSB_rise}	12VSB output voltage rise time	5		20	ms
$T_{VSB_on_delay}$	Delay from AC being applied to 12VSB being within regulation.			1500	ms
$T_{AC_on_delay}$	Delay from AC being applied to all output voltages being within regulation.			5000	ms
T_{12V_holdup}	Time 12V output voltage stay within regulation after loss of AC. Po is full load	12			ms
$T_{PWOK_H_holdup}$	Delay from loss of AC to de-assertion of PWOK_H	10			ms
$T_{PSON_L_on_delay}$	Delay from PSON_L active to output voltages within regulation limits.	5		400	ms
$T_{PSKILL_on_delay}$	Delay from PSKILL active to output voltages within regulation limits.	5		5000	ms
$T_{PSON_L_PWOK_H}$	Delay from PSON_L deactivate to PWOK_H being de-asserted.			400	ms
$T_{PWOK_H_on}$	Delay from output voltages within regulation limits to PWOK_H asserted at turn on.	100		500	ms
$T_{PWOK_H_off}$	Delay from PWOK_H de-asserted to output voltages dropping out of regulation limits.	1			ms
$T_{PWOK_H_low}$	Duration of PWOK_H being in the de-asserted state during an off/on cycle using AC or the PSON_L signal.	100			ms
T_{VSB_holdup}	Time the 12VSB output voltage stays within regulation after loss of AC.	100			ms
$T_{AC_off_SMB_ALERT_L}$	The power supply shall assert the SMB_ALERT_L signal quickly after a loss of AC input voltage			4	ms

Table 7. Timing Requirements

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8.9 LED INDICATOR

The front-end PSU has one front LED showing the status of the supply. The LED is bi-colored: green and amber, that indicates input and output power presence, and warning or fault conditions. Table 9 lists the different LED status.

Color	MIN λd WAVELENGTH	NOMINAL λd WAVELENGTH	MAX λd WAVELENGTH	UNITS
Green	565		571	nm
Yellow	584		590	nm

Table 8. LED Characteristics

OPERATING CONDITION	LED STATE
Outputs ON and OK	Solid Green
No AC power to all power supplies	LED OFF
AC present and Only 12VSB on (Standby mode)	1Hz Blink Green
AC cord unplugged, 12VSB power comes from shared 12VSB bus	Solid Amber
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, OTP…	Solid Amber
Power supply in FW upload mode	2Hz Blink Green

Table 9. LED Status

9. I²C / POWER MANAGEMENT BUS COMMUNICATION

The PES front-end is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing are defined in Table 10 further characterized through:

- The SDA/SCL IOs use 3.3V logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery
- within 10 ms
- Recognizes any time Start/Stop bus conditions

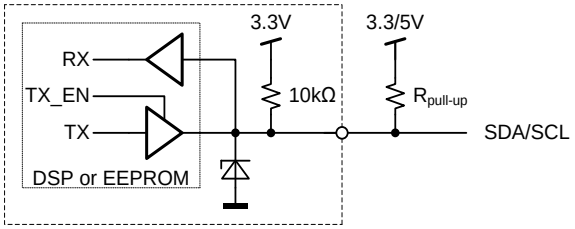

Figure 22. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V_{SB} output or V_1 output (provided e.g., by the redundant unit).

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		$20+0.1C_b$[1]	300	ns

t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1)]	250	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull-up}$	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[1)] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 10. I²C / SMBus Specification

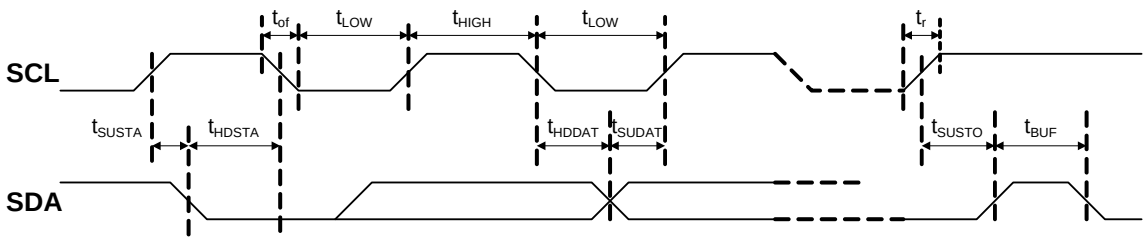

Figure 23. I²C / SMBus Timing

ADDRESS SELECTION

The address for I²C communication can be configured by pulling address input pin A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A0 pin to be in High Level if left open. A fixed addressing offset exists between the Controller and the EEPROM.

A2	A1	A0	I2C Address	
			Controller	EEPROM
X	0	0	0xB0	0xA0
X	0	1	0xB2	0xA2

Table 11. Address and Protocol Encoding

9.1 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 24) and can be accessed under different addresses, see Table 11.
The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3.3V.
The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

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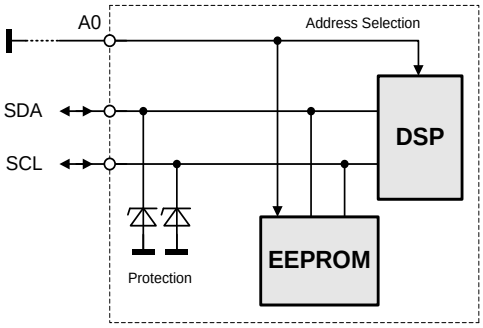


Figure 24 - I2C Bus to DSP and EEPROM

9.2 EEPROM PROTOCOL

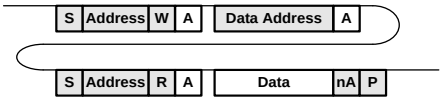
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



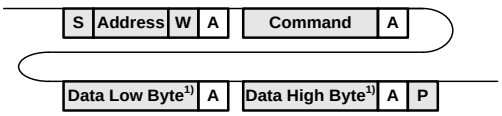
9.3 POWER MANAGEMENT BUS COOMUNICATION PROTOCOL

The Power Management Bus communication protocol is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus communication protocol command codes are not register addresses. They describe a specific command to be executed.
The PLS1600-12-080xA supply supports the following basic command structures:

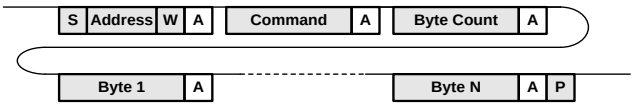
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

WRITE
The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



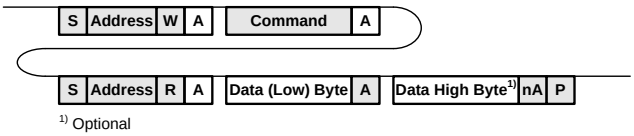
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes.



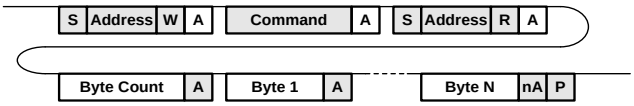
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes.



9.4 POWER SUPPLY DIAGNOSTIC "EVENT RECORDER"

The power supply shall save the latest data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible via the Power Management Bus communication interface with an external source providing power to the 12Vstby output.
Critical Events to trigger an update to the Event Recorder includes:

- Output OVP
- Output OCP
- Input OV/UV Fault
- Fan fault
- OTP
- Other faults to cause output shutdown.

Refer to BCA.20007, the Power Management Bus Communication Application Note for further information about the Power Management Bus Communication commands to support this function.

9.5 FIRMWARE UPDATE

The power supply shall have the capability to update its firmware via the Power Management Bus communication interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 12VSB pins. BPS standard GUI supports the firmware update function.

12VSB output remains on during and after firmware update period. Green LED should be blinking with 2 Hz frequency during firmware update period.

9.6 GRAPHICAL USER INTERFACE

Bel Power Solutions provide with its "I²C Utility" a Windows® XP/Vista/Win7/Win10 compatible graphical user interface allowing the programming and monitoring of the PLS1600-12-080xA Front-End.
The utility can be downloaded on: belfuse.com/power-solutions and supports both the PSMI and Power Management Bus communication protocols.
The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.
If the GUI is used in conjunction with the YTM.G2W01.0 Evaluation Board. It is also possible to control the PSON_L pin(s) of the power supply.

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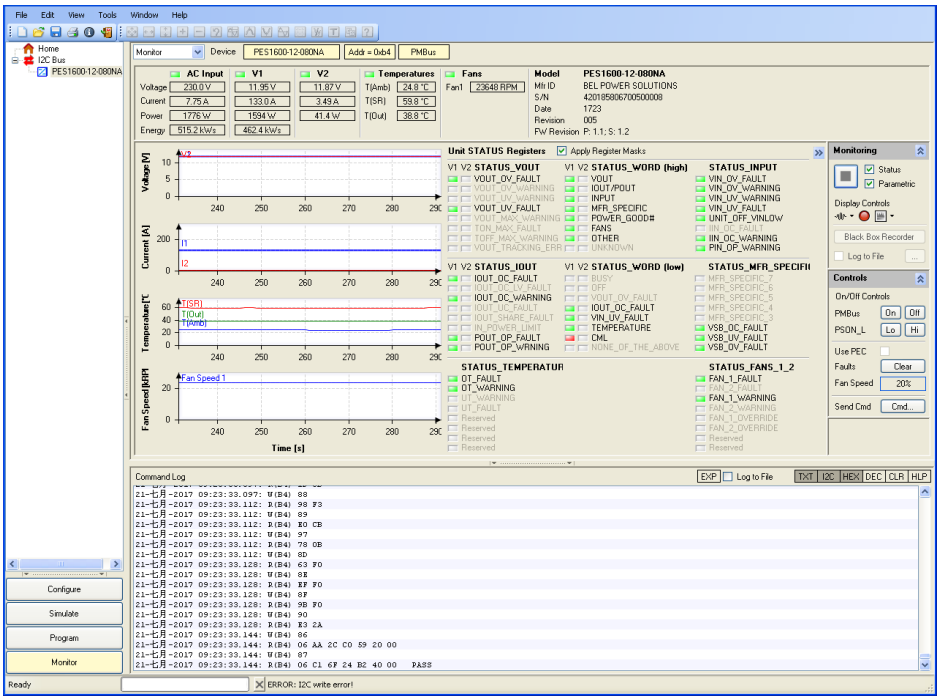

Figure 25. Monitoring dialog of the I²C Utility

10. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the air-flow at the rear of the supply by placing large objects directly at the output connector. The PLS1600-12-080NA is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. The PLS1600-12-080RA is provided with a front to rear airflow

The fan inside of the supply is controlled by a microprocessor. The rotate speed of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	POWER MANAGEMENT BUS REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet air temperature	Sensor located on airflow inlet	8Dh	60	65
Syn rectifier MOSFET	Sensor located close to Syn rectifier MOSFET	8Eh	NA: 90 RA:110	NA: 95 RA:115
Outlet air temperature	Sensor located on airflow outlet	8Fh	NA: 93 RA: 78	NA: 98 RA: 83
PFC heat sink	Sensor located on PFC heat sink HW OTP protection	\	\	115

Table 12. Temperature Sensor Location and Thresholds

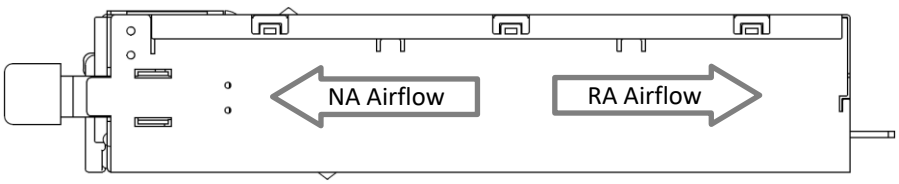

Figure 26. Airflow Direction

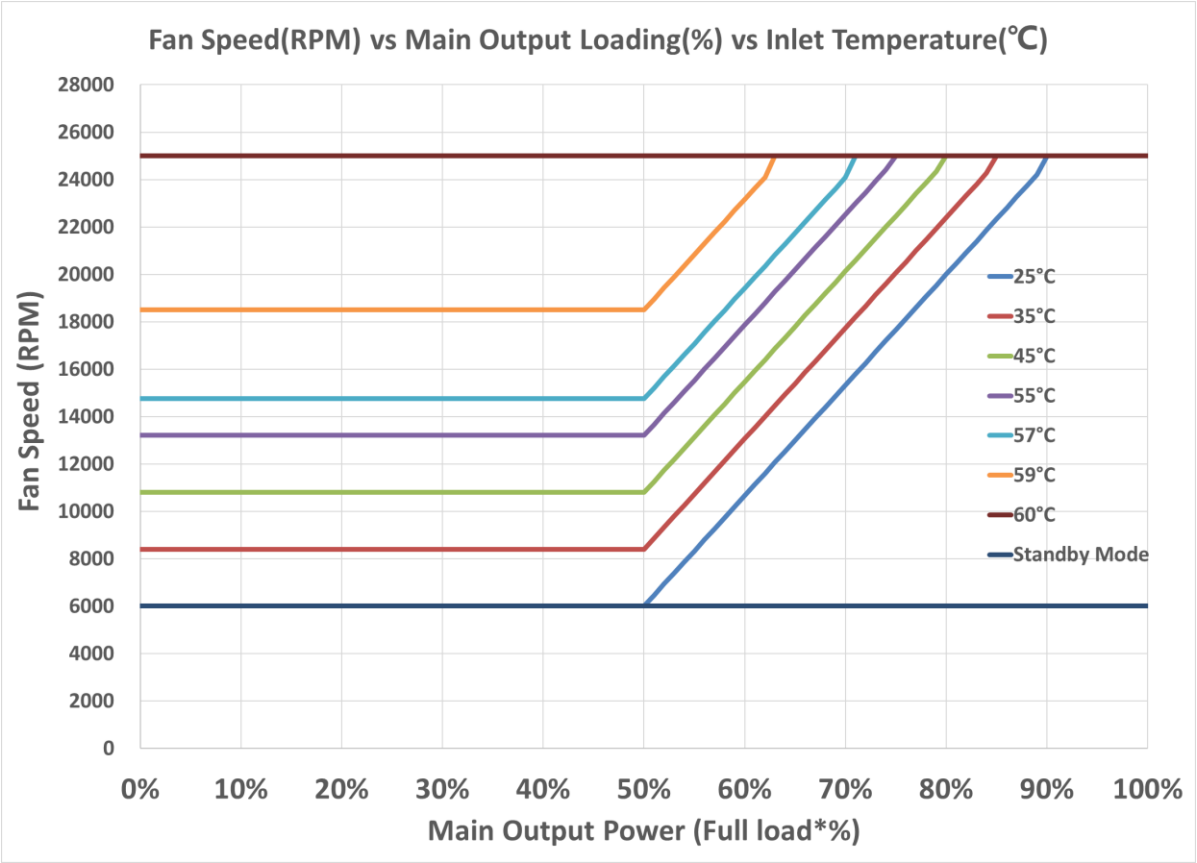

Figure 27. Fan Speed vs. Main Output Load & Inlet Temperature

Comment: The fan minimum speed is set to 6000RPM.

11. ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetics Filed	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation, 80 MHz…1 GHz	A
EFT/Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute	A
Surge*	IEC / EN 61000-4-5 Line to earth: ±2 kV, 2 Ohm Line to earth: ±4 kV, 12 Ohm Line to line: ±2 kV, 2 Ohm	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.15 … 80 MHz	A

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Harmonic Emissions	The power supply shall meet the requirements of EN61000-3-2	A
AC Flicker	IEC 61000-3-3, Vi = 230 VAC / 50Hz, 100% Load	
Voltage Dips and Interruptions	IEC/EN 61000-4-11	

LEVEL	DESCRIPTION
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

Table 13. Performance Criteria

11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single power supply	Class A (with 6dB margin)
	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, 2 power supplies in a system	Class A (with 6dB margin)
Radiated Emission	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, single power supply	Class A (with 6dB margin)
	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, 2 power supplies in a system	Class A (with 6dB margin)
Acoustical Noise	Sound power statistical declaration (ISO 9296, ISO 7779, IS9295) @ 50% load (20°C)	49dBA

Table 14. Emission

12. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	CAN/CSA-C22.2 No. 62368-1:19 UL 62368-1 3rd Ed. IEC 60950-1:2005 IEC/EN62368-1:2020; A11 BSMI: CNS13438 (95 version), CNS14336-1 (99 version) CQC: GB17625.1-2012, GB4943.1-2011, GB/T9254-2008 (Class A) BIS: IS 13252 (Part 1): 2010 + A1:2013 + A2:2015 EAC: IEC60950-1-2014	BSMI, CQC, BIS, EAC are pending for approval. (2021-04-14)
Isolation Strength	Input (L/N) to chassis (PE)	Basic
	Input (L/N) to output	Reinforced
	Output to chassis	None (Direct connection)
Electrical Strength Test	Input to output	4242 VDC
	Input to chassis	2121 VDC

Table 15. Safety and Approvals

13. ENVIRONMENTAL

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as “Handle, knobs, grips, etc. held for short periods of time only”.

In case the exit air temperature requirement cannot be met, the power supply must have a warning label for high touch temperature that is in compliance with IEC/UL 60950-1 and additionally 85°C rated power cords must also be used with this power supply.

ITEM		DESCRIPTION	MIN	NOM	MAX	UNITS
T_A	Operation Ambient Temperature	$V_{I\,min}$ to $V_{I\,max}$, $I_{1\,nom}$, $I_{SB\,nom}$ at 1800 m	-5		+55	°C
		$V_{I\,min}$ to $V_{I\,max}$, $I_{1\,nom}$, $I_{SB\,nom}$ at 4000 m	-5		+45	°C
T_S	Storage Temperature	Non-operational	-40		+70	°C
	Altitude	Operational, above Sea Level			4000	m

Table 16. Requirements for Non-Redundant Power Supply Configuration (High System Ambient)

13.1 HUMIDITY

Operating: To 85% relative humidity (non-condensing)

Non-Operating: To 95% relative humidity (non-condensing)

NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

13.2 ALTITUDE

Operating: To 1800m (Maximum operating altitude 4000 meters and the Maximum operating temperature to 45°C.)

Non-operating: To 12000m

13.3 SHOCK AND VIBRATION

13.3.1 RANDOM VIBRATION – OPERATING

Sample Size: For all product classes and categories, the minimum number of samples shall be 3 devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing -Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance. Each device shall be tested in three axes for a minimum of 30 minutes per axis. The device shall be powered for the duration of the test at nominal input voltage and no load. For operating vibration testing, see Figure 28

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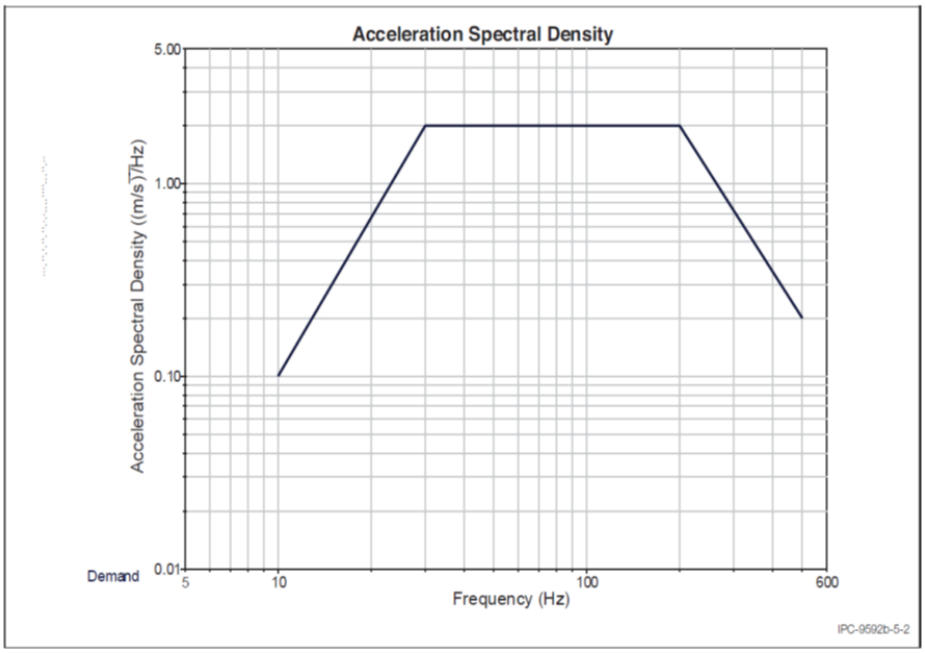

Figure 28. Class II PCDs Operating Vibration Test: Acceleration vs Frequency

The total acceleration for Class II PCDs is approximately 2.4g rms (See Table 18)

Frequency	Class I Acceleration Specification		Class II Acceleration Specification	
Hz	$(m/s^2)^2/Hz$	G^2/Hz	$(m/s^2)^2/Hz$	G^2/Hz
10	0.022	0.000229	0.1	0.00046
30	0.20	0.0021	2	0.0052
200	0.20	0.0021	2	0.0052
500	0.0052	0.000054	0.2	0.0001
	Grms = 0.71		Grms = 2.40	

Table 17. Operation Vibration Profile Charts

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

13.3.2 RANDOM VIBRATION - NON-OPERATING

Sample Size: For all product categories and product classes, the minimum number of samples shall be 3 devices packaged in their fully populated, bulk shipping package or individual packages of product.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing -Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance, with the acceleration spectral density curves provided in this document. The products are in the shipping packaging for this test. For non-operating vibration testing, see Table 18. Each shipping package shall be tested in three axes for a minimum of 30 minutes per axis.

The total acceleration for Class II PCDs is approximately 3.8g rms (See Table 18).

Frequency	Class I Acceleration Specification		Class II Acceleration Specification	
Hz	$(m/s^2)^2/Hz$	G^2/Hz	$(m/s^2)^2/Hz$	G^2/Hz
5	1	0.01	5	0.0052
200	1	0.01	5	0.0052
500	0.03	0.003	0.3	0.003
	Grms = 1.90		Grms = 3.80	

Table 18. Non-Operating Vibration Profile Charts

Pass Criteria: At the conclusion of all three axes of testing, the products shall be unpackaged and visually inspected for any signs of damage. Only minor cosmetic damage that does not affect form, fit or function is allowed. Bent connector pins, damaged switches, damaged handles, labels with impaired readability, or bent or deformed sheet metal are not allowed. All units shall also pass a functional test.
There are no requirements on the condition of the shipping package.

13.3.3 SHOCK – OPERATING

Sample Size: For all product types and product classes, the minimum number of samples shall be three devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-27, Environmental Testing- Part 2.27 Test Ea and guidance: Shock. Each tested device shall be exposed to three shocks in each of 3 axes. The amplitude of each shock shall be no less than 30 g with a half sine wave shape and a duration of 11mS.

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

13.3.4 THERMAL SHOCK (SHIPPING)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

14. RELIABILITY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	Mean time between failure	T_A = 40°C, 75% load, according Telcordia SR-332, issue 2	250			kh

Comment: All components de-rating follow IPC9592B latest revision.

15. MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width Heigth Depth		80 40 195		mm mm mm
m	Weight			1		kg

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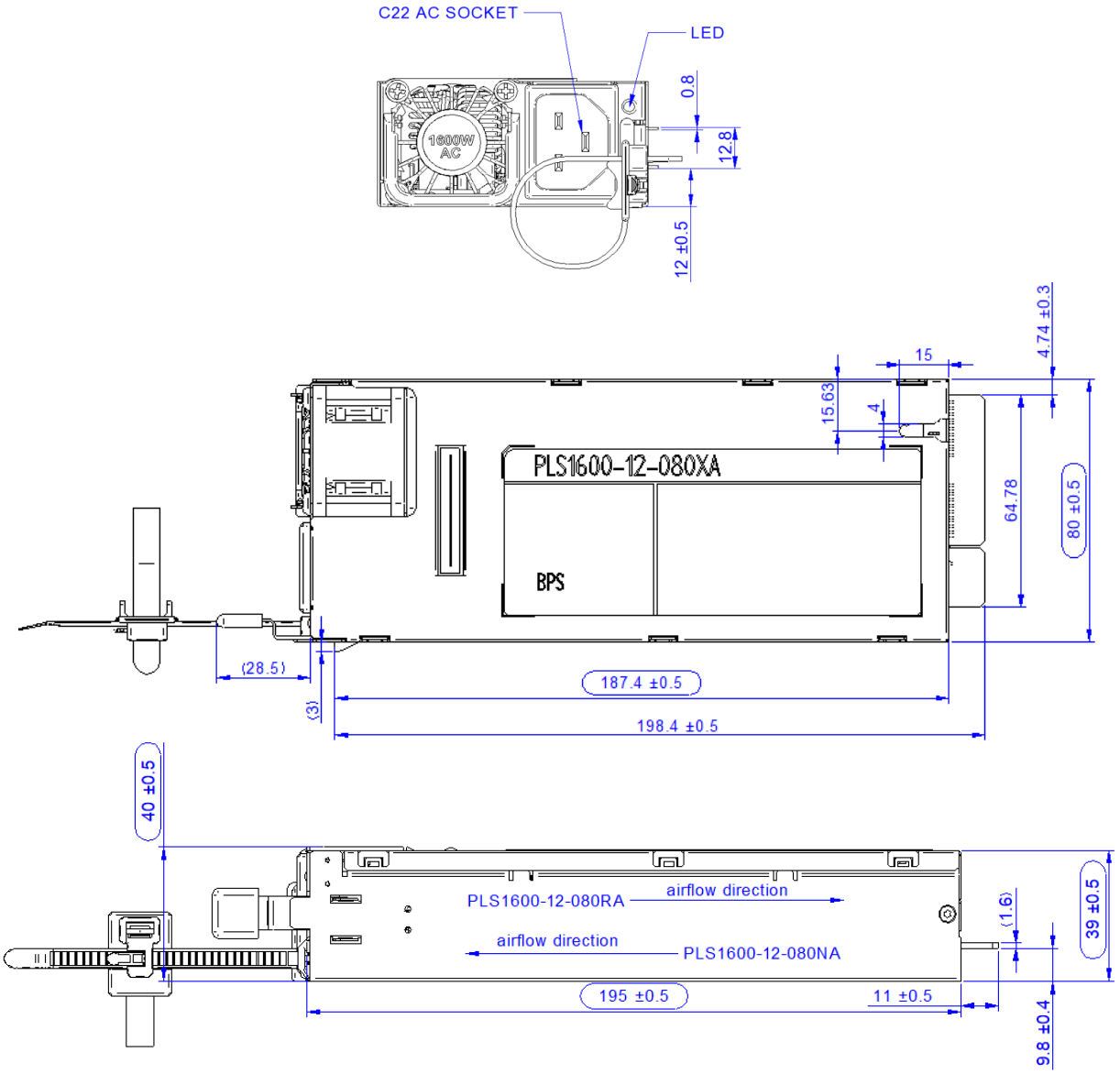

Figure 29. Front, top and side view

16. CONNECTORS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Input Connector	IEC 60320 C22				
AC cord requirement	Wire size		16		AWG
Output connector	36 Power + 24 signals Pins PCB card edge				
Mating output connector	Manufacturer : FCI Electronics Manufacturer P/N: 10130248-005LF BEL P/N: ZES.00678				

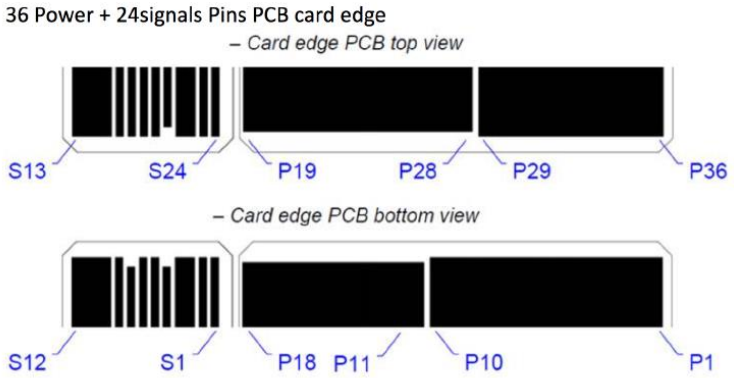

Figure 30. Output gold finger in PSU

PIN	SIGNAL NAME	DESCRIPTION	Mating Sequence[1)]
P1 ~ P10 P29 ~ P36	P12V_MAIN_RTN P12V_STNDBY_RTN	+12V main and 12V Standby Power Ground (Return)	1
P11 ~ P18 P19 ~ P28	P12V_MAIN_OUT	+12V main output	2
S1	I2C_A0	I2C Address Pin	1
S2	NC	Reserved	1
S3, S4	P12V_STNDBY_OUT	+12V Standby Output	1
S5	PSKILL	Shuts off power supply both 12V Main and 12V Standby outputs	3
S6	P12V_ISHARE	Main Output Current Bus for Active Current Sharing Used	1
S7	VIN_OK_H (ACOK_H)	Input OK signal output, active-high	1
S8	PRESENT_L (PS_SEATED_L)	Connected to Power Supply Ground	3
S9	NC	Reserved	1
S10 ~ S15	SGND	I2C Signal Ground Pin and 12V Standby Return	1
S16	PWOK_H (DCOK_H)	Power OK signal output, active-high	1
S17	MAIN_SENSE	Main output Remote Sense	1
S18	MAIN_SENSE_RTN	Main output Return of Remote Sense	1
S19	SMB_ALERT_L (INTERRUPT_L)	Same as or similar to SMBALERT#. Active on warning or error conditions	1
S20	PSON_L	Low=12V Main ON, High=12V Main OFF	2
S21, S22	P12V_STNDBY_OUT	+12V Standby Output	1
S23	I2C_SCL	I2C Clock Pin	2
S24	I2C_SDA	I2C Data Pin	2

[1)] 1 = First, 2= Second, 3 = Last, given by different card edge finger pin lengths and mating connector pin arrangement

Table 19. Output connector pin assignment

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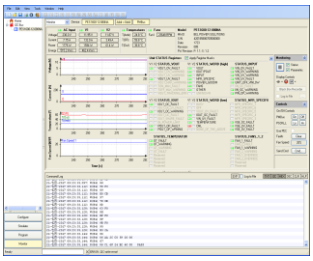
17. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**I²C Utility** Windows® XP/Vista/Win7/Win10 compatible GUI to program, control and monitor Front-End power supplies (and other I²C units)	N/A	belfuse.com/power-solutions
	Evaluation Board Connector board to operate PLS1600-12-080xA. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).	YTM.G2W01.0	belfuse.com/power-solutions

18. REVISION HISTORY

REVISION	DESCRIPTION OF CHANGES	DATE	ORIGINATOR
A-0	Release to A-0 revision	2021-06-02	Gang Wang

For more information on these products consult: tech.support@psbel.com

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