SERIES: P78E-1000 | **DESCRIPTION:** NON-ISOLATED DC SWITCHING REGULATOR

FEATURES

- 1 A of output current
- efficiency up to 96%
- industry standard SIP package
- industrial operating temp -40~+85°C
- drop in equivalent LM78 regulator
- no load input current of 0.2 mA
- output short circuit protection on output
- designed to meet EN/BS EN 62368

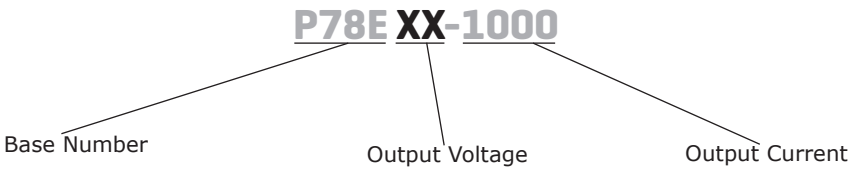
RoHS

MODEL

MODEL	input voltage[1] typ (Vdc)	input voltage[1] range (Vdc)	output voltage (Vdc)	output current max (mA)	output power max (W)	ripple & noise[2] max (mVp-p)	efficiency[3] typ (%)
P78E03-1000	24	6~36	3.3	1000	3.3	75	90
P78E05-1000	24	8~36	5	1000	5	75	93
	12	8~27	-5	-500	2.5	75	85
P78E09-1000	24	13~36	9	1000	9	75	94
P78E12-1000	24	16~36	12	1000	12	75	95
	12	8~20	-12	-300	3.6	75	88
P78E15-1000	24	20~36	15	1000	15	75	96
	12	8~18	-15	-300	4.5	75	87

Notes:
1. For input voltages higher than 30 Vdc, a 22 µF / 50 V input capacitor is required.
2. Tested at nominal input, 20~100% load, 20 MHz bandwidth, with 10 µF electrolytic and 1 µF ceramic capacitor on the output. At loads below 20%, the max ripple and noise of the 3.3 & 5 Vdc outputs will be 100 mVp-p, and the other outputs will be 2% Vo.
3. Measured at min Vin, full load.
4. All specifications are measured at Ta=25°C, humidity < 75%, nominal input voltage, and rated output load unless otherwise specified.

PART NUMBER KEY



INPUT

parameter	conditions/description	min	typ	max	units
operating input voltage[5]	for positive output applications for negative output applications	6 8		36 27	Vdc Vdc
filter	capacitor filter				
input reverse polartiy protection	no				
no-load input current	positive outputs negative outputs		0.3 1	1 4	mA mA

Note: 5. See Model section on page 1 for specific input voltage ranges.

OUTPUT

parameter	conditions/description	min	typ	max	units
maximum capacitive load[6]	for positive output applications for negative output applications			680 330	µF µF
voltage accuracy	at full load, input voltage range 3.3 Vdc output model all other models		 ±2 ±1.5	 ±4 ±3	 % %
line regulation	at full load, input voltage range		±0.2	±0.4	%
load regulation	at nominal input, 10~100% load positive output applications negative output applications		 ±0.4 ±0.4	 ±0.6 ±0.8	 % %
switching frequency	at nominal input voltage, full load		520		kHz
transient recovery time	at nominal input voltage, 25% load step change			1	ms
transient response deviation	at nominal input voltage		±60	±200	mV
temperature coefficient	at full load			±0.03	%/°C

Note: 6. The maximum capacitive load was tested at nominal input voltage, full load.

PROTECTIONS

parameter	conditions/description	min	typ	max	units
short circuit protection	continuous, auto recovery				

SAFETY AND COMPLIANCE

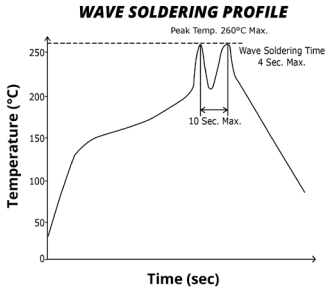
parameter	conditions/description	min	typ	max	units
safety approvals	designed to meet 62368: EN/BS EN				
conducted emissions	CISPR32/EN55032, class B (external circuit required, see Figure 4/5-b)				
radiated emissions	CISPR32/EN55032, class B (external circuit required, see Figure 4/5-b)				
ESD	IEC/EN61000-4-2, contact ± 4kV, class B				
radiated immunity	IEC/EN61000-4-3, 10V/m, class A				
EFT/burst	IEC/EN61000-4-4, ± 1kV, class B (external circuit required, see Figure 4/5-a)				
surge	IEC/EN61000-4-5, line-line ± 1kV, class B (external circuit required, see Figure 4/5-a)				
conducted immunity	IEC/EN61000-4-6, 3 Vr.m.s, class A				
MTBF	as per MIL-HDBK-217F, 25°C	2,000,000			hours
RoHS	yes				

ENVIRONMENTAL

parameter	conditions/description	min	typ	max	units
operating temperature	see derating curves	-40		85	°C
storage temperature		-55		125	°C
storage humidity	non-condensing			95	%

SOLDERABILITY

parameter	conditions/description	min	typ	max	units
wave soldering	see wave soldering profile			260	°C



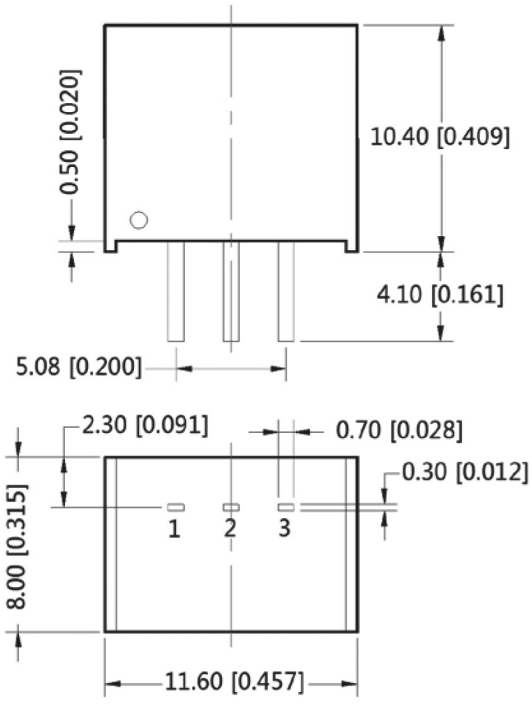
MECHANICAL

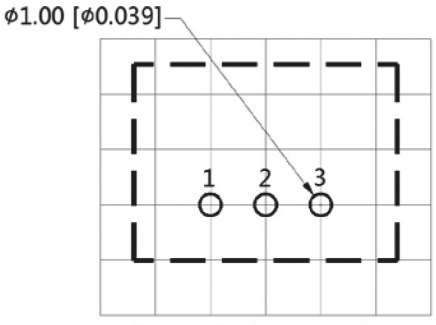
parameter	conditions/description	min	typ	max	units
dimensions	11.6 x 8.0 x 10.40 [0.457 x 0.315 x 0.409 inch]				mm
case material	black flame-retardant and heat-resistant plastic (UL94 V-0)				
weight			1.9		g

MECHANICAL DRAWING

units: mm [inch]
tolerance: ±0.50[±0.020]
pin diameter tolerance: ±0.10[±0.004]

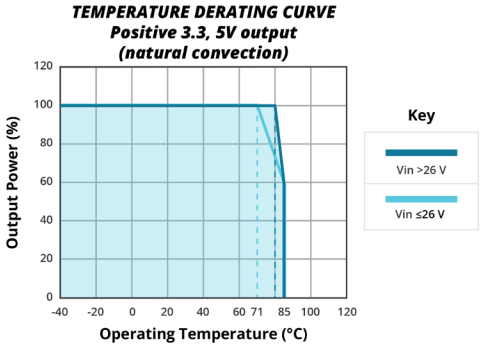
PIN CONNECTIONS		
PIN	+OUTPUT	-OUTPUT
1	+VIN	+VIN
2	GND	-VOUT
3	+VOUT	GND

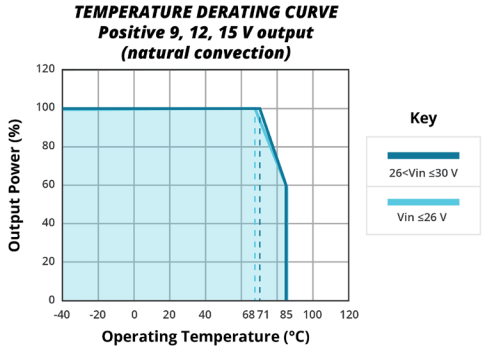


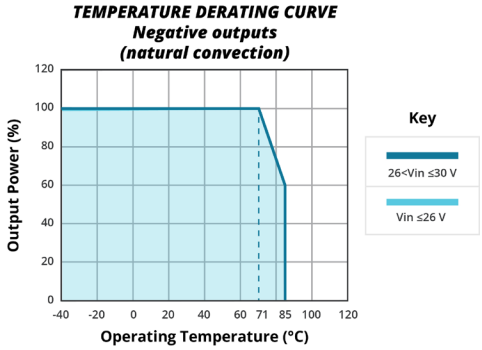


Note : Grid 2.54*2.54mm
Recommended PCB Layout
Top View

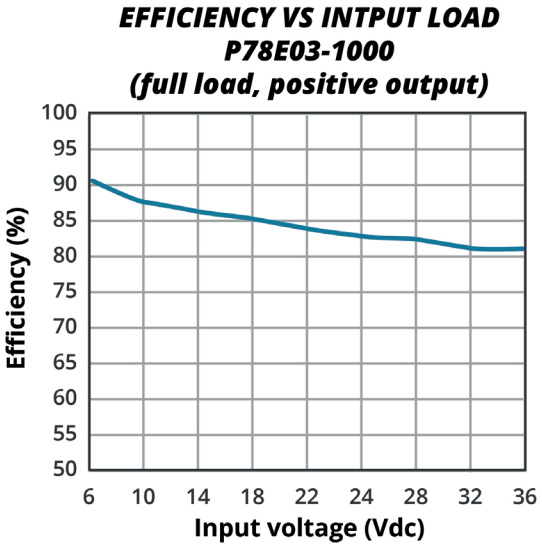
DERATING CURVES

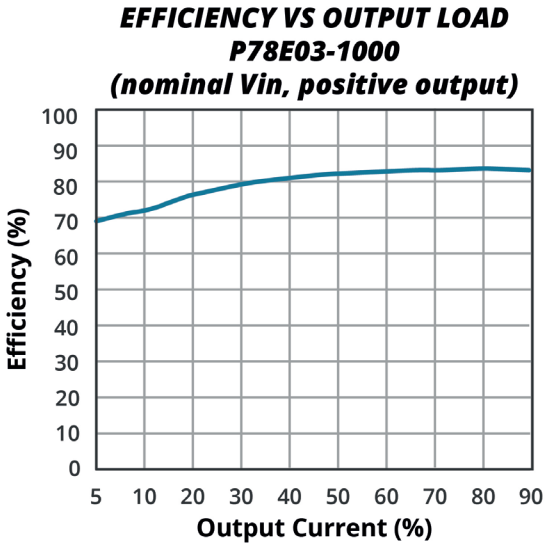


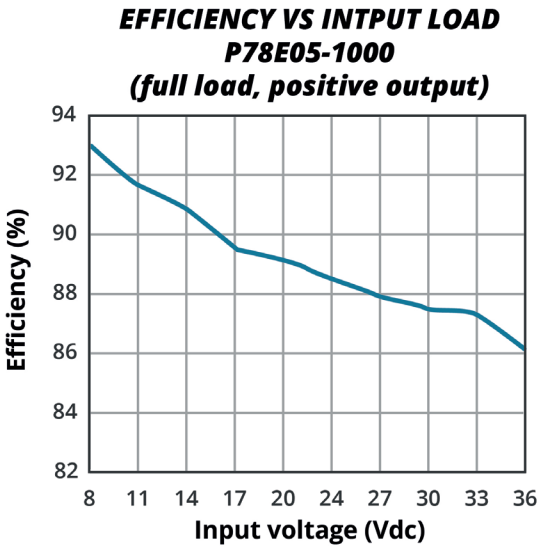


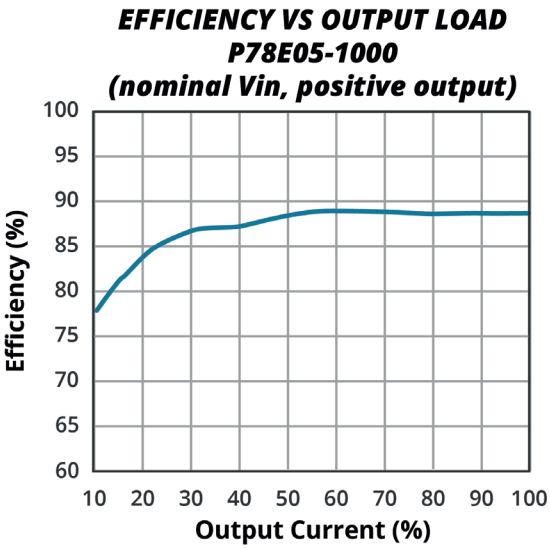


EFFICIENCY CURVES



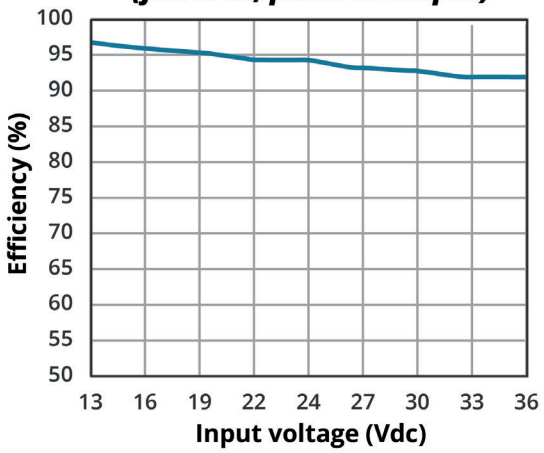




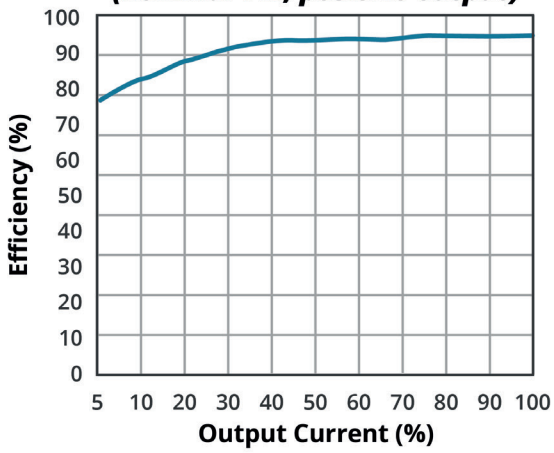


EFFICIENCY CURVES (CONTINUED)

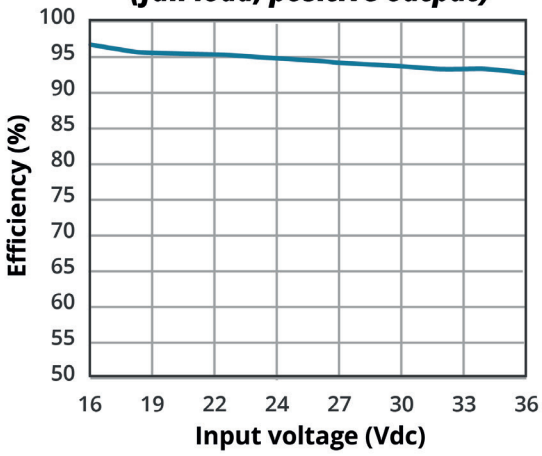
EFFICIENCY VS INTPUT LOAD
P78E09-1000
(full load, positive output)



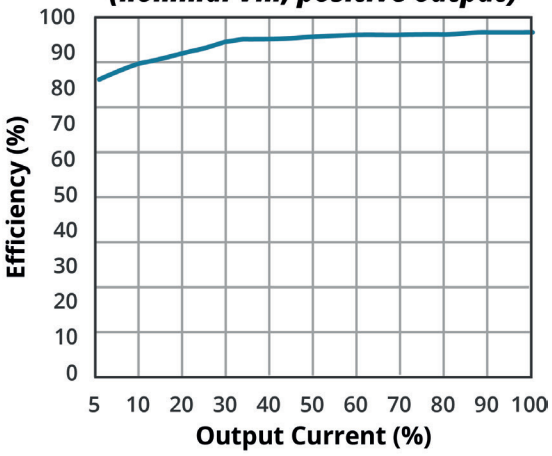
EFFICIENCY VS OUTPUT LOAD
P78E09-1000
(nominal Vin, positive output)



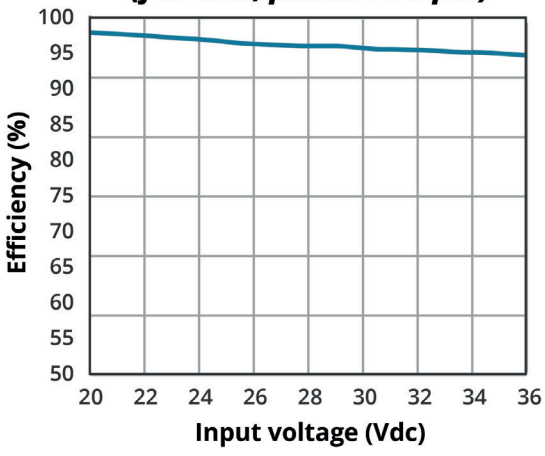
EFFICIENCY VS INTPUT LOAD
P78E12-1000
(full load, positive output)



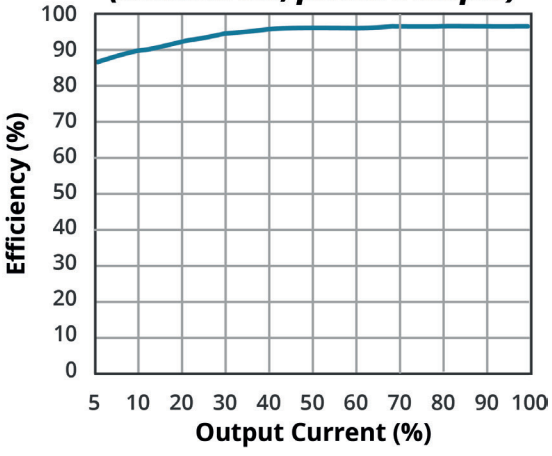
EFFICIENCY VS OUTPUT LOAD
P78E12-1000
(nominal Vin, positive output)



EFFICIENCY VS INTPUT LOAD
P78E15-1000
(full load, positive output)



EFFICIENCY VS OUTPUT LOAD
P78E15-1000
(nominal Vin, positive output)



TYPICAL APPLICATION CIRCUIT

Figure 1
Positive Output Application Circuit

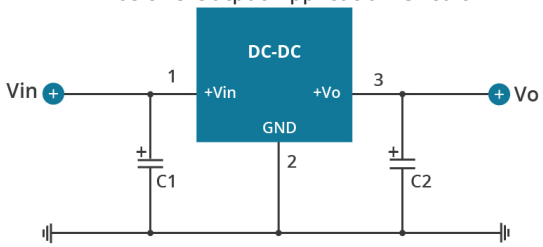


Figure 2
Negative Output Application Circuit

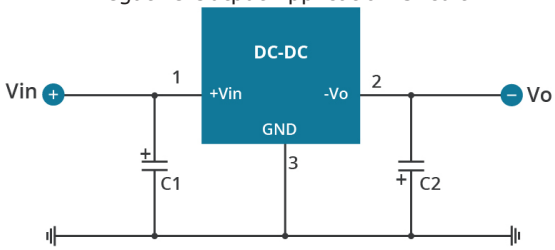


Figure 3
Positive and Negative Output Paralleling Application Circuit

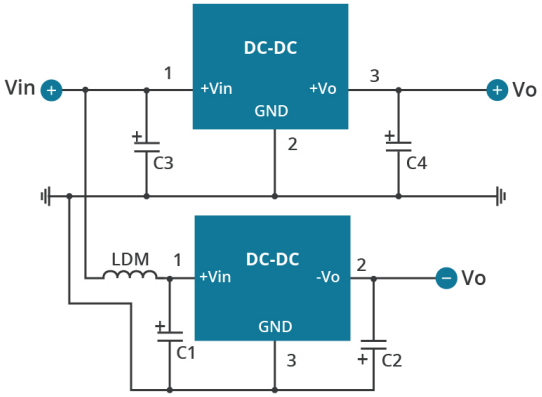


Table 1
External Capacitor Table

Model Number	C1, C3 (ceramic capacitor)	C2, C4 (ceramic capacitor)
P78E03-1000	10 µF/50 V	22 µF/10 V
P78E05-1000	10 µF/50 V	22 µF/10 V
P78E09-1000	10 µF/50 V	22 µF/16 V
P78E12-1000	10 µF/50 V	22 µF/25 V
P78E15-1000	10 µF/50 V	22 µF/25 V

EMC RECOMMENDED CIRCUIT

Figure 4
Positive output

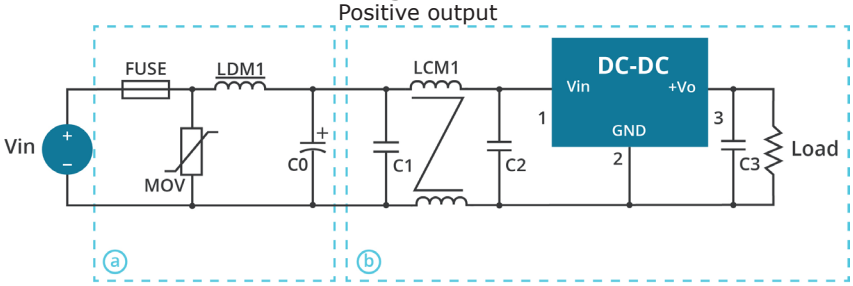


Table 2

Recommended external circuit components	
FUSE	choose according to actual input current
MOV	20D470K
LDM1	82 µH
C0	680 µF/50 V
LCM1	4.7 mH
C1, C2	4.7 µF/50 V
C3	10 µF/50 V

Figure 5
Negative output

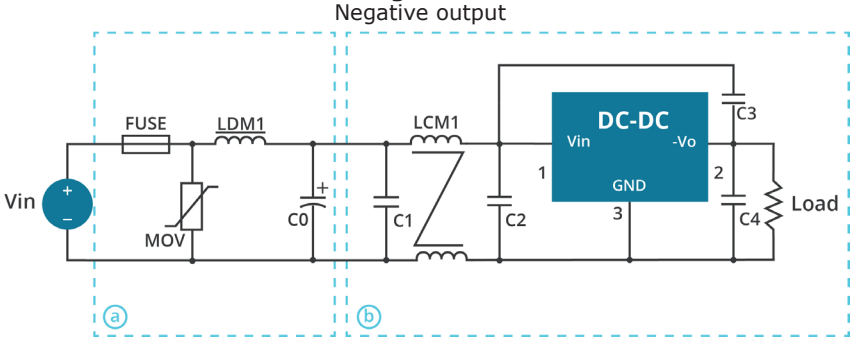


Table 3

Recommended external circuit components	
FUSE	choose according to actual input current
MOV	20D470K
LDM1	82 µH
C0	680 µF/50 V
LCM1	4.7 mH
C1, C3, C4	4.7 µF/50 V
C2	10 µF/50 V

Note:
7. C1 & C2 (C3 & C4) are required and should be connected as close to the module pins as possible.
8. To reduce the output ripple further, C2 & C4 can be increased as needed and the use of tantalum or low ESR electrolytic capacitors would be recommended.
9. When using application circuit in Figure 3, a 10 µH LDM component is recommended to reduce the interference.

REVISION HISTORY

rev.	description	date
1.0	initial release	09/12/2018
1.01	features and safety line updated, packaging removed	01/14/2021
1.02	derating curves, efficiency curves and circuit figures updated	09/20/2021
1.03	CE removed	11/04/2022
1.04	application circuit updated	03/22/2023

The revision history provided is for informational purposes only and is believed to be accurate.

CUI INC
a bel group

Headquarters
20050 SW 112th Ave.
Tualatin, OR 97062
800.275.4899

Fax 503.612.2383
cui.com
techsupport@cui.com